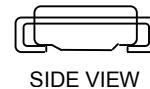
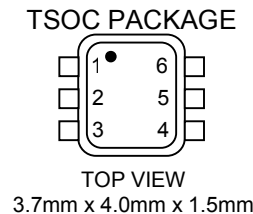


## FEATURES

- 4096 bits of SRAM
- Four 32-bit, read-only counters
- Active-low external trigger inputs for two of the counters with on-chip debouncing compatible with reed and Wiegand switches
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester) assures absolute traceability because no two parts are alike
- Memory partitioned into 16 256-bit pages in for packetizing data
- 256-bit scratchpad with strict read/write protocols ensures integrity of data transfer
- On-chip 16-bit CRC generator for safeguarding data transfers
- Built-in multidrop controller ensures compatibility with other MicroLAN products
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3kbits per second
- Overdrive mode boosts communication speed to 142kbits per second
- 8-bit family code specifies device communication requirements to reader

- Presence detector acknowledges when reader first applies voltage
- Compact, low cost 6-pin TSOC surface mount package
- Reads, writes and counts over a wide voltage range of 2.8V to 5.5V from -40°C to +85°C

## PIN ASSIGNMENT



## PIN DESCRIPTION

Pin 1	Ground
Pin 2	Data
Pin 3	Vbat
Pin 4	NC
Pin 5	Input channel B
Pin 6	Input channel A

## ORDERING INFORMATION

DS2423P	6-pin TSOC package
DS2423P/T&R	Tape & Reel Version of DS2423P
DS2423X	Chip Scale Pkg., Tape & Reel

## DESCRIPTION

The DS2423 1-Wire<sup>®</sup> RAM with Counters is a fully static, read/write memory for battery operation in a low-cost, six-lead TSOC, surface-mount package. The memory is organized as 16 pages of 256 bits each. In addition, the device has four counters, two of them with external trigger inputs called A and B. Each of the counters is associated with a memory page. A counter without external trigger input increments each time data is written to the page it is associated with (write cycle counter). The counters triggered by inputs A and B, respectively, increment with every low-going pulse on their input. All counters are read-only. They are automatically cleared to 0 when the battery is connected.

The battery-backed memory offers a simple solution to storing and retrieving information pertaining to the equipment where the DS2423 is installed and its frequency of use. The scratchpad is an additional page that acts as a buffer when writing to memory. Data is first written to the scratchpad where it may be read back for verification. A copy scratchpad command will then transfer the data to memory. This process ensures data integrity when modifying the memory. A 64-bit registration number is factory lasered into each DS2423 to provide a guaranteed unique identity which allows for absolute traceability and acts as node address if multiple DS2423 are connected in parallel to form a local network. Data is transferred serially via the 1-Wire protocol, which requires only a single data lead and a ground return.

The DS2423 1-Wire RAM with Counters can store encrypted data. The unique registration number and the page write cycle counter(s) prevent unauthorized manipulation of data stored in a page with a write cycle counter associated.

## OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS2423. The DS2423 has four main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, 3) 4096-bit SRAM, and 4) four 32-bit read-only counters. The hierarchical structure of the 1-Wire protocol is shown in Figure 2. Each of these counters is associated with one of the 256-bit memory pages. The four counters of the DS2423 are associated with pages 12 to 15. The contents of the counter is read together with the memory data using a special command. The bus master must first provide one of the six ROM Function Commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, 5) Overdrive-Skip ROM or 6) Overdrive-Match ROM. Upon completion of an Overdrive ROM command byte executed at standard speed, the device will enter Overdrive mode where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 9. After a ROM function command is successfully executed, the memory functions become accessible and the master may provide any one of the five memory function commands. The protocol for these memory function commands is described in Figure 7. All data is read and written least significant bit first.

## PARASITE POWER

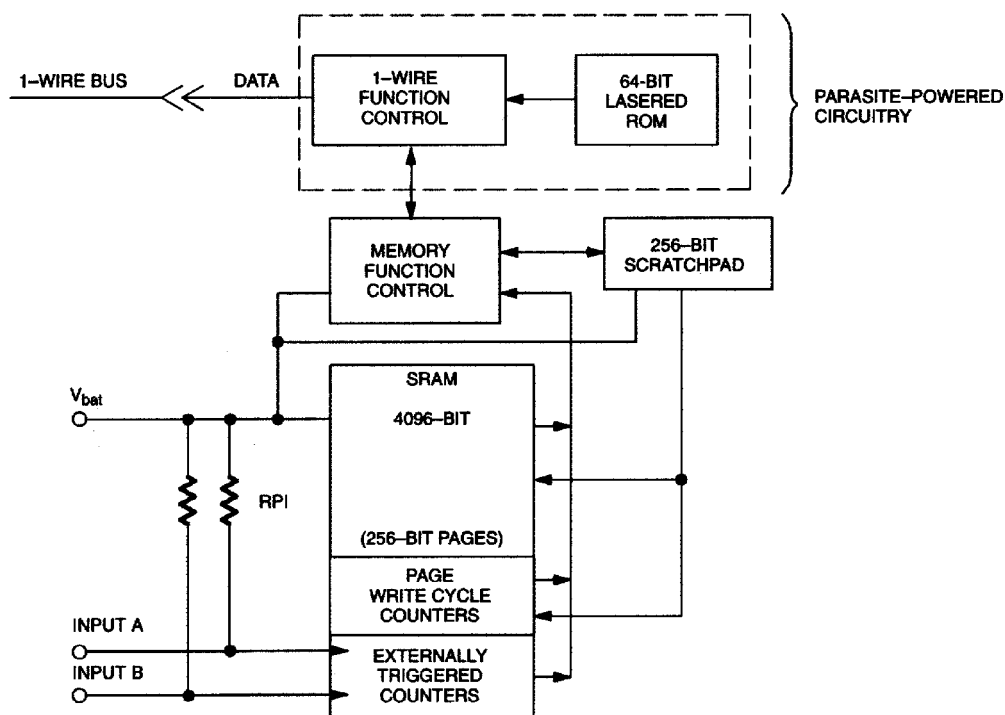
The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry steals power whenever the I/O input is high. I/O will provide sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) by parasiting off this input, lithium is conserved, and 2) if the battery is exhausted for any reason, the ROM may still be read normally.

## 64-BIT LASERED ROM

Each DS2423 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits (See Figure 3). The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is  $X^8 + X^5 + X^4 + 1$ . Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in the *Book of DS19xx iButton® Standards*.

The shift register bits are initialized to 0. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8<sup>th</sup> bit of the family code has been entered, then the serial number is entered. After the 48<sup>th</sup> bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC should return the shift register to all 0s.

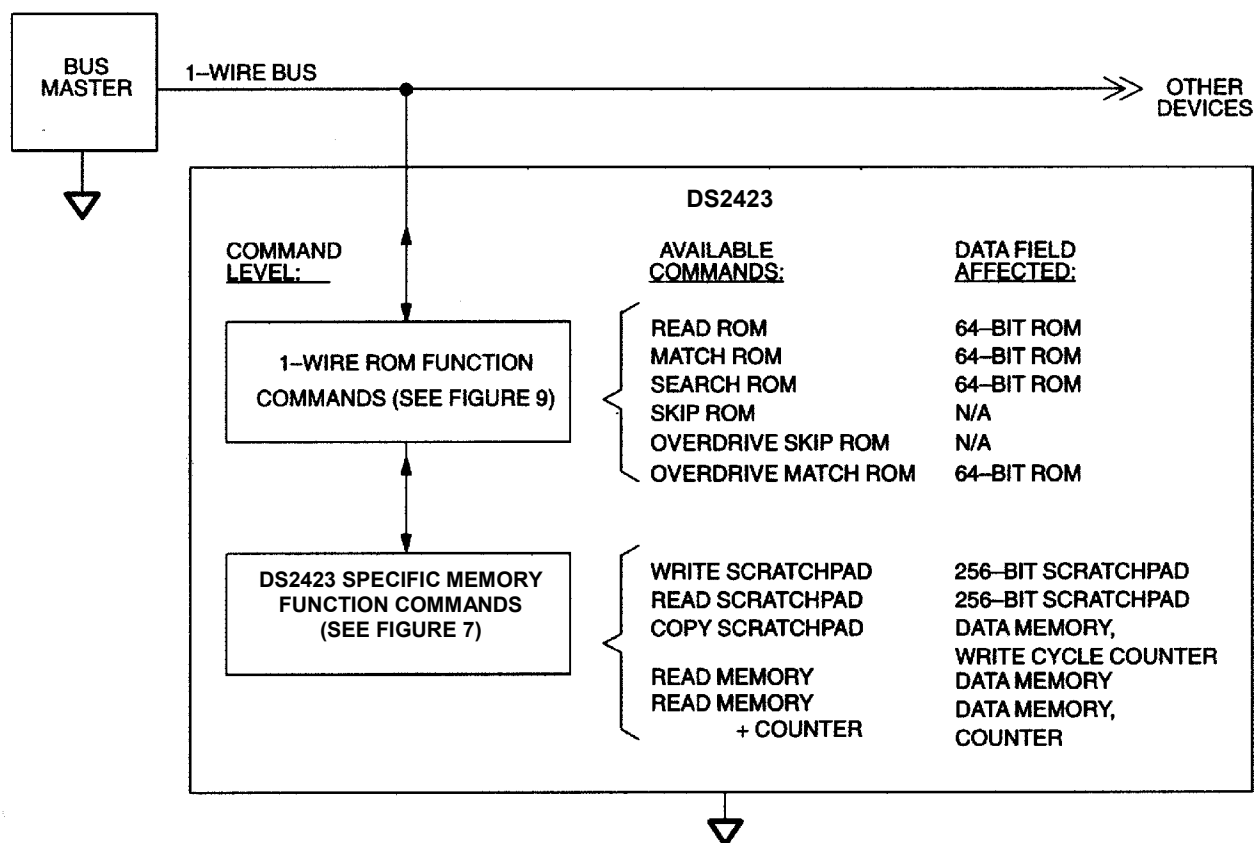
## BLOCK DIAGRAM Figure 1



## ADDRESS REGISTERS AND TRANSFER STATUS

Because of the serial data transfer, the DS2423 employs three address registers called TA1, TA2, and E/S (Figure 6). Registers TA1 and TA2 must be loaded with the target address to which the data will be written or from which data will be sent to the master upon a Read command. Register E/S acts like a byte counter and Transfer Status register. It is used to verify data integrity with write commands. Therefore, the master only has read access to this register. The lower 5 bits of the E/S register indicate the address of the last byte that has been written to the scratchpad. This address is called Ending Offset. Bit 5 of the E/S register, called PF or “partial byte flag,” is set if the number of data bits sent by the master is not an integer multiple of 8. Bit 6 has no function; it always reads 0. Note that the lowest 5 bits of the target address also determine the address within the scratchpad, where intermediate storage of data will begin. This address is called byte offset. If the target address (TA1) for a Write command is 03CH for example, then the scratchpad will store incoming data beginning at the byte offset 1CH and will be full after only 4 bytes. The corresponding ending offset in this example is 1FH. For best economy of speed and efficiency, the target address for writing should point to the beginning of a new page, i.e., the byte offset will be 0. Thus the full 32-byte capacity of the scratchpad is available, resulting also in the ending offset of 1FH. However, it is possible to write one or several contiguous bytes somewhere within a page. The ending offset together with the Partial Flag support the master checking the data integrity after a Write command. The highest valued bit of the E/S register, called AA or Authorization Accepted, acts as a flag to indicate that the data stored in the scratchpad has already been copied to the target memory address. Writing data to the scratchpad clears this flag.

## HIERARCHICAL STRUCTURE FOR 1-WIRE PROTOCOL Figure 2

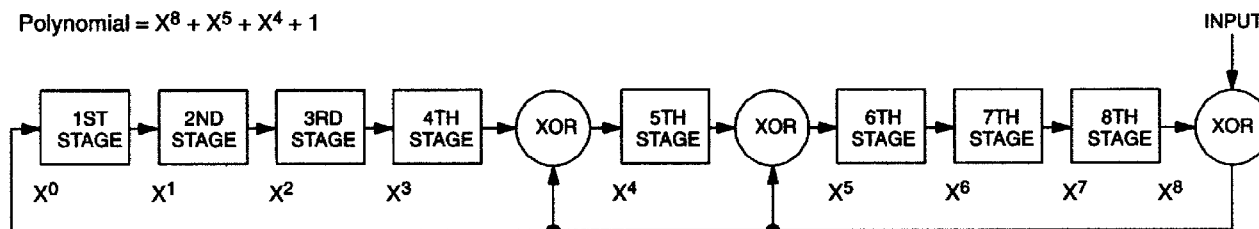


## 64-BIT LASERED ROM Figure 3



## 1-WIRE CRC GENERATOR Figure 4

$$\text{Polynomial} = X^8 + X^5 + X^4 + 1$$



## WRITING WITH VERIFICATION

To write data to the DS2423, the scratchpad has to be used as intermediate storage. First the master issues the Write Scratchpad command to specify the desired target address, followed by the data to be written to the scratchpad. Under certain conditions (see Write Scratchpad command) the master will receive an inverted CRC16 of the command, address and data at the end of the Write Scratchpad command sequence. Knowing this CRC value, the master can compare it to the value it has calculated itself to decide if the communication was successful and proceed to the Copy Scratchpad command. If the master could not receive the CRC16, it has to send the Read Scratchpad command to read back the scratchpad to verify data integrity. As preamble to the scratchpad data, the DS2423 repeats the target address TA1 and TA2 and sends the contents of the E/S register. If the PF flag is set, data did not arrive correctly in the scratchpad. The master does not need to continue reading; it can start a new trial to write data to the scratchpad. Similarly, a set AA flag indicates that the Write command was not recognized by the device. If everything went correctly, both flags are cleared and the ending offset indicates the address of the last byte written to the scratchpad. Now the master can continue reading and verifying every data byte. After the master has verified the data, it has to send the Copy Scratchpad command. This command must be followed exactly by the data of the three address registers TA1, TA2 and E/S. The master may obtain the contents of these registers by reading the scratchpad or derive it from the target address and the amount of data to be written. As soon as the DS2423 has received these bytes correctly, it will copy the data to the requested location beginning at the target address.

## MEMORY FUNCTION COMMANDS

The Memory Function Flow Chart (Figure 7) describes the protocols necessary for accessing the memory. An example follows the flowchart. The communication between master and DS2423 takes place either at regular speed (default, OD = 0) or at Overdrive speed (OD = 1). If not explicitly set into the Overdrive mode the DS2423 assumes regular speed.

### Write Scratchpad Command [0FH]

After issuing the Write Scratchpad command, the master must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data will be written to the scratchpad starting at the byte offset (T4:T0). The ending offset (E4:E0) will be the byte offset at which the master stops writing data. Only full data bytes are accepted. If the last data byte is incomplete its content will be ignored and the partial byte flag PF will be set.

When executing the Write Scratchpad command the CRC generator inside the DS2423 (see Figure 12) calculates a CRC over the entire data stream, starting at the command code and ending at the last data byte sent by the master. This CRC is generated using the CRC16 polynomial by first clearing the CRC generator and then shifting in the command code (0FH) of the Write Scratchpad command, the Target Addresses TA1 and TA2 as supplied by the master and all the data bytes. The master may end the Write Scratchpad command at any time. However, if the ending offset is 11111b, the master may send 16 read time slots and will receive the CRC generated by the DS2423.

The memory address range of the DS2423 is 0000H to 01FFH. If the bus master sends a target address higher than this, the internal circuitry of the chip will set seven most significant address bits to 0 as they are shifted into the internal address register. The Read Scratchpad command will reveal the target address as it will be used by the DS2423. The master will identify such address modifications by comparing the target address read back to the target address transmitted. If the master does not read the scratchpad, a subsequent Copy Scratchpad command will not work since the most significant bits of the target address the master sends will not match the value the DS2423 expects.

---

## **Read Scratchpad Command [AAH]**

This command is used to verify scratchpad data and target address. After issuing the Read Scratchpad command, the master begins reading. The first 2 bytes will be the target address. The next byte will be the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset (T4: T0). The master may read data until the end of the scratchpad after which the data read will be all logic 1s.

## **Copy Scratchpad [5AH]**

This command is used to copy data from the scratchpad to memory. After issuing the Copy Scratchpad command, the master must provide a 3-byte authorization pattern which can be obtained by reading the scratchpad for verification. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA (Authorization Accepted) flag will be set and the copy will begin. A pattern of alternating 1s and 0s will be transmitted after the data has been copied until a Reset Pulse is issued by the master. Any attempt to reset the part will be ignored while the copy is in progress. Copy typically takes 30 $\mu$ s. The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset will be copied to memory, starting at the target address. Anywhere from 1 to 32 bytes may be copied to memory with this command. The AA flag will be cleared only by executing a Write Scratchpad command.

## DS2423 MEMORY MAP Figure 5

32-BYTE INTERMEDIATE STORAGE SCRATCHPAD		
ADDRESS		
0000H TO 001FH	32-BYTE FINAL STORAGE NV RAM	page 0
0020H TO 003FH	32-BYTE FINAL STORAGE NV RAM	page 1
0040H TO 005FH	32-BYTE FINAL STORAGE NV RAM	page 2
0060H TO 007FH	32-BYTE FINAL STORAGE NV RAM	page 3
0080H TO 017FH	FINAL STORAGE NV RAM	page 4 to page 11
0180H TO 019FH	32-BYTE FINAL STORAGE NV RAM	page 12
01A0H TO 01BFH	32-BYTE FINAL STORAGE NV RAM	page 13
01C0H TO 01DFH	32-BYTE FINAL STORAGE NV RAM	page 14
01E0H TO 01FFH	32-BYTE FINAL STORAGE NV RAM	page 15

## ADDRESS REGISTERS Figure 6

TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	1)	PF	E4	E3	E2	E1	E0

1) THIS BIT WILL ALWAYS BE 0.

## Read Memory [F0H]

The read memory command may be used to read the entire memory. After issuing the command, the master must provide the 2-byte target address. After the two bytes, the master reads data beginning from the target address and may continue until the end of memory, at which point logic 1s will be read. It is important to realize that the target address registers will contain the address provided. The ending offset/data status byte is unaffected.

The hardware of the DS2423 provides a means to accomplish error-free writing to the memory section. To safeguard reading data in the 1-Wire environment and to simultaneously speed up data transfers, it is recommended to packetize data into data packets of the size of one memory page each. Such a packet would typically store a 16-bit CRC with each page of data to ensure rapid, error-free data transfers that eliminate having to read a page multiple times to determine if the received data is correct or not. (See the *Book of DS19xx iButton Standards*, Chapter 7 for the recommended file structure.)

## Read Memory + Counter [A5H]

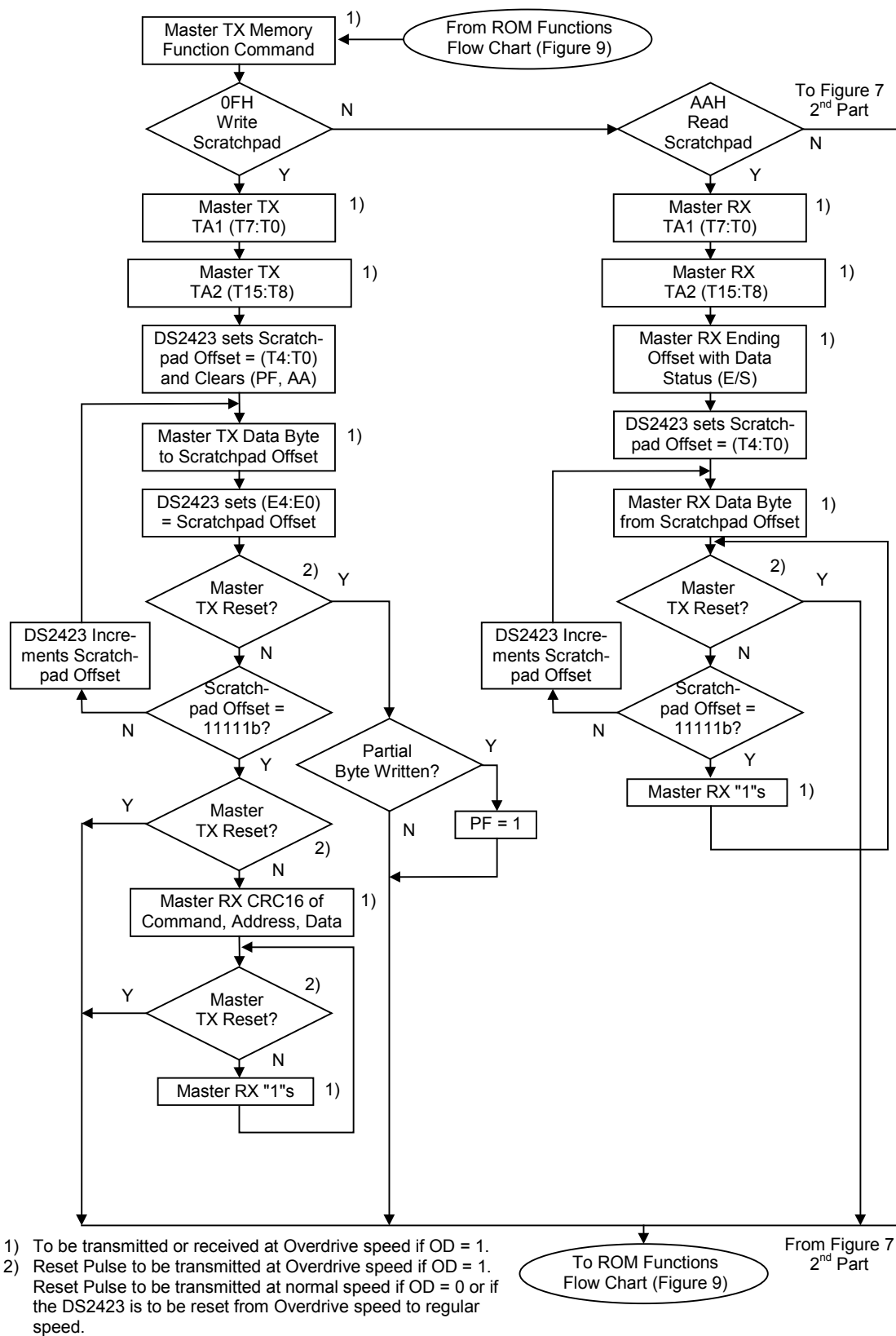
The Read Memory + Counter command is used to read memory data together with the write cycle counter or externally triggered counter associated with the addressed page of data memory. The additional information is transmitted by the DS2423 as the end of a memory page is encountered. Following the current value of the counter the DS2423 transmits 32 0-bits and a 16-bit CRC generated by the DS2423.

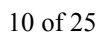
After having sent the command code of the Read Memory + Counter command, the bus master sends a two-byte address (TA1 = (T7:T0), TA2 = (T15:T8)) that indicates a starting byte location within the data field. With the subsequent read data time slots the master receives data from the DS2423 starting at the initial address and continuing until the end of a 32-byte page is reached. At that point the bus master will send 80 additional read data time slots and receive the contents of the 32-bit counter associated with the addressed page, 32 0-bits and a 16-bit CRC. With subsequent read data time slots the master will receive data starting at the beginning of the next page followed by the contents of the counter associated with the page, 0-bits and CRC for that page. This sequence will continue until the final page and its accompanying data is read by the bus master. When applying the Read Memory + Counter command to a page that does not have a counter associated, the master will read FFFFFFFFH instead of a valid count.

With the initial pass through the Read Memory + Counter flow chart the 16-bit CRC value is the result of shifting the command byte into the cleared CRC generator, followed by the two address bytes, the contents of the data memory, the counter and the 0-bits. Subsequent passes through the Read Memory + Counter flow chart will generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the contents of the data memory page, its associated counter and 0-bits. After the 16-bit CRC of the last page is read, the bus master will receive logical 1s from the DS2423 until a Reset Pulse is issued. The Read Memory + Counter command sequence can be ended at any point by issuing a Reset Pulse.

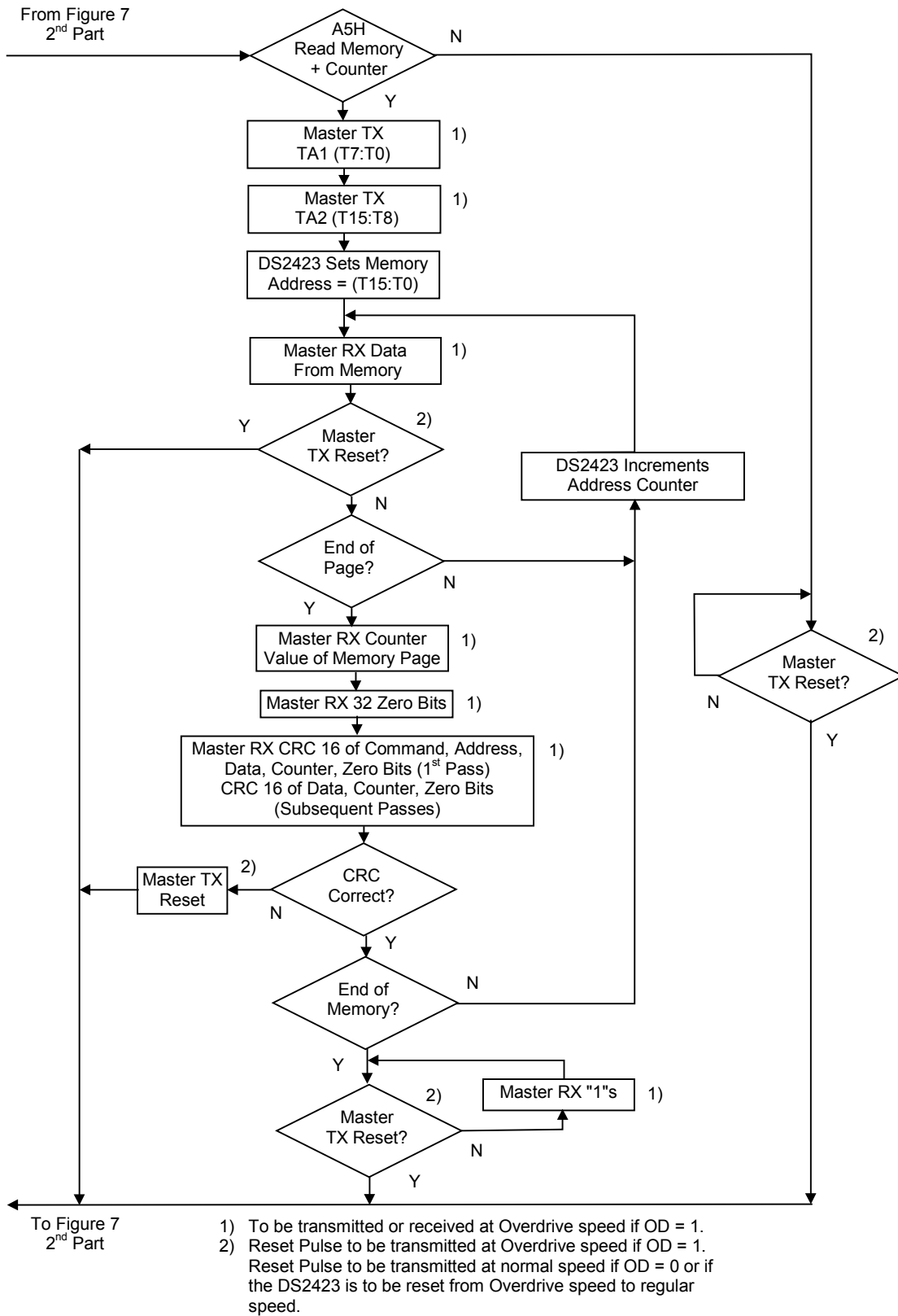


### MEMORY FUNCTION FLOW CHART Figure 7





# MEMORY FUNCTION FLOW CHART Figure 7 cont'd



## MEMORY FUNCTION EXAMPLE

Example: Write two data bytes to memory location 0026 and 0027. Read entire memory.

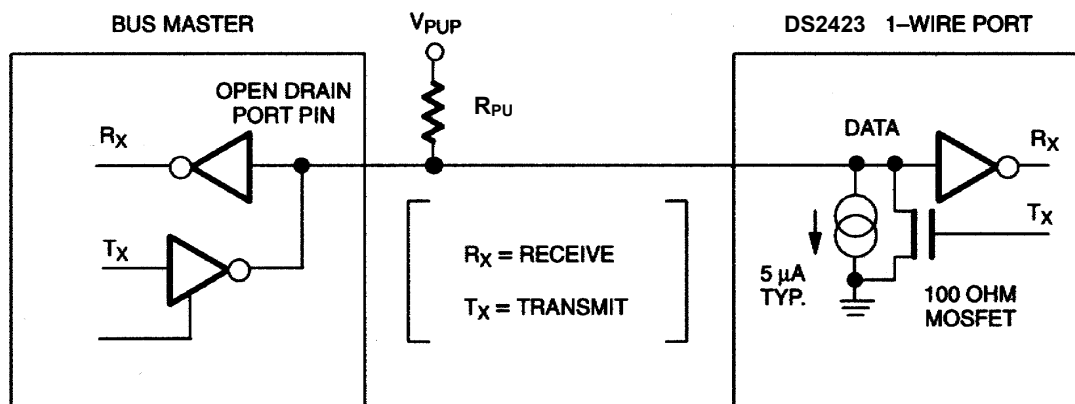
MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480-960 $\mu$ s)
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	0Fh	Issue “write scratchpad” command
TX	26h	TA1, beginning offset=26h
TX	00h	TA2, address=0026h
TX	<2 data bytes>	Write 2 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	AAh	Issue “read scratchpad” command
RX	26h	Read TA1, beginning offset=26h
RX	00h	Read TA2, address=0026h
RX	07h	Read E/S, ending offset=7h, flags=0h
RX	<2 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	5Ah	Issue “copy scratchpad” command
TX	26h	TA1 } TA2 } AUTHORIZATION CODE E/S }
TX	00h	
TX	07h	
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	F0h	Issue “read memory” command
TX	00h	TA1, beginning offset=0
TX	00h	TA2, address=0000h
RX	<512 bytes>	Read entire memory
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

## MEMORY FUNCTION EXAMPLE

Read page 14 and counts of Input A. Rewrite page 14 with 32 bytes. Read Memory + Counter, Write Scratchpad, Copy Scratchpad.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480-960 $\mu$ s)
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	A5h	Issue “read memory + counter” command
TX	C0h	TA1, beginning offset=C0h
TX	01h	TA2, address=01C0h
RX	<32 data bytes>	Read 32 bytes of data
RX	<4 data bytes>	Read Counts of Input A
RX	<4 data bytes>	Read 32 Zero Bits
RX	<2 data bytes>	Read (inverted) CRC16
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	0Fh	Issue “write scratchpad” command
TX	C0h	TA1, beginning offset=C0h
TX	01h	TA2, address=01C0h
TX	<32 data bytes>	Read 32 bytes of data to scratchpad
RX	<2 data bytes>	Read (inverted) CRC16
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	5Ah	Issue “copy scratchpad” command
TX	C0h	TA1 } TA2 } AUTHORIZATION CODE E/S }
TX	01h	
TX	1Fh	
RX	<1 data byte>	Read Copy Scratchpad response
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

## HARDWARE CONFIGURATION Figure 8



Note: Depending on the 1-Wire communication speed and the bus load characteristics, the optimal pull-up resistor ( $R_{PU}$ ) value will be in the  $1.5k\Omega$  to  $5k\Omega$  range.

### 1-WIRE BUS SYSTEM

The 1-Wire bus is a system which has a single bus master and one or more slaves. In all instances the DS2423 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). A 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the *Book of DS19xx iButton Standards*.

### HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or 3-state outputs. The 1-Wire port of the DS2423 is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. At regular speed the 1-Wire bus has a maximum data rate of 16.3kbits per second. The speed can be boosted to 142kbits per second by activating the Overdrive mode. The 1-Wire bus requires a pullup resistor of approximately  $5k\Omega$ . The 1-Wire bus requires a pullup resistor range of  $1.5k\Omega$  to  $5k\Omega$ , depending on the bus load characteristics.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus **MUST** be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than  $16\mu s$  (Overdrive speed) or more than  $120\mu s$  (regular speed), one or more devices on the bus may be reset.

### TRANSACTION SEQUENCE

The protocol for accessing the DS2423 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

## INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a Reset Pulse transmitted by the bus master followed by Presence Pulse(s) transmitted by the slave(s).

The Presence Pulse lets the bus master know that the DS2423 is on the bus and is ready to operate. For more details, see the 1-Wire Signaling section.

## ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the six ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (refer to flowchart in Figure 9):

### Read ROM [33H]

This command allows the bus master to read the DS2423's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS2423 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The resultant family code and 48-bit serial number will result in a mismatch of the CRC.

### Match ROM [55H]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS2423 on a multidrop bus. Only the DS2423 that exactly matches the 64-bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a Reset Pulse. This command can be used with a single or multiple devices on the bus.

### Skip ROM [CCH]

This command can save time in a single-drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired-AND result).

### Search ROM [F0H]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The search ROM process is the repetition of a simple, three-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, three-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the *Book of DS19xx 1-Wire Standards* for a comprehensive discussion of a search ROM, including an actual example.

### Overdrive Skip ROM [3CH]

On a single-drop bus this command can save time by allowing the bus master to access the memory functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command the Overdrive Skip ROM sets the DS2423 in the Overdrive mode (OD = 1). All communication following this command has to occur at Overdrive speed until a Reset Pulse of minimum 480μs duration resets all devices on the bus to regular speed (OD = 0).

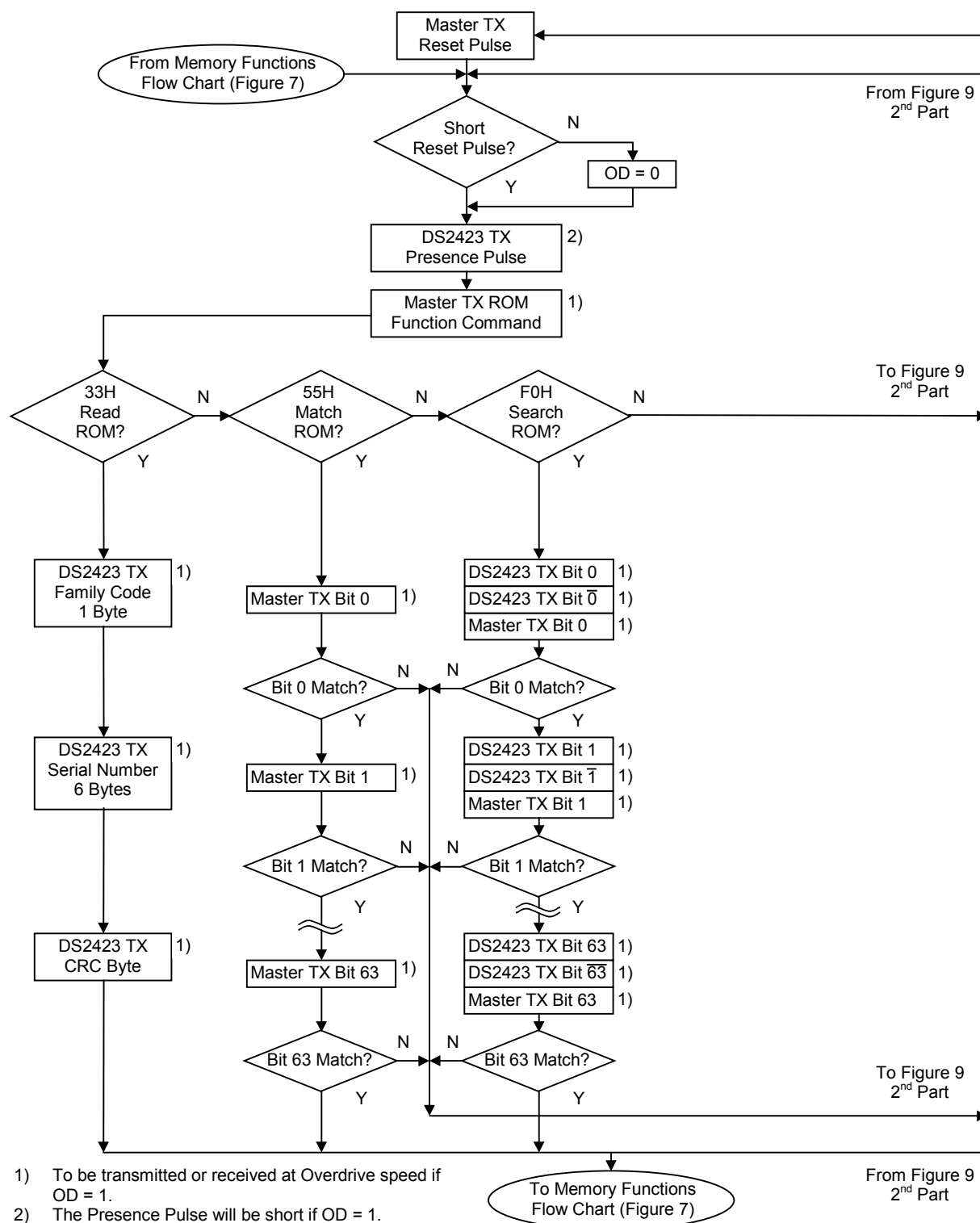
When issued on a multidrop bus this command will set all Overdrive-supporting devices into Overdrive mode. To subsequently address a specific Overdrive-supporting device, a Reset Pulse at Overdrive speed has to be issued followed by a Match ROM or Search ROM command sequence. This will speed up the time for the search process. If more than one slave supporting Overdrive is present on the bus and the Overdrive Skip ROM command is followed by a read command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired-AND result).

### **Overdrive Match ROM [69H]**

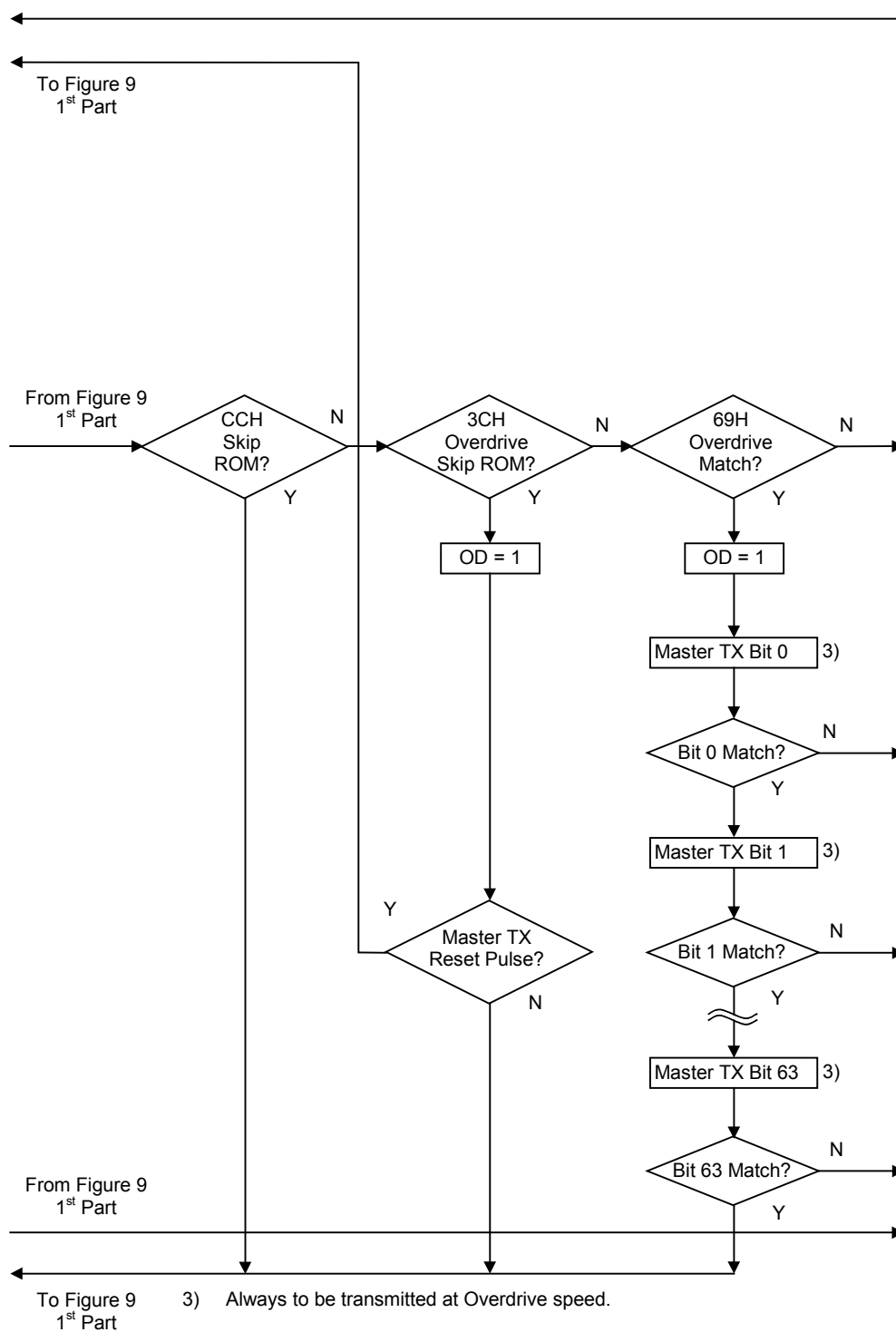
The Overdrive Match ROM command, followed by a 64-bit ROM sequence transmitted at Overdrive speed, allows the bus master to address a specific DS2423 on a multidrop bus and to simultaneously set it in Overdrive mode. Only the DS2423 that exactly matches the 64-bit ROM sequence will respond to the subsequent memory function command. Slaves already in Overdrive mode from a previous Overdrive Skip or Match command will remain in Overdrive mode. All other slaves that do not match the 64-bit ROM sequence or do not support Overdrive will return to or remain at regular speed and wait for a Reset Pulse of minimum 480  $\mu$ s duration. The Overdrive Match ROM command can be used with a single or multiple devices on the bus.



# ROM FUNCTIONS FLOW CHART Figure 9 (First Part)



# ROM FUNCTIONS FLOW CHART Figure 9 cont'd



## 1-WIRE SIGNALING

The DS2423 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1 and Read Data. The bus master initiates all these signals except Presence Pulse. The DS2423 can communicate at two different speeds, regular speed and Overdrive speed. If not explicitly set into the Overdrive mode, the DS2423 will communicate at regular speed. While in Overdrive mode the fast timing applies to all waveforms.

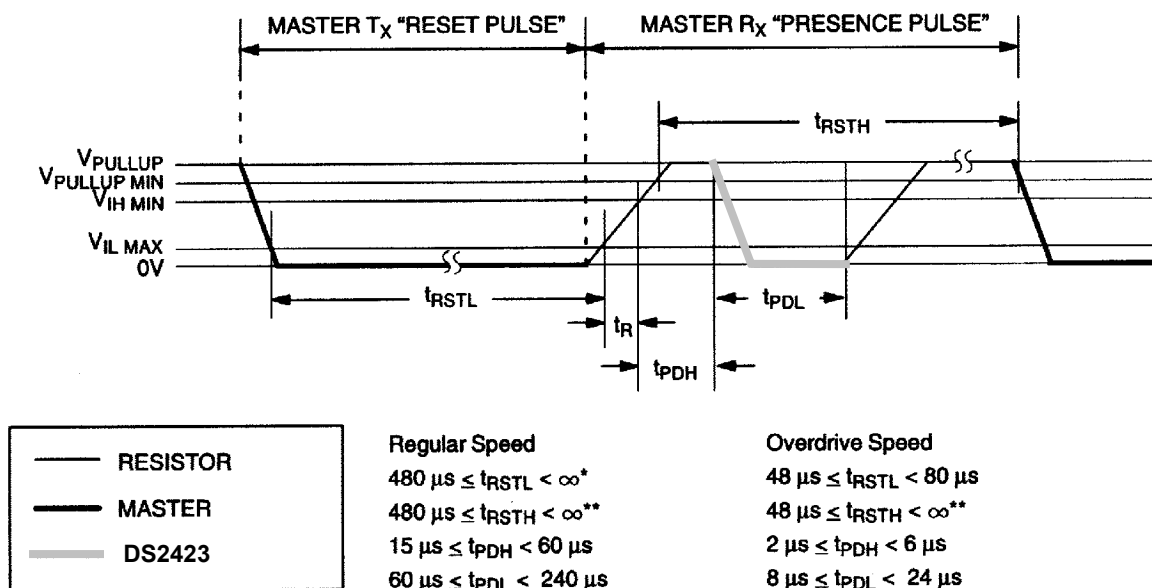
The initialization sequence required to begin any communication with the DS2423 is shown in Figure 10. A Reset Pulse followed by a Presence Pulse indicates the DS2423 is ready to send or receive data given the correct ROM command and memory function command. The bus master transmits (TX) a Reset Pulse ( $t_{RSTL}$ , minimum 480  $\mu$ s at regular speed, 48  $\mu$ s at Overdrive speed). The bus master then releases the line and goes into receive mode (RX). The 1-Wire bus is pulled to a high state via the pullup resistor. After detecting the rising edge on the data pin, the DS2423 waits ( $t_{PDH}$ , 15-60 $\mu$ s at regular speed, 2-6 $\mu$ s at Overdrive speed) and then transmits the Presence Pulse ( $t_{PDL}$ , 60-240 $\mu$ s at regular speed, 8-24 $\mu$ s at Overdrive speed).

A Reset Pulse of 480 $\mu$ s or longer will exit the Overdrive mode returning the device to regular speed. If the DS2423 is in Overdrive mode and the Reset Pulse is no longer than 80 $\mu$ s the device will remain in Overdrive mode.

### Read/Write Time Slots

The definitions of write and read time slots are illustrated in Figure 11. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS2423 to the master by triggering a delay circuit in the DS2423. During write time slots, the delay circuit determines when the DS2423 will sample the data line. For a read data time slot, if a “0” is to be transmitted, the delay circuit determines how long the DS2423 will hold the data line low overriding the 1 generated by the master. If the data bit is a “1”, the device will leave the read data time slot unchanged.

### INITIALIZATION PROCEDURE “RESET AND PRESENCE PULSES” Figure 10

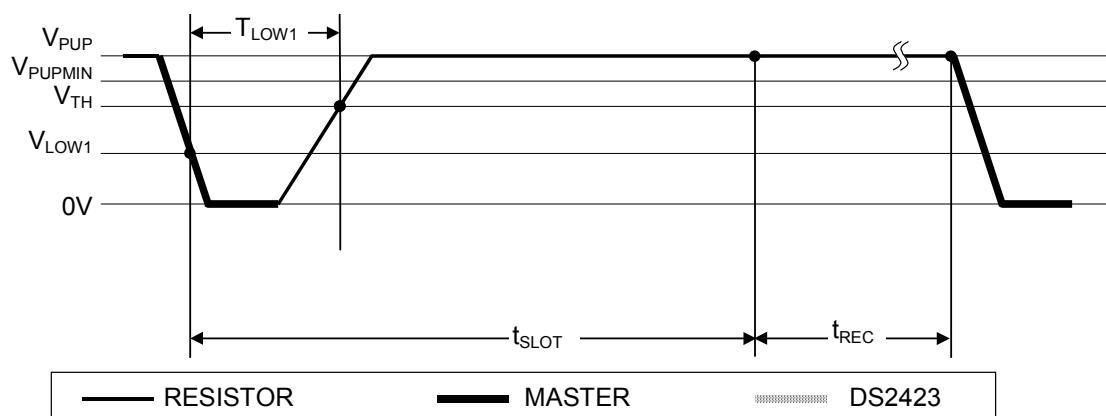


\*IN ORDER NOT TO MASK INTERRUPT SIGNALING BY OTHER DEVICES ON THE 1-WIRE BUS,  $t_{RSTL} + t_R$  SHOULD ALWAYS BE LESS THAN 960  $\mu$ s

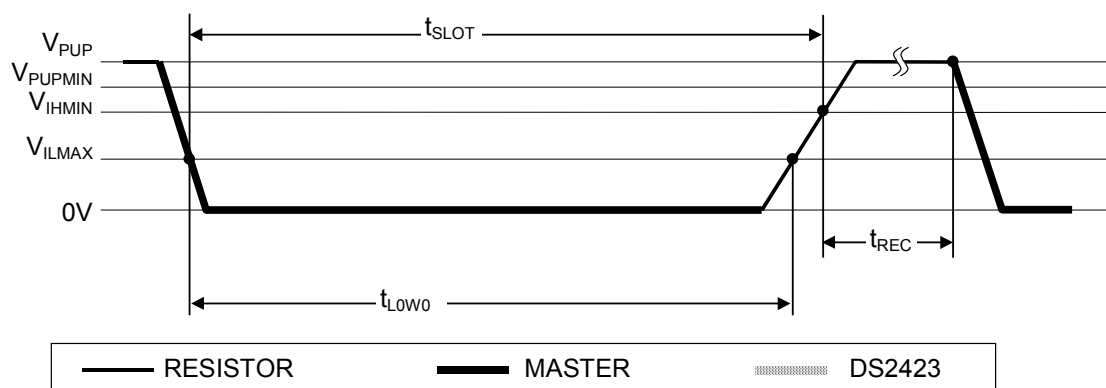
\*\*INCLUDES RECOVERY TIME

# **READ/WRITE TIMING DIAGRAM Figure 11**

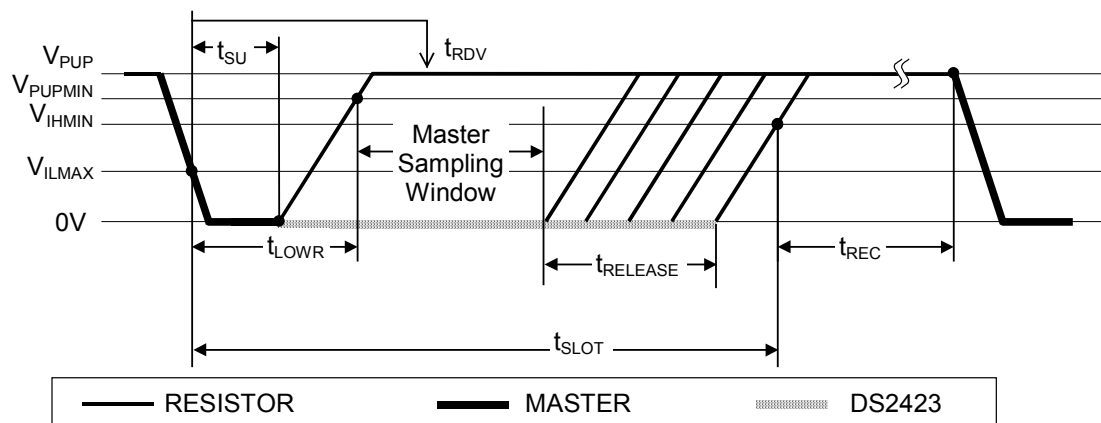
## **Write-One Time Slot**



## **Write-Zero Time Slot**



## Read-Data Time Slot



## CRC GENERATION

With the DS2423 there are two different types of CRCs (Cyclic Redundancy Checks). One CRC is an 8-bit type and is stored in the most significant byte of the 64-bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM and compare it to the value stored within the DS2423 to determine if the ROM data has been received error-free by the bus master. The equivalent polynomial function of this CRC is:  $X^8 + X^5 + X^4 + 1$ . This 8-bit CRC is received in the true (non-inverted) form when reading the ROM of the DS2423. It is computed at the factory and lasered into the ROM.

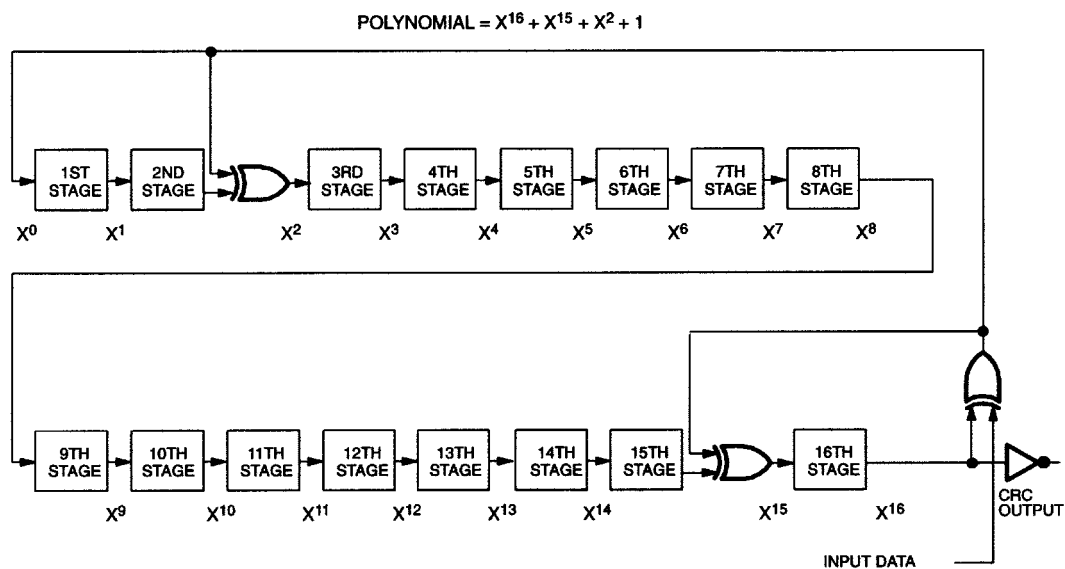
The other CRC is a 16-bit type, generated according to the standardized CRC16-polynomial function  $x^{16} + x^{15} + x^2 + 1$ . This CRC is used for error detection when reading Data Memory using the Read Memory + Counter command and for fast verification of a data transfer when writing to the scratchpad. It is the same type of CRC as is used with NV RAM based iButtons for error detection within the iButton Extended File Structure. In contrast to the 8-bit CRC, the 16-bit CRC is always returned or sent in the complemented (inverted) form. A CRC-generator inside the DS2423 chip (Figure 12) will calculate a new 16-bit CRC as shown in the command flow chart of Figure 7. The bus master compares the CRC value read from the device to the one it calculates from the data and decides whether to continue with an operation or re-read the portion of the data with the CRC error.

With the initial pass through the Read Memory + Counter flow chart the 16-bit CRC value is the result of shifting the command byte into the cleared CRC generator, followed by the two address bytes, data bytes, value of the counter associated with the page and zero bits. Subsequent passes through the Read Memory + Counter flow chart will generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the data bytes, the value of the counter and the zero bits.

With the Write Scratchpad command the CRC is generated by first clearing the CRC generator and then shifting in the command code, the Target Addresses TA1 and TA2 and all the data bytes. The DS2423 will transmit this CRC only if the data bytes written to the scratchpad include scratchpad ending offset 11111b. The data may start at any location within the scratchpad.

For more details on generating CRC values including example implementations in both hardware and software, see the *Book of DS19xx iButton Standards*.

# CRC-16 HARDWARE DESCRIPTION AND POLYNOMIAL Figure 12



**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See J-STD-020A Specifications

- \* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**DC CHARACTERISTICS** ( $V_{PUP} = 2.8V$  to  $6.0V$ ;  $V_{BAT} = 2.8$  to  $5.5V$ ; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	$V_{IH}$	2.2			V	1, 8
Logic 0	$V_{IL}$	-0.3		+0.8	V	1, 9
Output Logic Low @ 4 mA	$V_{OL}$			0.4	V	1
Output Logic High	$V_{OH}$		$V_{PUP}$	6.0	V	1, 2
Input Load Current	$I_L$		5		$\mu A$	3
Standby Current	$I_{BATS}$			200	nA	
I/O Operate Charge	$Q_{BATO}$			200	nC	12, 16

**CAPACITANCE**( $t_A = 25^\circ C$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
I/O (1-Wire)	$C_{IN/OUT}$		100	800	pF	6, 16

**COUNTER INPUT CHARACTERISTICS**( $V_{PUP} = 2.8V$  to  $6.0V$ ;  $V_{BAT} = 2.8$  to  $5.5V$ ; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Trip Point	$V_{TRIP}$		$\frac{1}{2} V_{BAT}$		V	
Logic 1	$V_{INH}$	$V_{TRIP}$		$V_{BAT} + 0.3$	V	1, 10
Logic 0	$V_{INL}$	-0.3		$V_{TRIP}$	V	1
Internal Pullup Resistor	$R_{PI}$		28		$M\Omega$	11, 16
Debounce Time	$T_{DEB}$	170	290	460	$\mu s$	13
Pulse Width (Active Low)	$T_{PW}$	1			$\mu s$	16

**AC CHARACTERISTICS REGULAR SPEED**(V<sub>PUP</sub> = 2.8V to 6.0V; V<sub>BAT</sub> = 2.8 to 5.5V; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t <sub>SLOT</sub>	60		120	μs	
Write 1 Low Time	t <sub>LOW1</sub>	1		15	μs	15
Write 0 Low Time	t <sub>LOW0</sub>	60		120	μs	
Read Low Time	t <sub>LOWR</sub>	1		15	μs	15
Read Data Valid	t <sub>RDV</sub>		15		μs	14, 16
Release Time	t <sub>RELEASE</sub>	0	15	45	μs	
Read Data Setup	t <sub>SU</sub>			1	μs	5
Recovery Time	t <sub>REC</sub>	1			μs	
Reset Time High	t <sub>RSTH</sub>	480			μs	4
Reset Time Low	t <sub>RSTL</sub>	480		960	μs	7
Presence Detect High	t <sub>PDH</sub>	15		60	μs	
Presence Detect Low	t <sub>PDL</sub>	60		240	μs	

**AC CHARACTERISTICS OVERDRIVE SPEED**(V<sub>PUP</sub> = 2.8V to 6.0V; V<sub>BAT</sub> = 2.8 to 5.5V; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t <sub>SLOT</sub>	6		16	μs	
Write 1 Low Time	t <sub>LOW1</sub>	1		2	μs	15
Write 0 Low Time	t <sub>LOW0</sub>	6		16	μs	
Read Low Time	t <sub>LOWR</sub>	1		2	μs	15
Read Data Valid	t <sub>RDV</sub>		2		μs	14, 16
Release Time	t <sub>RELEASE</sub>	0	1.5	4	μs	
Read Data Setup	t <sub>SU</sub>			1	μs	5
Recovery Time	t <sub>REC</sub>	1			μs	
Reset Time High	t <sub>RSTH</sub>	48			μs	4
Reset Time Low	t <sub>RSTL</sub>	48		80	μs	
Presence Detect High	t <sub>PDH</sub>	2		6	μs	
Presence Detect Low	t <sub>PDL</sub>	8		24	μs	



**NOTES:**

- 1) All voltages are referenced to ground.
- 2)  $V_{PUP}$  = external pullup voltage.
- 3) Input load is to ground.
- 4) An additional reset or communication sequence cannot begin until the reset high time has expired.
- 5) Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within  $1\mu s$  of this falling edge.
- 6) Capacitance on the data pin could be 800pF when power is first applied. If a  $5k\Omega$  resistor is used to pull up the data line to  $V_{PUP}$ ,  $5\mu s$  after power has been applied the parasite capacitance will not affect normal communications.
- 7) The reset low time ( $t_{RSTL}$ ) should be restricted to a maximum of  $960\mu s$ , to allow interrupt signaling, otherwise, it could mask or conceal interrupt pulses.
- 8)  $V_{IH}$  is a function of the external pullup resistor and  $V_{PUP}$ .
- 9) Under certain low voltage conditions  $V_{ILMAX}$  may have to be reduced to as much as 0.5V to always guarantee a Presence Pulse.
- 10) The counter inputs are designed for interfacing to mechanical switches and piezo sensors. If interfacing to digital circuits, one should use an open drain driver.
- 11) A lower impedance pullup, e. g., for reed switches, can be achieved by connecting an external resistor from the counter input to  $V_{BAT}$ .
- 12) Read and write scratchpad (all 32 bytes) at  $V_{BAT}$  of 3.0 V.
- 13) Each low-going edge on a counter input resets the channel's debounce timer. The debounce time starts as the input voltage rises beyond the trip point. In order for the next pulse to be counted the debounce time must have expired.
- 14) The optimal sampling point for the master is as close as possible to the end time of the  $t_{RDV}$  period without exceeding  $t_{RDV}$ . For the case of a Read-One Time slot, this maximizes the amount of time for the pullup resistor to recover to a high level. For a Read-Zero Time slot, it ensures that a read will occur before the fastest 1-Wire device(s) releases the line.
- 15) The duration of the low pulse sent by the master should be a minimum of  $1\mu s$  with a maximum value as short as possible to allow time for the pullup resistor to recover the line to a high level before the 1-Wire device samples in the case of a Write-One Time or before the master samples in the case of a Read-One Time.
- 16) Guaranteed by design; not production tested.