

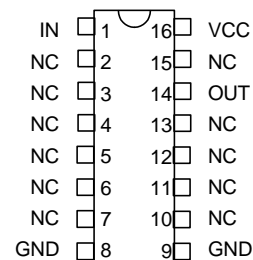
MECHANICALLY VARIABLE TTL DELAY LINE (SERIES DDU39F)



FEATURES

- Ideal for "Set and Forget" applications
- Multi-turn adjustment screw (approx. 15 turns)
- Fits standard 16-pin DIP socket
- Input & output fully TTL interfaced & buffered
(10 T²L fan-out capability)
- **Resolution:** 0.5ns typical
- **Adjustment range:** 7ns to 25ns
- **Output rise time:** 4ns typical
- **Min. input pulse width:** 10ns
- **Power dissipation:** 230mW maximum
- **Operating temperature:** 0° to 70°C (Commercial)
-55° to 125°C (Military)

PACKAGES



DDU39F (Commercial)
DDU39FM (Military)

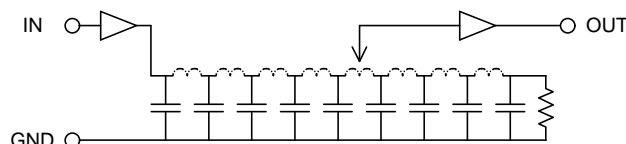
FUNCTIONAL DESCRIPTION

The DDU39F-series device is a mechanically variable, FAST-TTL interfaced delay line. The signal input (IN) is reproduced at the tap output (OUT), shifted by an amount which can be adjusted between 7ns and 25ns. The device operates from a single 5V supply and is TTL interfaced, capable of driving up to 10 TTL loads.

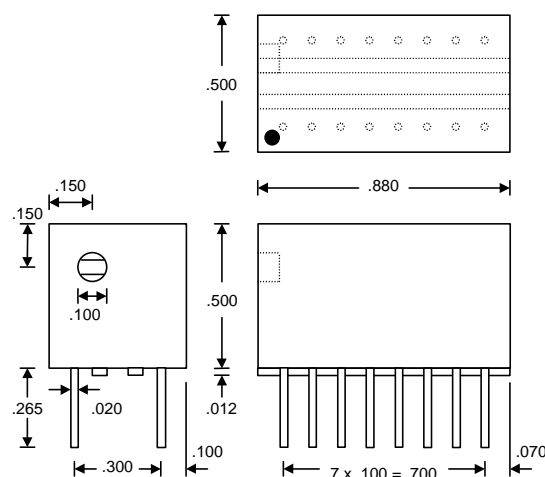
PIN DESCRIPTIONS

IN Signal Input
OUT Fixed Output
VCC +5V
GND Ground
NC No connection

SERIES SPECIFICATIONS



Functional Diagram



Package Dimensions

APPLICATION NOTES

HIGH FREQUENCY RESPONSE

The DDU39F tolerances are guaranteed for input pulse widths and periods greater than those specified in the test conditions. Although the device will function properly for pulse widths as small as 10ns and periods as small 20ns (for a symmetric input), the delays may deviate from their values at low frequency. However, for a given input condition, the deviation will be repeatable from pulse to pulse. Contact technical support at Data Delay Devices if your application

requires device testing at a specific input condition.

POWER SUPPLY BYPASSING

The DDU39F relies on a stable power supply to produce repeatable delays within the stated tolerances. A 0.1uf capacitor from VCC to GND, located as close as possible to the VCC pin, is recommended. A wide VCC trace and a clean ground plane should be used.

DEVICE SPECIFICATIONS

TABLE 1: ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
|---------------------|-------------------|------|----------------------|-------|--------|
| DC Supply Voltage | V _{CC} | -0.3 | 7.0 | V | |
| Input Pin Voltage | V _{IN} | -0.3 | V _{DD} +0.3 | V | |
| Storage Temperature | T _{STRG} | -55 | 150 | C | |
| Lead Temperature | T _{LEAD} | | 300 | C | 10 sec |

TABLE 2: DC ELECTRICAL CHARACTERISTICS

(0C to 70C, 4.75V to 5.25V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|--|------------------|-----|------|------|-------|--|
| High Level Output Voltage | V _{OH} | 2.5 | 3.4 | | V | V _{CC} = MIN, I _{OH} = MAX V _{IH} = MIN, V _{IL} = MAX |
| Low Level Output Voltage | V _{OL} | | 0.35 | 0.5 | V | V _{CC} = MIN, I _{OL} = MAX V _{IH} = MIN, V _{IL} = MAX |
| High Level Output Current | I _{OH} | | | -1.0 | mA | |
| Low Level Output Current | I _{OL} | | | 20.0 | mA | |
| High Level Input Voltage | V _{IH} | 2.0 | | | V | |
| Low Level Input Voltage | V _{IL} | | | 0.8 | V | |
| Input Clamp Voltage | V _{IK} | | | -1.2 | V | V _{CC} = MIN, I _I = I _{IK} |
| Input Current at Maximum Input Voltage | I _{IHH} | | | 0.1 | mA | V _{CC} = MAX, V _I = 7.0V |
| High Level Input Current | I _{IH} | | | 20 | μA | V _{CC} = MAX, V _I = 2.7V |
| Low Level Input Current | I _{IL} | | | -0.6 | mA | V _{CC} = MAX, V _I = 0.5V |
| Short-circuit Output Current | I _{OS} | -60 | | -150 | mA | V _{CC} = MAX |
| Output High Fan-out | | | | 25 | Unit | |
| Output Low Fan-out | | | | 12.5 | Load | |

DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

INPUT:

Ambient Temperature: $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$

Supply Voltage (V_{CC}): $5.0\text{V} \pm 0.1\text{V}$

Input Pulse: High = $3.0\text{V} \pm 0.1\text{V}$
Low = $0.0\text{V} \pm 0.1\text{V}$

Source Impedance: 50Ω Max.

Rise/Fall Time: 3.0 ns Max. (measured
between 0.6V and 2.4V)

Pulse Width: 100ns

Period: 1000ns

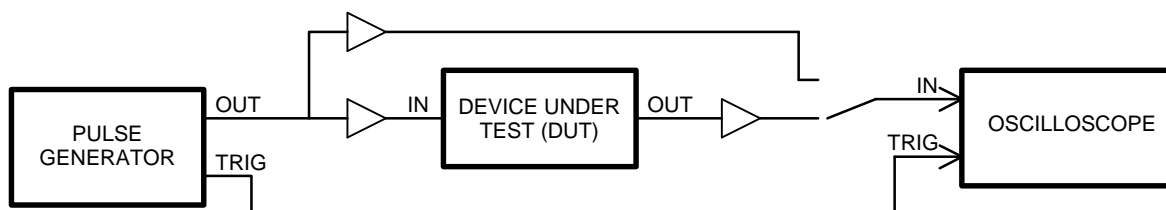
OUTPUT:

Load: 1 FAST-TTL Gate

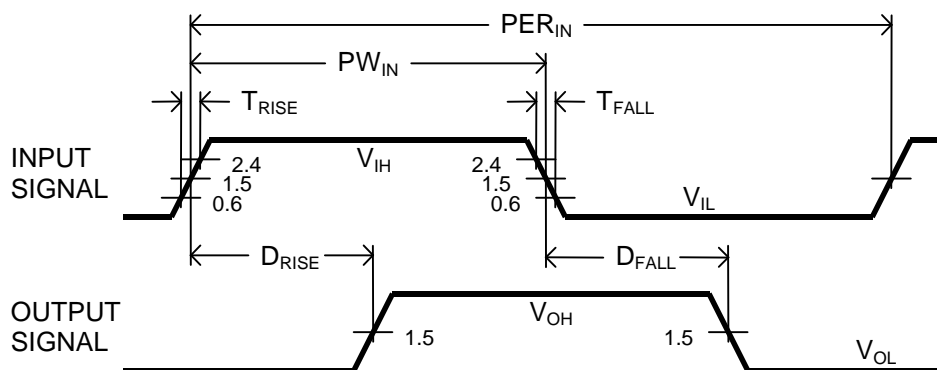
C_{load} : $5\text{pf} \pm 10\%$

Threshold: 1.5V (Rising & Falling)

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Test Setup



Timing Diagram For Testing