

élantec
 HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2223/EL2223C

Dual, 500 MHz High Speed, Operational Amplifier

ELANTEC INC

T-79-07-20

EL2223/EL2223C

Features

- Wide gain bandwidth—500 MHz
- High slew rate—350 V/ μ s
- High power bandwidth ($\pm 10 V_{out}$) 5.5 MHz
- Large open loop gain 83 dB
- Low power—5 mA/amplifier
- Low input offset—0.5 mV typ.
- Wide supply voltage range $V_s = \pm 5V$ to $\pm 15V$
- Output short circuit protected

Applications

- High performance active filters
- Video and pulse amplifiers
- Local area networks
- Wideband amplifiers
- Replace two HA2540s

Ordering Information

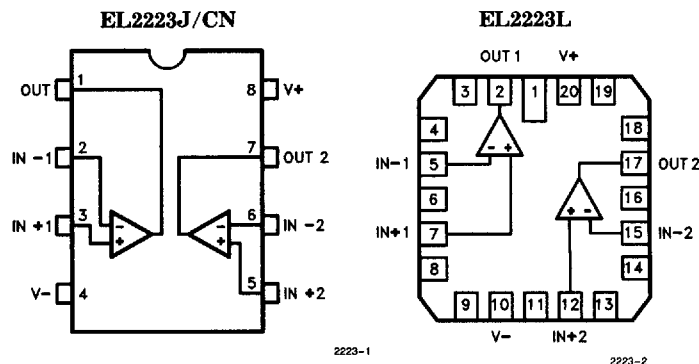
Part No.	Temp. Range	Package	Outline #
EL2223CJ	0°C to +75°C	CerDIP	MDP0010
EL2223CN	0°C to +75°C	P-DIP	MDP0031
EL2223J	-55°C to +125°C	CerDIP	MDP0010
EL2223J/883B	-55°C to +125°C	CerDIP	MDP0010
EL2223L/883B	-55°C to +125°C	LCC	MDP0007
EL2223CM	0°C to +75°C	SOL	MDP0027

General Description

The EL2223 monolithic dual operational amplifier is an extension of Elantec's position in high speed analog products. This patented amplifier features 350 V/ μ s slew rate, a 500 MHz gain bandwidth gain-of-10 stable, along with an excellent speed power relationship. The dual 500 MHz EL2223 consumes only 10 mA, making it ideal for HA2540 type applications. The EL2223 has short-circuit-protected outputs and will operate from $\pm 5V$ to $\pm 15V$. It is fabricated using Elantec's complementary bipolar process which allows both fast PNP and NPN transistors to be manufactured on a single chip.

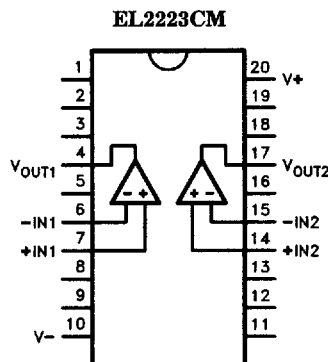
Elantec's products and facilities comply with MIL-STD-883 Revision C, MIL-I-45208A, and other applicable quality specifications. For information on Elantec's military processing, see Elantec document, QRA-2: "Elantec's Military Processing, Monolithic Integrated Circuits".

Connection Diagrams



2223-1

2223-2



2223-3

This product covered under U.S. Patent No. 4,837,523

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July 1991 Rev B

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Dual, 500 MHz High Speed, Operational Amplifier**Absolute Maximum Ratings** ($T_A = 25^\circ\text{C}$)

Voltage between V+ and V-	35V	Storage Temperature Range	-65°C to +150°C
Differential Input Voltage	±6V	Maximum Junction Temperature	
Internal Power Dissipation	See Curves	CerDIP, LCC	175°C
Peak Output Current	Short Circuit Protected	Plastic DIP, SOL	150°C
Output Short Circuit Duration (Note 1)	Continuous	Lead Temperature	
Operational Temperature Range		DIP Package	300°C
EL2223	-55°C to +125°C	SOL Package	
EL2223C	0°C to +75°C	Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25^\circ\text{C}$ and QA sample tested at $T_A = 25^\circ\text{C}$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25^\circ\text{C}$ for information purposes only.

DC Electrical Characteristics $V_S = \pm 15\text{V}$; $R_L = 2\text{ k}\Omega$, unless otherwise specified

Parameter	Description	Temp	EL2223				EL2223C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	+25°C			5	I			5	I	mV
		Full		0.5	8	I		0.5	8	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		3		V		3		V	$\mu\text{V}/^\circ\text{C}$
I_B	Bias Current	+25°C			4	I			4	I	μA
		Full		1.5	6	I		1.5	6	III	μA
I_{OS}	Offset Current	+25°C			2	I			2	I	μA
		Full		0.2	3	I		0.2	3	III	μA
R_{IN}	Input Resistance	+25°C		6		V		6		V	k Ω
C_{IN}	Input Capacitance	+25°C		1		V		1		V	pF
V_{CM}	Common Mode Input Range	Full	±10	±12		I	±10	±12		II	V
e_{IN}	Input Noise Voltage ($f = 1\text{ kHz}$, $R_G = 0\Omega$)	+25°C		7		V		7		V	$\text{nV}/\sqrt{\text{Hz}}$
A_{VOL}	Large Signal Voltage Gain (Notes 2, 3)	+25°C	20k	40k		I	20k	40k		I	V/V
		Full	10k			I	10k			III	V/V

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Dual, 500 MHz High Speed, Operational Amplifier

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DC Electrical Characteristics $V_S = \pm 15V$; $R_L = 2\text{ k}\Omega$, unless otherwise specified — Contd.

Parameter	Description	Temp	EL2223				EL2223C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
CMRR	Common-Mode Rejection Ratio (Note 4)	Full	70	90		I	70	90		II	dB
V_O	Output Voltage Swing	Full	± 11	± 12.5		I	± 11	± 12.5		II	V
I_{SC}	Short Circuit Current	+25°C		± 50	± 70	I		± 50	± 70	I	mA
R_O	Output Resistance	+25°C		40		V		40		V	Ω
I_S	Supply Current	Full		9.5	13	I		9.5	13	II	mA
PSRR	Power Supply Rejection Ratio (Note 5)	Full	70	90		I	70	90		II	dB

AC Electrical Characteristics $V_S = \pm 15V$; $R_L = 2\text{ k}\Omega$, unless otherwise specified

Parameter	Description	Temp	EL2223				EL2223C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
f_u	Open Loop Unity Bandwidth (Note 6)	+25°C		500		V		500		V	MHz
FPBW	Full Power Bandwidth (Notes 2, 7)	+25°C	3.98	5.5		I	3.98	5.5		I	MHz
t_r	Rise Time (Note 8)	+25°C		7		V		7		V	ns
OS	Overshoot (Note 8)	+25°C		30		V		30		V	%
SR	Slew Rate (Note 8)	+25°C	250	350		I	250	350		I	V/ μ s
t_s	Settling Time (Notes 9, 10) 10V Step to 0.05%	+25°C		330		V		330		V	ns
Ch S_p	Channel Separation ($f = 10\text{ MHz}$)			70		V		70		V	dB

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.

Note 2: $V_O = \pm 10V$.Note 3: $R_L = 2\text{ k}\Omega$.Note 4: Two tests are performed. $V_{CM} = 0V$ to +10V and $V_{CM} = 0V$ to -10V.Note 5: Two tests are performed. $V+ = 15V$, and $V-$ is changed from -5V to -15V. $V- = -15V$, and $V+$ is changed from +5V to +15V.Note 6: $V_O = 100\text{ mV}$.Note 7: Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \text{Slew Rate} / 2\pi V_{peak}$.

Note 8: Refer to Test Circuit section of data sheet.

Note 9: Settling time measurement are made with techniques in the following reference: "Take The Guesswork Out of Settling-Time Measurements," EDN September 19, 1985.

Note 10: $A_V = +10$, $R_L = 2\text{ k}\Omega$.

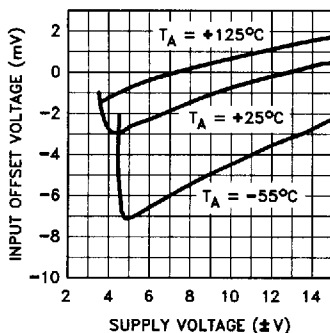
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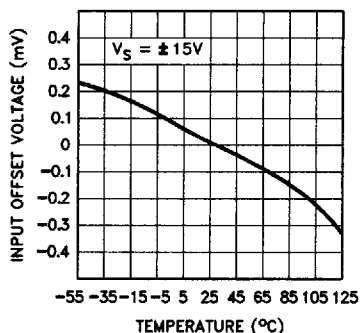
Dual, 500 MHz High Speed, Operational Amplifier

Typical Performance Curves

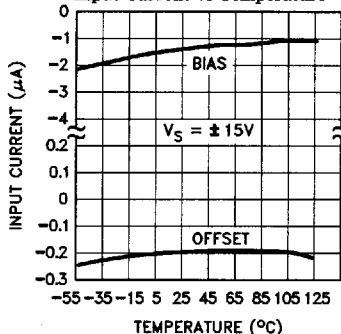
Input Offset Voltage vs Supply Voltage



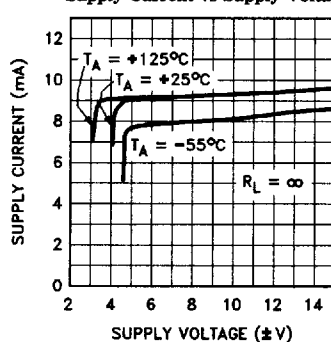
Normalized Input Offset Voltage vs Temperature



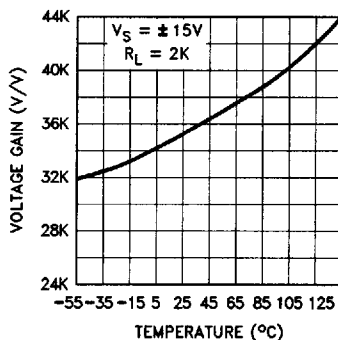
Input Current vs Temperature



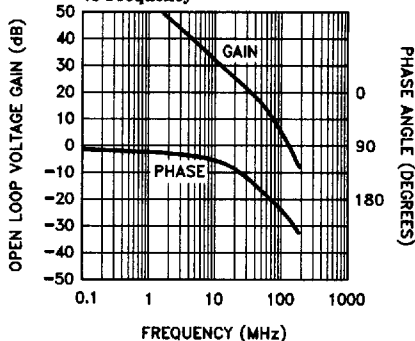
Supply Current vs Supply Voltage



Voltage Gain vs Temperature



Open Loop Voltage Gain vs Frequency



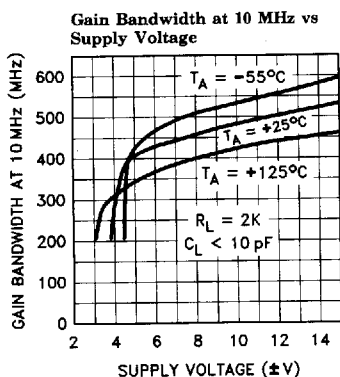
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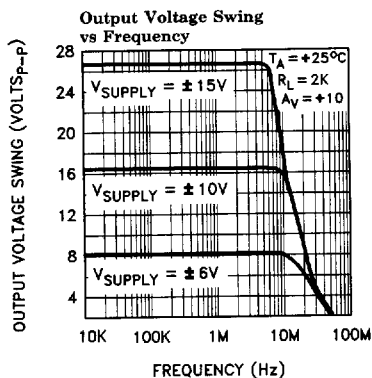
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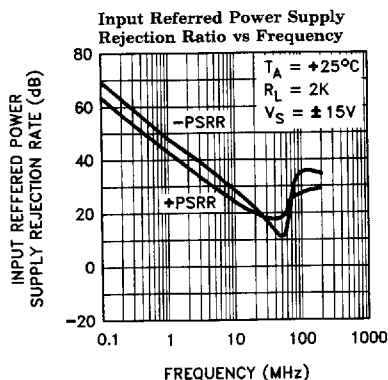
Typical Performance Curves — Contd.



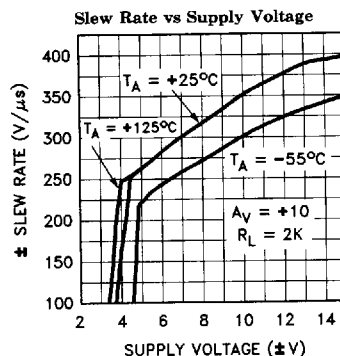
2223-10



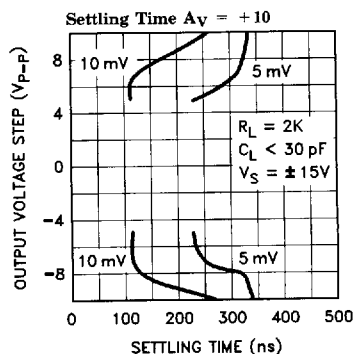
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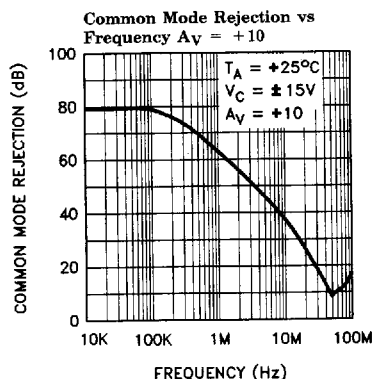
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2223-11



2223-13



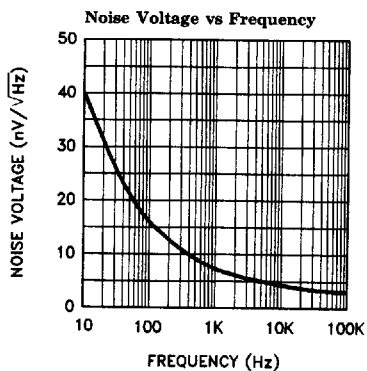
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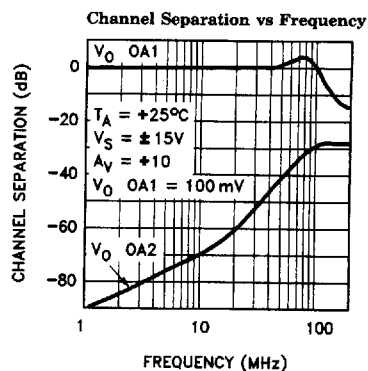
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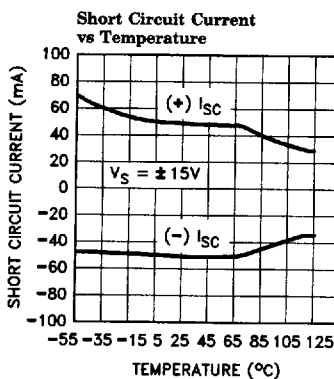
Typical Performance Curves — Contd.



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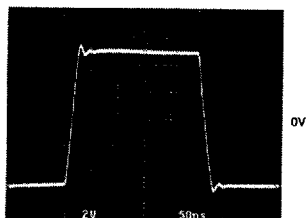


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2223-18

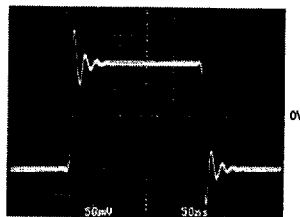
Large Signal Response



$A_V = +10$
 $V_{IN} = \pm 0.5\text{V}$
 $V_O = \pm 5\text{V}$
 $R_L = 2\text{k}$

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Small Signal Response



$A_V = +10$
 $V_{IN} = \pm 10\text{ mV}$
 $V_O = \pm 100\text{ mV}$
 $R_L = 2\text{k}$

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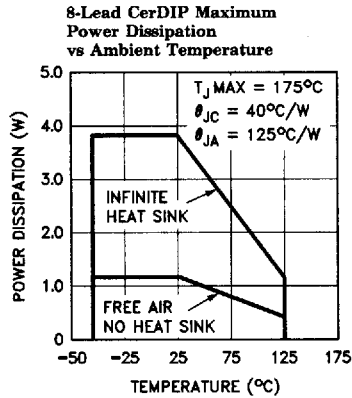
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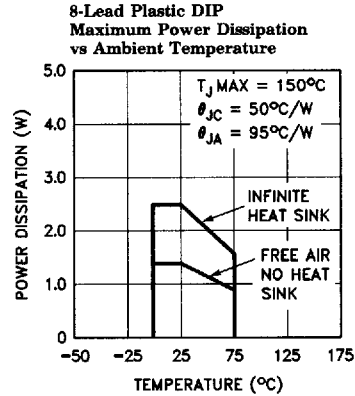
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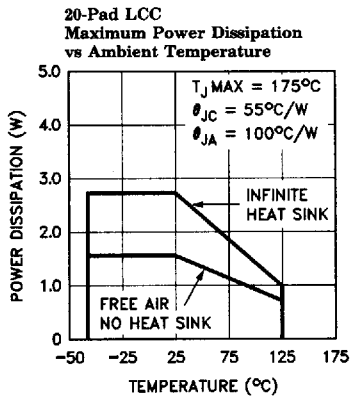
Typical Performance Curves — Contd.



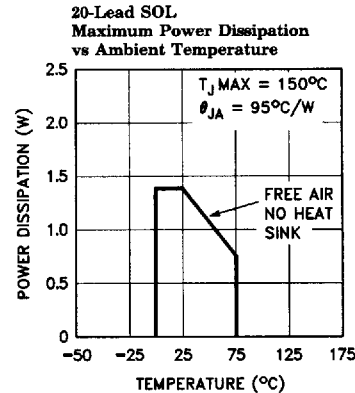
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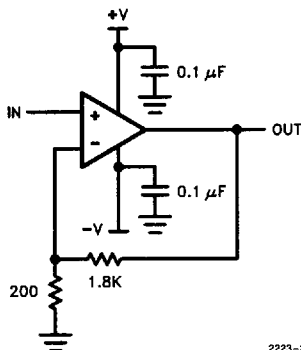


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2223-24

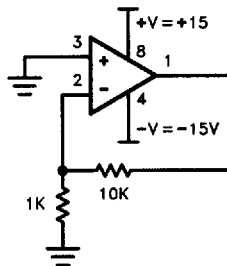
Test Circuit



2223-27

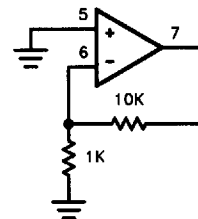
$A_V = +10$
 $C_L \leq 10 \text{ pF Scope Probe}$

Burn-In Circuit



2223-28

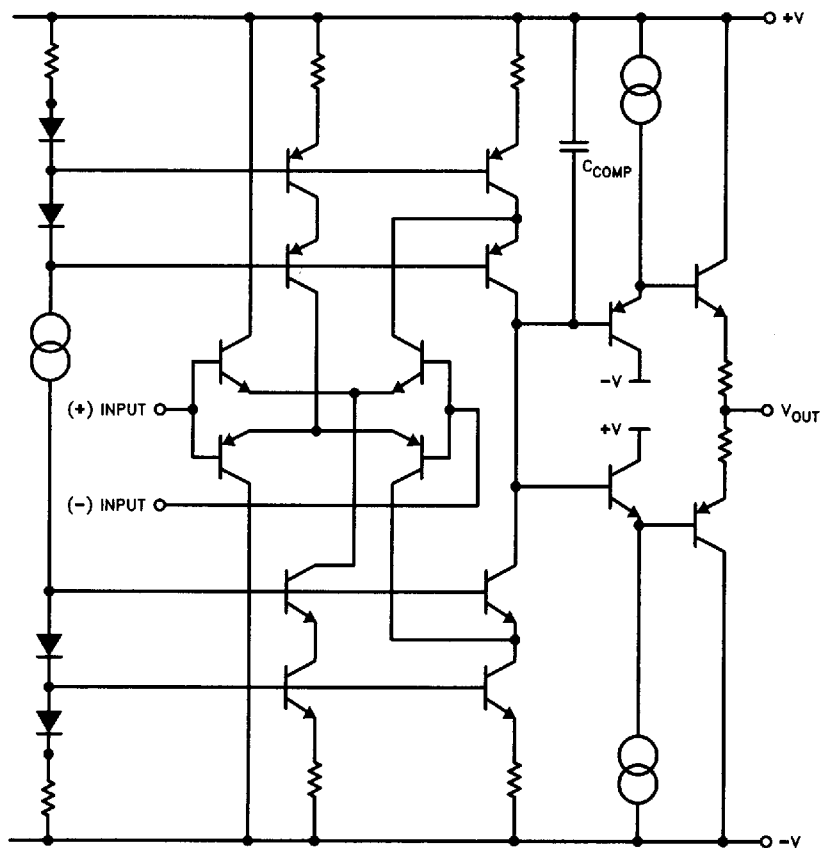
Pin numbers are for the 8-Lead CerDIP.
 Burn-in circuit is identical for all package types.



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Dual, 500 MHz High Speed, Operational Amplifier**Simplified Schematic** (one amplifier)

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Dual, 500 MHz High Speed, Operational Amplifier

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EL2223 Macromodel

```

* Connections:      + input
*                   |
*                   | - input
*                   |
*                   | + Vsupply
*                   |
*                   | - Vsupply
*                   |
*                   | output
*                   |
.subckt M2233      3      2      7      4      6

```

* Input stage

```

ie 37 4 2mA
r6 36 37 60
r7 38 37 60
rc1 7 30 75
rc2 7 39 75
q1 30 3 36 qn
q2 39 2 38 qna
ediff 33 0 39 30 7.25
rdiff 33 0 1Meg

```

* Compensation Section

```

ga 0 34 33 0 2.6m
rh 34 0 3Meg
ch 34 0 1.5pF
rc 34 40 600
cc 40 0 7pF

```

* Poles

```

ep 41 0 40 0 1
rpa 41 42 75
cpa 42 0 25pF
rpb 42 43 50
cpb 43 0 15pF

```

* Output Stage

```

ios1 7 50 1.25mA
ios2 51 4 1.25mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 25
ros2 6 53 25

```

* models

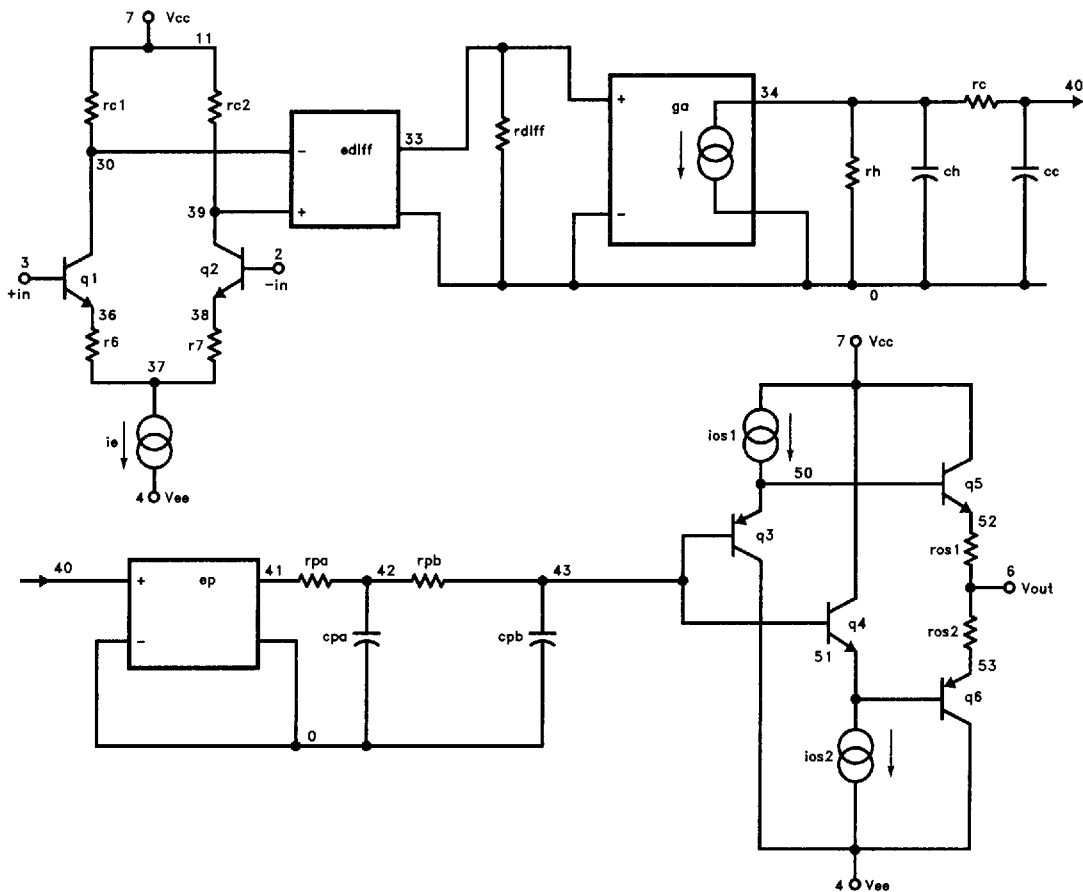
```

.model qn npn (is = 800.0E-18 bf = 250 tf = 0.2nS)
.model qna npn (is = 864E-18 bf = 300 tf = 0.2nS)
.model qp pnp (is = 800E-18 bf = 60 tf = 0.2nS)
.ends

```

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Dual, 500 MHz High Speed, Operational Amplifier**EL2223 Macromodel — Contd.**

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