



1. GENERAL DESCRIPTION

EM78447S is an 8-bit microprocessor with low-power and high-speed CMOS technology. Integrated into a single chip are on-chip watchdog timer (WDT), RAM, ROM, real time clock/counter, external and interrupt, power down mode, and tri-state I/O.



2. FEATURES

- Operating voltage range: 2.3V~5.5V.
- Operating in temperature range: 0°C~70°C.
- Operating frequency range (base on 2 clocks)
 - * Crystal mode: DC~20MHz at 5V, DC~8MHz at 3V, DC~4MHz at 2.3V.
 - * RC mode: DC~4MHz at 5V, DC~4MHz at 3V, DC~4MHz at 2.3V.
- Low power consumption:
 - * Less then 2.2 mA at 5V/4MHz
 - * Typically 30 μ A at 3V/32KHz
 - * Typically 1 μ A during sleep mode
- 4K \times 13 bits on chip ROM
- One configuration register to accommodate user' s requirements
- 148 \times 8 bits on chip registers (SRAM, general purpose register)
- 3 bi-directional I/O ports
- 5 level stacks for subroutine nesting
- 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
- Two clocks per instruction cycle
- Power down (SLEEP) mode
- Two available interruptions
 - * TCC overflow interrupt
 - * External interrupt
- Programmable free running watchdog timer
- 10 programmable pull-high pins
- 2 programmable open-drain pins
- 2 programmable R-option pins
- Package types:
 - * 28 pin DIP 600mil :EM78447SAP
 - * 28 pin SOP(SOIC) 300mil :EM78447SAM
 - * 28 pin SSOP 209mil :EM78447SAS
 - * 32 pin DIP 300mil :EM78447SBP
 - * 32 pin SOP(SOIC) 450mil :EM78447SBWM



EM78447S MASK ROM

- 99.9% single instruction cycle commands
- The transient point of system frequency between HXT and LXT is around 400KHz

3. PIN ASSIGNMENT

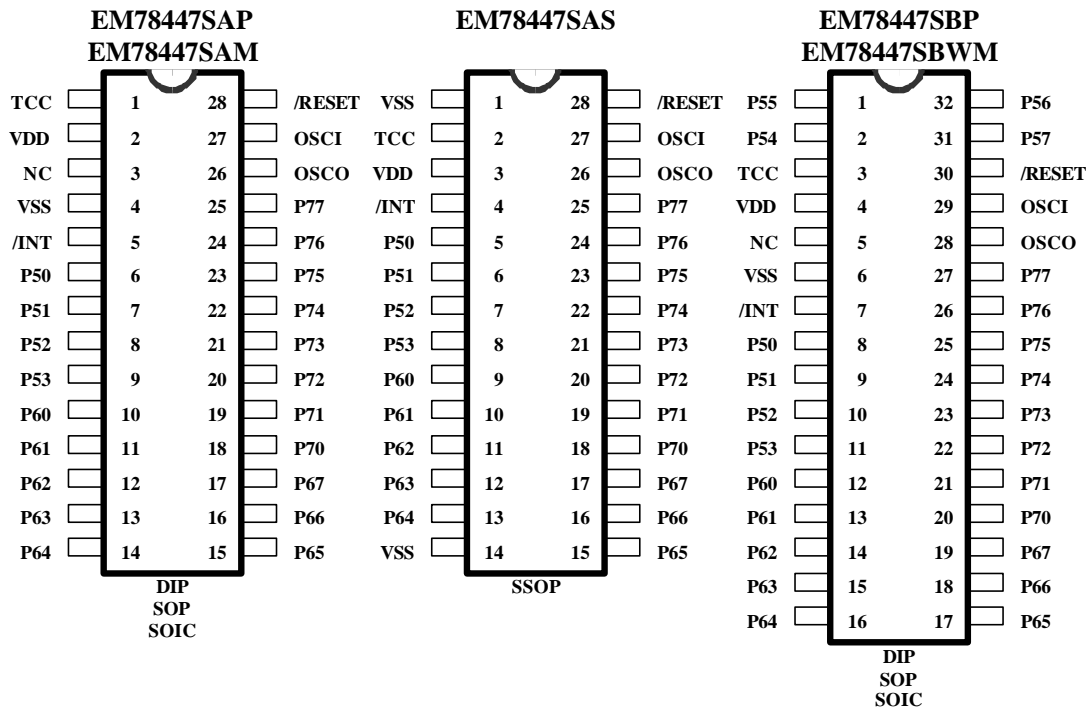


Fig. 1 Pin assignment

Table 1 EM78447SAP and EM78447SAM Pin Description

Symbol	Pin No.	Type	Function
VDD	2	-	* Power supply.
OSCI	27	I	* XTAL type: Crystal input terminal or external clock input pin. * RC type: RC oscillator input pin.
OSCO	26	I/O	* XTAL type: Output terminal for crystal oscillator or external clock input pin. * RC type: Instruction clock output. * External clock signal input.
TCC	1	I	* The real time clock/counter (with Schmitt trigger input pin), must be tied to VDD or VSS if not in use.
/RESET	28	I	* Input pin with Schmitt trigger. If this pin remains at logic low, the controller will also remain in reset condition.
P50~P53	6~9	I/O	* P50~P53 are bi-directional I/O pins.
P60~P67	10~17	I/O	* P60~P67 are bi-directional I/O pins. These can be pulled-high internally by software control.
P70~P77	18~25	I/O	* P70~P77 are bi-directional I/O pins. * P74~P75 can be pulled-high internally by software control. * P76~P77 can have open-drain output by software control. * P70 and P71 can also be defined as the R-option pins.



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/INT	5	I	* External interrupt pin triggered by falling edge.
VSS	4	-	* Ground.
NC	3	-	* No connection.

Table 2 EM78447SAS Pin Description

Symbol	Pin No.	Type	Function
VDD	3	-	* Power supply.
OSCI	27	I	* XTAL type: Crystal input terminal or external clock input pin. * RC type: RC oscillator input pin.
OSCO	26	I/O	* XTAL type: Output terminal for crystal oscillator or external clock input pin. * RC type: Instruction clock output. * External clock signal input.
TCC	2	I	* The real time clock/counter (with Schmitt trigger input pin), must be tied to VDD or VSS if not in use.
/RESET	28	I	* Input pin with Schmitt trigger. If this pin remains at logic low, the controller will also remain in reset condition.
P50~P53	5~8	I/O	* P50~P53 are bi-directional I/O pins.
P60~P67	9~13, 15~17	I/O	* P60~P67 are bi-directional I/O pins. These can be pulled-high internally by software control.
P70~P77	18~25	I/O	* P70~P77 are bi-directional I/O pins. * P74~P75 can be pulled-high internally by software control. * P76~P77 can have open-drain output by software control. * P70 and P71 can also be defined as the R-option pins.
/INT	4	I	* External interrupt pin triggered by falling edge.
VSS	1,14	-	* Ground.

Table 3 EM78447SBP and EM78447SBWM Pin Description

Symbol	Pin No.	Type	Function
VDD	4	-	* Power supply.
OSCI	29	I	* XTAL type: Crystal input terminal or external clock input pin. * RC type: RC oscillator input pin.
OSCO	28	I/O	* XTAL type: Output terminal for crystal oscillator or external clock input pin. * RC type: Instruction clock output. * External clock signal input.
TCC	3	I	* The real time clock/counter (with Schmitt trigger input pin), must be tied to VDD or VSS if not in use.
/RESET	30	I	* Input pin with Schmitt trigger. If this pin remains at logic low, the controller will also remain in reset condition.
P50~P57	8~11,2~1, 32~31	I/O	* P50~P57 are bi-directional I/O pins.
P60~P67	12~19	I/O	* P60~P67 are bi-directional I/O pins. These can be pulled-high internally by software control.
P70~P77	20~27	I/O	* P70~P77 are bi-directional I/O pins. * P74~P75 can be pulled -high internally by software control. * P76~P77 can have open-drain output by software control. * P70 and P71 can also be defined as the R-option pins.
/INT	7	I	* External interrupt pin triggered by falling edge.
VSS	6	-	* Ground.
NC	5	-	* No connection.

4. FUNCTION DESCRIPTION

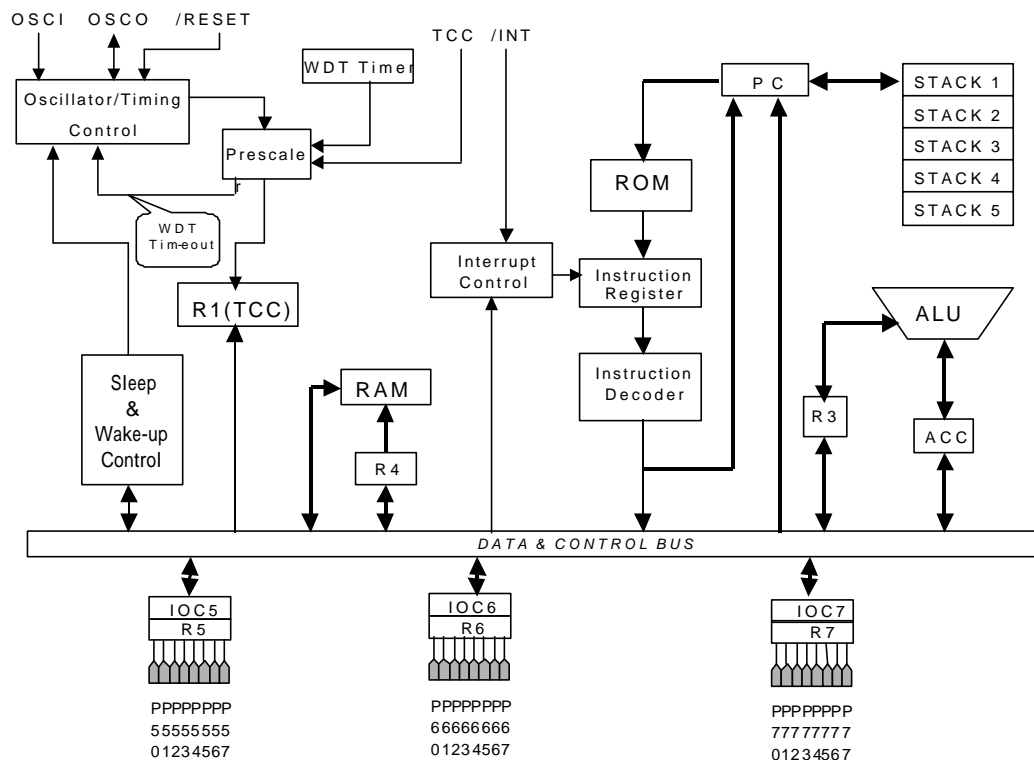


Fig. 2 Functional block diagram

4.1 Operational Registers

1. R0 (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is as indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

2. R1 (Time Clock /Counter)

- Increased by an external signal edge, which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock.
- Writable and readable as any other registers.
- Defined by resetting PAB (CONT-3).
- The prescaler is assigned to TCC, if the PAB bit (CONT-3) is reset.

- The contents of the prescaler counter will be cleared only when TCC register is written with a value.

3. R2 (Program Counter) & Stack

- Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in Fig.3.
- Generating 1024×13 bits on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- R2 is set as all "0"s when under RESET condition.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to go to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2,A" allows the contents of 'A' to be added to the current PC, and the ninth and tenth bits of the PC are cleared.
- "MOV R2,A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC are cleared.
- Any instruction that writes to R2 (e.g. "ADD R2,A", "MOV R2,A", "BC R2,6",.....) will cause the ninth and tenth bits (A8~A9) of the PC to be cleared. Thus, the computed jump is limited to the first 256 locations of a page.
- All instruction are single instruction cycle (fclk/2 or fclk/4) except for the instruction that would change the contents of R2. Such instruction will need one more instruction cycle.

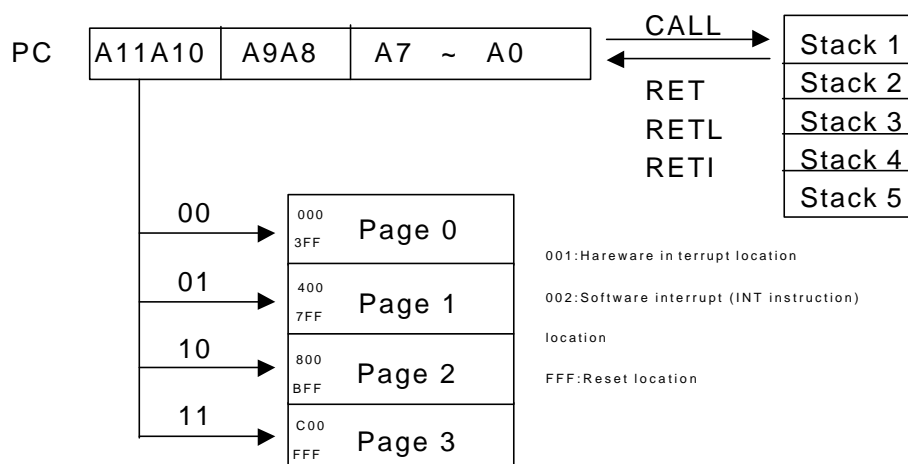


Fig. 3 Program Counter Organization



4. R3 (Status Register)

7	6	5	4	3	2	1	0
GP	PS1	PS0	T	P	Z	DC	C

- Bit 0 (C) Carry flag
- Bit 1 (DC) Auxiliary carry flag
- Bit 2 (Z) Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.
- Bit 3 (P) Power down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.
- Bit 4 (T) Time-out bit. Set to 1 with the "SLEP" and "WDTC" commands, or during power up and reset to 0 by WDT timeout.
- Bits 5 (PS0) ~ 6 (PS1) Page select bits. PS0~PS1 are used to pre-select a program memory page. When executing a "JMP", "CALL", or other instructions which causes the program counter to change (e.g. MOV R2, A), PS0~PS1 are loaded into the 11th and 12th bits of the program counter where it selects one of the available program memory pages. Note that RET (RETL, RETI) instruction does not change the PS0~PS1 bits. That is, the return will always be to the page from where the subroutine was called, regardless of the current setting of PS0~PS1 bits.

PS1	PS0	Program memory page [Address]
0	0	Page 0 [000-3FF]
0	1	Page 1 [400-7FF]
1	0	Page 2 [800-BFF]
1	1	Page 3 [C00-FFF]

- Bit 7 (GP) General read/write bit.

5. R4 (RAM Select Register)

- Bits 0~5 are used to select the registers (address: 00~3F) in the indirect addressing mode.
- Bits 6~7 determine which bank is activated among the 4 banks.
- If no indirect addressing is used, the RSR is used as an 8-bit general-purposed read/writer register.
- See the configuration of the data memory in Fig. 4.

6. R5~R7 (Port 5 ~ Port7)

- R5, R6 and R7 are I/O registers

7. R8~R1F and R20~R3E (General-Purpose Register)

- R8~R1F, and R20~R3E (including Banks 0~3) are general-purpose registers.

8. R3F (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	EXIF	-	-	TCIF

- Bit 0 (TCIF) TCC overflow interrupt flag. Set as TCC overflows; flag cleared by software.

- Bit 3(EXIF) External interrupt flag. Set by falling edge on /INT pin, flag cleared by software
- Bits 1,2,4~7 are not used and read as "0".
- "1" means interrupt request, "0" means non-interrupt.
- R3F can be cleared by instruction, but cannot be set by instruction.
- IOCF is the interrupt mask register.
- Note that to read R3F will obtain the result of "logic AND" of R3F and IOCF.

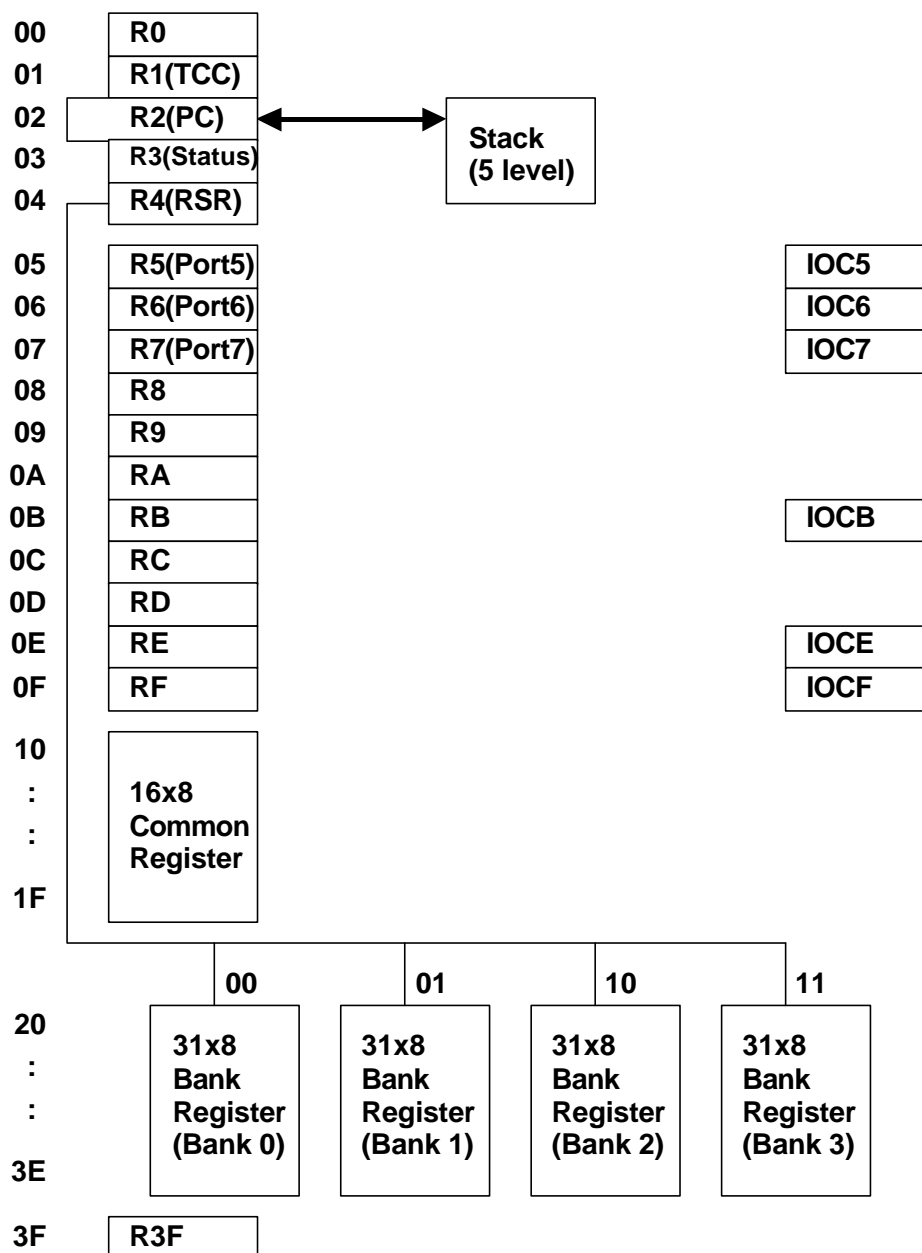


Fig. 4 Data Memory Configuration



9. R20~R3E (General-Purpose Register)

- RA~R1F, and R20~R3E (including Banks 0~3) are general-purpose registers.

10. R3F (Interrupt Status Register)

7	6	5	4	3	2	1	0
-	-	-	-	EXIF	-		TCIF

“1” means interrupt request, and “0” means no interrupt occur.

- **Bit 0 (TCIF)** TCC overflow interrupt flag. Set when TCC overflows, reset by software.
- **Bit 3 (EXIF)** External interrupt flag. Set by falling edge on /INT pin, reset by software.
- Bits 1, 2 and 3 ~ 7 Not used.
- R3F can be cleared by instruction but cannot be set.
- IOCF is the interrupt mask register.
- Note that the result of reading R3F is the "logic AND" of R3F and IOCF.

4.2 Special Purpose Registers

1. A (Accumulator)

- Internal data transfer, or instruction operand holding.
- It can not be addressed.

2. CONT (Control Register)

7	6	5	4	3	2	1	0
/PHEN	/INT	TS	TE	PAB	PSR2	PSR1	PSR0

- Bit 0 (PSR0) ~ Bit 2 (PSR2) TCC/WDT prescaler bits.

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

- **Bit 3 (PAB)** Prescaler assignment bit.
0: TCC
1: WDT
- **Bit 4 (TE)** TCC signal edge
0: increment if the transition from low to high takes place on TCC pin
1: increment if the transition from high to low takes place on TCC pin



- **Bit 5 (TS)** TCC signal source
 - 0: internal instruction cycle clock
 - 1: transition on TCC pin
- **Bit 6 (/INT)** Interrupt enable flag
 - 0: masked by DISI or hardware interrupt
 - 1: enabled by ENI/RETI instructions
- **Bit 7 (/PHEN)** Control bit used to enable the pull-high of P60~P67, P74 and P75 pins
 - 0: Enable internal pull-high.
 - 1: Disable internal pull-high.
- CONT register is both readable and writable.

3. IOC5 ~ IOC7 (I/O Port Control Register)

- "1" put the relative I/O pin into high impedance, while "0" defines the relative I/O pin as output.
- IOC5 and IOC7 registers are both readable and writable.

4. IOCB (Wake-up Control Register for Port 6)

7	6	5	4	3	2	1	0
/WUE7	/WUE6	/WUE5	/WUE4	/WUE3	/WUE2	/WUE1	/WUE0

- **Bit 0 (/WUE0)** Control bit used to enable the wake-up function of P60 pin.
 - 0: Enable internal wake-up.
 - 1: Disable internal wake-up.
- **Bit 1 (/WUE1)** Control bit is used to enable the wake-up function of P61 pin.
- **Bit 2 (/WUE2)** Control bit is used to enable the wake-up function of P62 pin.
- **Bit 3 (/WUE3)** Control bit is used to enable the wake-up function of P63 pin.
- **Bit 4 (/WUE4)** Control bit is used to enable the wake-up function of P64 pin.
- **Bit 5 (/WUE5)** Control bit is used to enable the wake-up function of P65 pin.
- **Bit 6 (/WUE6)** Control bit is used to enable the wake-up function of P66 pin.
- **Bit 7 (/WUE7)** Control bit is used to enable the wake-up function of P67 pin.
- IOCB Register is both readable and writable.

6. IOCE (WDT Control Register)

7	6	5	4	3	2	1	0
-	ODE	WDTE	SLPC	ROC	-	-	/WUE

- **Bit 0 (/WUE)** Control bit used to enable the wake-up function of P74 and P75.
 - 0: Enable the wake-up function.
 - 1: Disable the wake-up function.
- The /WUE bit can be read and written.



- **Bit 3 (ROC)** ROC is used for the R-option. Setting ROC to "1" will enable the status of R-option pins (P70, P71) to be read by the controller. Clearing ROC will disable the R-option function. Otherwise, the R-option function is introduced. Users must connect the P71 pin or/and P70 pin to VSS by a 560K Ω external resistor (Rex). If Rex is connected/disconnected with VDD, the status of P70 (P71) will be read as "0"/"1" (refer to Fig. 7(b)). The ROC bit can be read and written.
- **Bit 4 (SLPC)** This bit is set by hardware at the falling edge of wake-up signal and is cleared in software. SLPC is used to control the oscillator operation. The oscillator is disabled (oscillator is stopped, and the controller enters the SLEEP2 mode) on the high-to-low transition and is enabled (the controller is awakened from SLEEP2 mode) on low-to-high transition. In order to ensure the stable output of the oscillator, once the oscillator is enabled again, there is a delay for approximately 18¹ ms (oscillator start-up timer (OST)) before the next program instruction is executed. The OST is always activated by wake-up from sleep mode whether the Code Option bit ENWDT is "0" or not. After waking up, the WDT is enabled if Code Option ENWDT is "1". The block diagram of SLEEP2 mode and wake-up caused by input triggered is depicted in Fig. 5. The SLPC bit can be read and written.
- **Bit 5 (WDTE)** Control bit used to enable Watchdog timer.
The WDTE bit can be used only if ENWDT, the CODE Option bit, is "0". If the ENWDT bit is "0", then WDT can be disabled/enabled by the WDTE bit.
0: Disable WDT.
1: Enable WDT.
The WDTE bit is not used if ENWDT, the CODE Option bit ENWDT, is "1". That is, if the ENWDT bit is "1", WDT is always disabled no matter what the WDTE bit status is.
The WDTE bit can be read and written.
- **Bit 6 (ODE)** Control bit used to enable the open-drain of P76 and P77 pins
0: Disable open-drain output.
1: Enable open-drain output.
The ODE bit can be read and written.
- Bits 1~2, and 7 Not used.

7. IOCF (Interrupt Mask Register)

7	6	5	4	3	2	1	0
-	-	-	-	EXIE	-	-	TCIE

¹ NOTE: Vdd = 5V, set up time period = 16.2ms \pm 5%

Vdd = 3V, set up time period = 19.6ms \pm 5%

- Bit 0 (TCIE) TCIF interrupt enable bit.
0: disable TCIF interrupt
1: enable TCIF interrupt
- Bit 3 (EXIE) EXIF interrupt enable bit.
0: disable EXIF interrupt
1: enable EXIF interrupt
- Bits 1, 2 and 4~7 Not used.
- Individual interrupt is enabled by setting its associated control bit in the IOCF to "1".
- Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Fig. 9.
- IOCF register is both readable and writable.

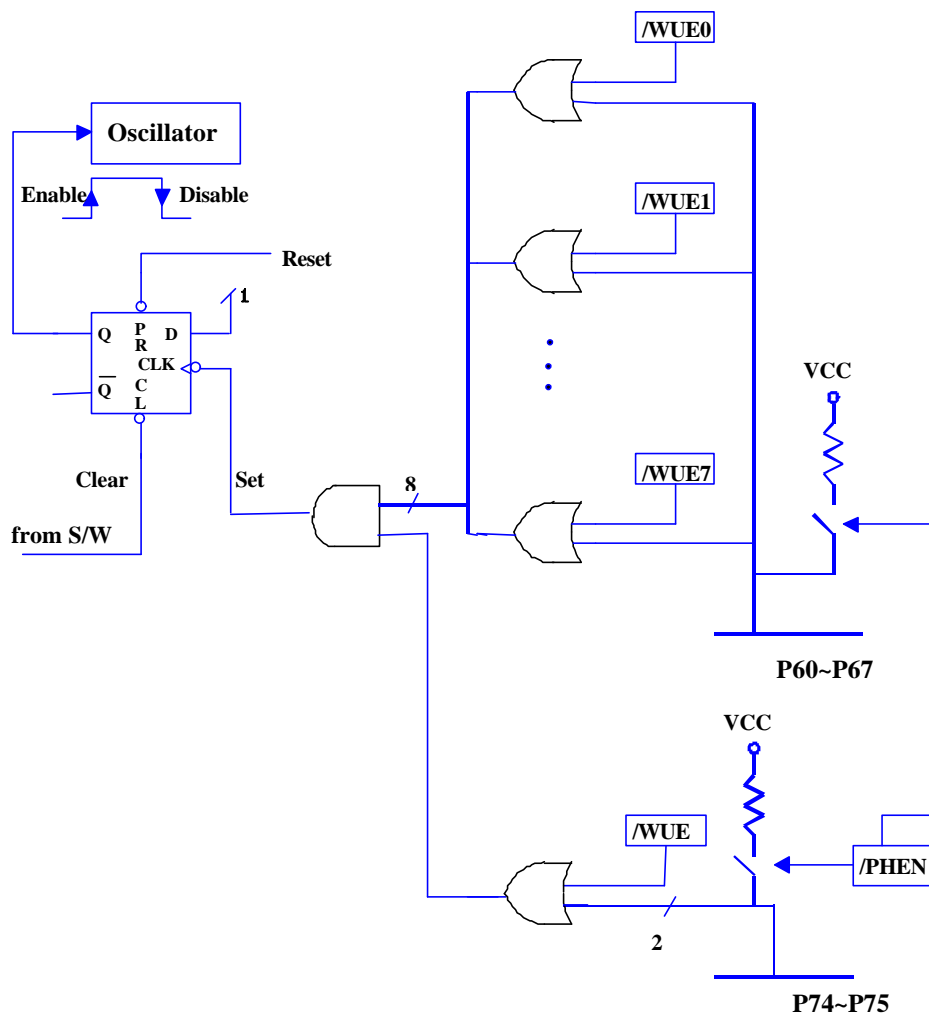


Fig. 5 Block Diagram of Sleep Mode and Wake-up Circuits on I/O Ports

4.3 TCC/WDT & Prescaler

An 8-bit counter is available as prescaler for the TCC or WDT. The prescaler is available for either the TCC or WDT only at any given time, and the PAB bit of CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the prescale ratio. The prescaler is cleared each time the instruction is written to TCC under TCC mode. The WDT and prescaler, when assigned to WDT mode, are cleared by the WDTC or SLEP instructions. Fig. 6 depicts the circuit diagram of TCC/WDT.

- R1 (TCC) is an 8-bit timer/counter. The TCC clock source can be internal clock or external clock input (edge selectable from TCC pin). If TCC signal source is from internal clock, TCC will increase by 1 at every instruction cycle (without prescaler). Referring to Fig. 6 below, clock category ($CLK = F_{osc}/2$ or $CLK = F_{osc}/4$) is dependent on the CODE Option bit CLKS status. $CLK = F_{osc}/2$ if CLKS bit is "0", and $CLK = F_{osc}/4$ if CLKS bit is "1". If TCC signal source is from external clock input, TCC will increase by 1 at every falling edge or rising edge of TCC pin.
- The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e., in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during the normal mode by software programming. Refer to WDTE bit of IOCE register. Without prescaler, the WDT time-out period is approximately 18ms¹(default).

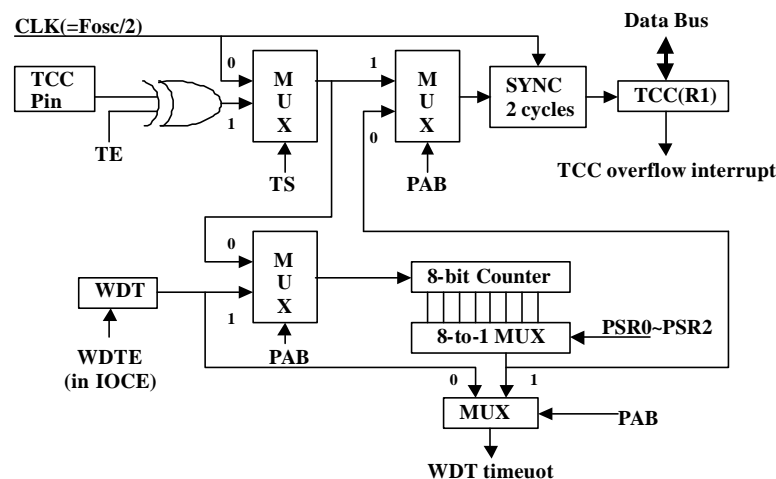


Fig. 6 Block Diagram of TCC and WDT

¹ NOTE: $V_{dd} = 5V$, set up time period = $16.2ms \pm 5\%$

$V_{dd} = 3V$, set up time period = $19.6ms \pm 5\%$

The I/O registers, Port 5, Port 6, and Port 7, are bi-directional tri-state I/O ports. The functions; Pull-high, R-option, and Open-drain can be internally done by CONT and IOCE respectively. Input status change wake-up function is provided by Port 6, P74, and P75. Each I/O pin can be defined as "input" or "output" pin by the I/O control registers (IOC5 ~ IOC7). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5, Port 6, and Port 7 are shown in the following Figures. 7(a), (b) respectively.





4.5 RESET and Wake-up

1. RESET

A RESET can be invoked by

- (1) Power on reset, or
- (2) /RESET pin input "low", or
- (3) WDT timeout. (if enabled)

The device is kept in a RESET condition for a period of approx. 18ms¹ (one oscillator start-up timer period) after the reset signal is detected. Once the RESET occurs, the following functions are performed (refer to Fig.8).

- The oscillator is running, or initiated.
- The Program Counter (R2) is set to all "1".
- When power is switched on, Bits 5~6 of R3 and the upper 2 bits of R4 are cleared.
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- On power on, Bits 5~6 of R3 are cleared.
- On power on, the upper 2 bits of R4 are cleared.
- The bits of CONT register are set to all "1," except for Bit 6 (INT flag).
- IOCB register is set to "1" (disable P60 ~ P67 wake-up function).
- Bits 3 and 6 of IOCE register are cleared, and Bits 0, 4, and 5 are set to "1".
- Bits 0 and 3 of R3F register and Bits 0 and 3 of IOCF registers are cleared.

Executing the "SLEP" instruction (designated as SLEEP1 mode) achieves sleep mode. While entering sleep mode, WDT (if enabled) is cleared but keeps on running. The controller can be awakened by-

- (1) External reset input on /RESET pin;
- (2) WDT time-out (if enabled)

The above two cases will cause the EM78447S controller to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up).

In addition to the basic SLEEP1 MODE, EM78447S has another sleep mode (set off by clearing "SLPC" bit of IOCE register, designated as SLEEP2 MODE). In the SLEEP2 MODE, the controller

¹ NOTE: Vdd = 5V, set up time period = 16.2ms ± 5%
Vdd = 3V, set up time period = 19.6ms ± 5%



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can be awakened by -

- (A) Any one of the wake-up pins is set to “0.” (refer to Figure 5). Upon waking, the controller will continue to execute the succeeding address. In this case, before entering SLEEP2 MODE, the wake-up function of the trigger sources (P60~P67, and P74~P75) should be selected (e.g., input pin) and enabled (e.g., pull-high, wake-up control). One caution should be noted, after waking up, the WDT is enabled if Code Option bit ENWDT is “0”. The WDT operation (to be enabled or disabled) should be appropriately controlled by software after waking up.
- (B) WDT time-out (if enabled) or external reset input on /RESET pin will cause a controller reset.

Table 4 The Summary of the Initialized Values for Registers

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Type	A B	A B	A B	A B	-	-	-	-
		Power-On	0 1	0 1	0 1	0 1	1	1	1	1
		/RESET and WDT	0 1	0 1	0 1	0 1	1	1	1	1
		Wake-Up from Pin Change	0 P	0 P	0 P	0 P	P	P	P	P
N/A	IOC6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC7	Bit Name	C77	C76	C75	C74	C73	C72	C71	C70
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	/PHEN	/INT	TS	TE	PAB	PSR2	PSR1	PSR0
		Power-On	1	0	1	1	1	1	1	1
		/RESET and WDT	1	P	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0(IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1(TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2(PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	**0/P	**0/P	**0/P	**0/P	**0/P	**0/P	**0/P	**0/P
0x03	R3(SR)	Bit Name	GP	PS1	PS0	T	P	Z	DC	C
		Power-On	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-Up from Pin Change	P	P	P	t	t	P	P	P
0x04	R4(RSR)	Bit Name	RSR.1	RSR.0	-	-	-	-	-	-
		Power-On	0	0	U	U	U	U	U	U
		/RESET and WDT	0	0	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x05	R5(P5)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x06	R6(P6)	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x07	R7(P7)	Bit Name	P77	P76	P75	P74	P73	P72	P71	P70
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P



		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x3F	R3F(ISR)	Bit Name	-	-	-	-	EXIF	-	-	TCIF
		Power-On	U	U	U	U	0	U	U	0
		/RESET and WDT	U	U	U	U	0	U	U	0
		Wake-Up from Pin Change	U	U	U	U	P	U	U	P
0x0B	IOCB	Bit Name	/WUE7	/WUE6	/WUE5	/WUE4	/WUE3	/WUE2	/WUE1	/WUE0
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0E	IOCE	Bit Name	-	ODE	WTE	SLPC	ROC	-	-	/WUE
		Power-On	U	0	1	1	0	U	U	1
		/RESET and WDT	U	0	1	1	0	U	U	1
		Wake-Up from Pin Change	U	P	1	1	P	U	U	P
0x0F	IOCF	Bit Name	-	-	-	-	EXIE	-	-	TCIE
		Power-On	U	U	U	U	0	U	U	0
		/RESET and WDT	U	U	U	U	0	U	U	0
		Wake-Up from Pin Change	U	U	U	U	P	U	U	P
0x08	R8	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x09~0x3E	R9~R3E	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

** To execute the next instruction after the "SLPC" bit status of IOCE register is on high-to-low transition.

X: Not used. U: Unknown or don't care. P: Previous value before reset. t: Check Table 5

2. The Status of RST, T, and P of STATUS Register

A RESET condition is initiated by one of the following events:

1. A power-on condition,
2. A high-low-high pulse on /RESET pin, and
3. Watchdog timer time-out.

The values of T and P, listed in Table 5 can be used to check how the processor wakes up.

Table 6 shows the events that may affect the status of T and P.

Table 5 The Values of RST, T, and P after RESET

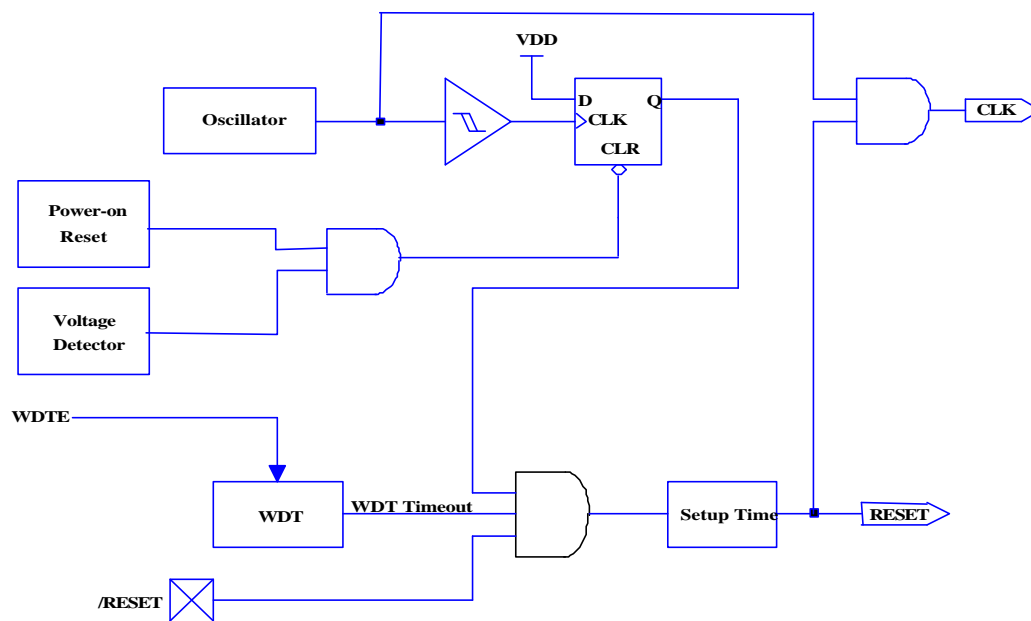
Reset Type	T	P
Power on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during SLEEP1 mode	1	0
/RESET wake-up during SLEEP2 mode	*P	*P
WDT during Operating mode	0	*P
WDT wake-up during SLEEP1 mode	0	0
WDT wake-up during SLEEP2 mode	0	*P
Wake-Up on pin change during SLEEP2 mode	*P	*P

*P: Previous status before reset

Table 6 The Status of RST, T, and P that are Affected by Events

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-Up on pin change during SLEEP2 mode	*P	*P

*P: Previous value before reset


Fig. 8 Reset Block Diagram

4.6 Interrupt

The EM78447S has two interrupts as listed below:

- (1) TCC overflow interrupt
- (2) External interrupt (/INT pin).

R3F is the interrupt status register, which records the interrupt requests in the relative flags/bits. IOCF is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (if enabled) occurs, the next instruction will be fetched from address 001H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in the R3F. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

When an interrupt is generated by the INT instruction (if enabled), the next instruction will be fetched from address 002H.

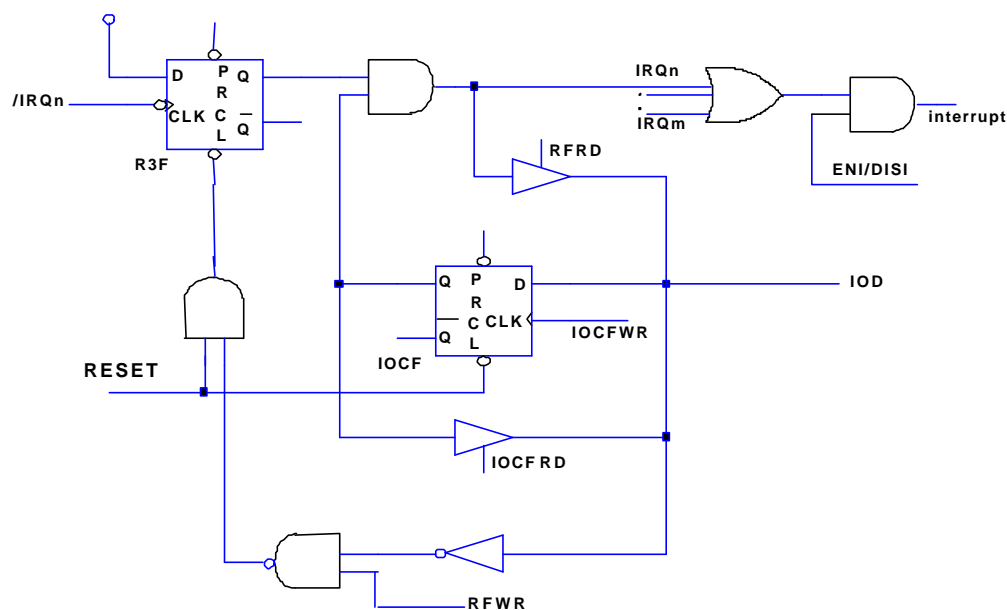


Fig. 9 Interrupt input circuit

4.7 Oscillator

1. Oscillator Modes

The maximum operating frequencies of crystal/resonator on different VDDs are listed in Table 8.

Table 7 Oscillator Modes Defined by MS and HLP

Mode	MS	HLF	HLP
ERC(External RC oscillator mode)	0	*X	*X
HXT(High XTAL oscillator mode)	1	1	*X

LXT(Low XTAL oscillator mode)	1	0	0
-------------------------------	---	---	---

<Note> 1. X, Don't care

2. The transient point of system frequency between HXT and LXY is around 400 KHz.

Table 8 The Summary of Maximum Operating Speeds

Conditions	VDD	Fxt max.(MHz)
Two cycles with two clocks	2.3	4.0
	3.0	8.0
	5.0	20.0

2. Crystal Oscillator/Ceramic Resonators(XTAL)

EM78447S can be driven by an external clock signal through the OSCI pin as shown in Fig. 10.

In most applications, Pin OSCI and Pin OSCO is connected with a crystal or ceramic resonator to generate oscillation. Fig. 11 depicts of such circuit. This is applicable in either HXT mode or in the LXT mode. Table 9 provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be required for AT strip cut crystal or low frequency mode.

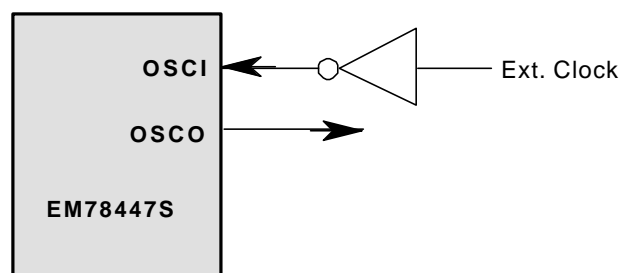


Fig. 10 External Clock Input Circuit

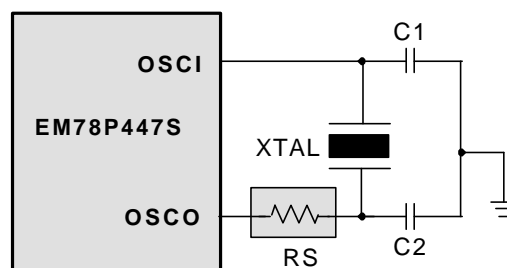


Fig. 11 Crystal/Resonator Circuit

Table 9 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator

Oscillator Type	Frequency Mode	Frequency	C1(pF)	C2(pF)
Ceramic Resonators	HXT	455 kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768kHz	25	15
		100KHz	25	25
		200KHz	25	25
	HXT	455KHz	20~40	20~150
		1.0MHz	15~30	15~30
		2.0MHz	15	15
		4.0MHz	15	15

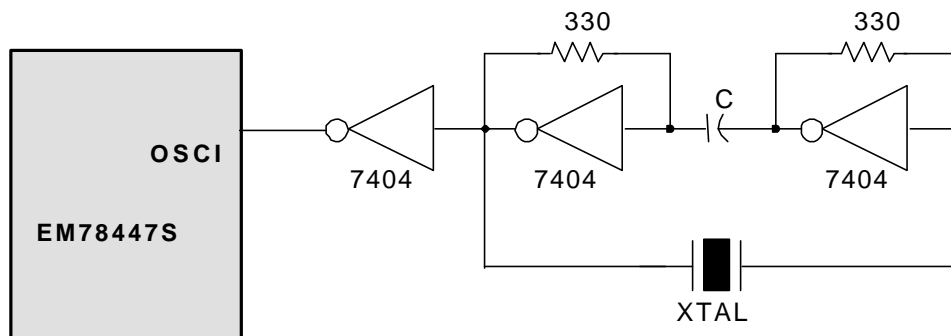


Fig. 12 Crystal/Resonator-Series Mode Circuit

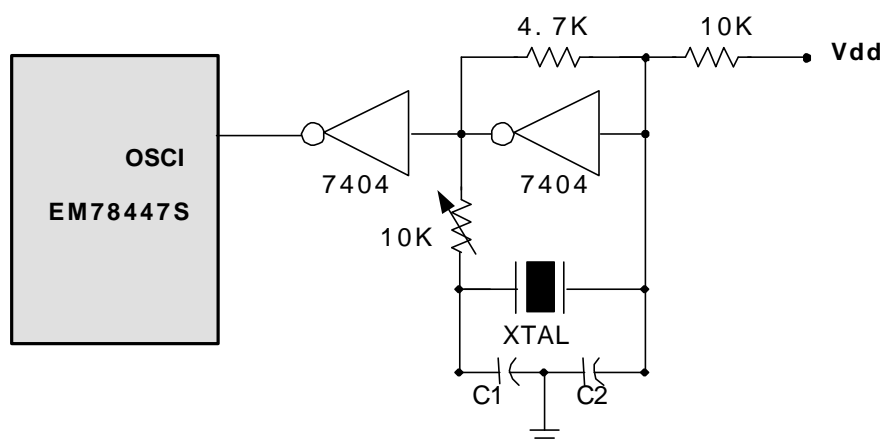


Fig. 13 Crystal/Resonator-Parallel Mode Circuit

3. External RC Oscillator Mode

For some applications that do not need a very precise timing calculation, the RC oscillator (Fig. 15) offers a lot of cost savings. Nevertheless, user should be aware that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (R_{ext}), the capacitor (C_{ext}), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to the manufacturing process variations.

In order to maintain a stable system frequency, the values of the C_{ext} should not be less than 20pF, and that the value of R_{ext} should not be greater than 1 M ohm. If they can not be kept in this range, the frequency is easily affected by noise, humidity, and leakage.

The smaller the R_{ext} in the RC oscillator, the faster its frequency will be. On the contrary, for very low R_{ext} values, for instance, 1 K Ω , the oscillator could become unstable, because the NMOS cannot properly discharge the current from the capacitor.

Based on the above reasons, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types, and the way the PCB is layout, will affect the system frequency in one way or another.

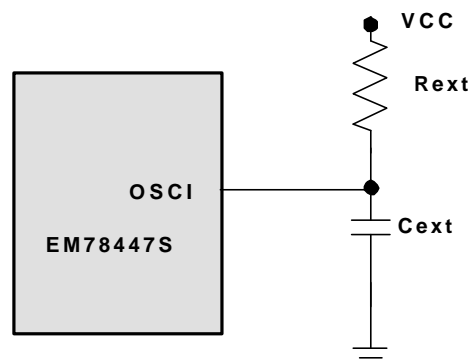


Fig. 14 External RC Oscillator Mode Circuit



Table 10 RC Oscillator Frequencies

Cext	Rext	Average Fosc 5V,25°C	Average Fosc 3V,25°C
20 pF	3.3k	4.32 MHz	3.56 MHz
	5.1k	2.83 MHz	2.8 MHz
	10k	1.62MHz	1.57 MHz
	100k	184 KHz	187 KHz
100 pF	3.3k	1.39 MHz	1.35 MHz
	5.1k	950 KHz	930 KHz
	10k	500 KHz	490 KHz
	100k	54KHz	55 KHz
300 pF	3.3k	580 KHz	550 KHz
	5.1k	390 KHz	380 KHz
	10k	200 KHz	200 KHz
	100k	21 KHz	21 KHz

<Note> 1. Measured on DIP packages.
2. Design reference only.

4.8 CODE Option Register

The EM78447S has one CODE option word that is not a part of the normal program memory. The option bits cannot be accessed during normal program execution.

Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6
CLK	MS	HLF	LVDD	/ENWDT	TYPE	-

- **Bit 0 (CLK):** Instruction period option bit.

0: two oscillator periods.

1: four oscillator periods.

Refer to the section on Instruction Set.

- **Bit 1 (MS):** Oscillator type selection.

0: RC type

1: XTAL type(XTAL1 and XTAL2)

- **Bit 2 (HLF):** XTAL frequency selection

0: XTAL2 type (low frequency, 32.768KHz)

1: XTAL1 type (high frequency)

This bit will affect system oscillation only when Bit1 (MS) is "1". When MS is "0", HLF must be "0".

<Note>: The transient point of system frequency between HXT and LXY is around 400 KHz.

- **Bit 3 (LVDD):** Levels of the Operating Voltage.

0: Operating Voltage 2.3V ~ 5.5V, not power saving.

1: Operating Voltage 4V ~ 5.5V, power saving.

- **Bit 4 (/ENWDT):** Watchdog timer enable bit.

0: Enable

1: Disable

- **Bit 5(TYPE):** Type selection for EM78447SA or B.

0: EM78447SB

1: EM78447SA

- **Bit 6 :** Reserved.

The bit6 set to "1" all the time.

4.9 Power On Considerations

Any microcontroller is not guaranteed to start operating properly before the power supply stabilizes. EM78447S is equipped with Power On Voltage Detector (POVD) with a detection level of 2.0V. Its performance improves if Vdd rise fast enough (10 ms or less). Under critical applications, however, extra devices may still be required to assist in solving power-up problems.

4.10 External Power On Reset Circuit

The circuit shown in Fig.15 implements an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough to allow Vdd to reach minimum operation voltage. This circuit is used when the power supply has a slow rise speed. Because the current leakage from the /RESET pin is about $\pm 5\mu\text{A}$, it is recommended that R should not be great than 40 K. In this way, the voltage at Pin /RESET is held below 0.2V. The diode (D) acts as a short circuit at power-down. The capacitor, C, is discharged rapidly and fully. Rin, the current-limited resistor, prevents high current discharge or ESD (electrostatic discharge) from flowing into Pin /RESET.

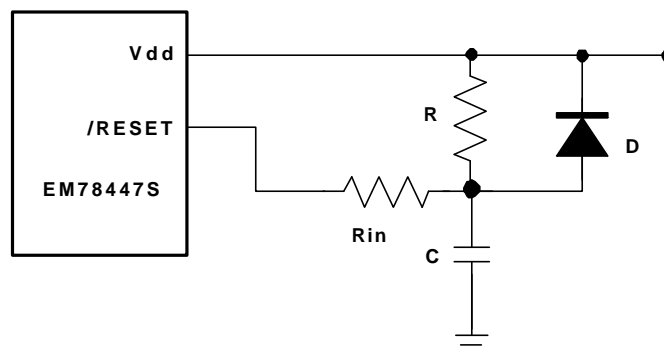


Fig. 15 External Power-Up Reset Circuit

4.11 Residue-Voltage Protection

When battery is replaced, device power (Vdd) is removed but residue-voltage remains. The residue-voltage may trips below Vdd minimum, but not to zero. This condition may cause a poor power on reset. Fig.16 and Fig.17 show how to build a residue-voltage protection circuit.

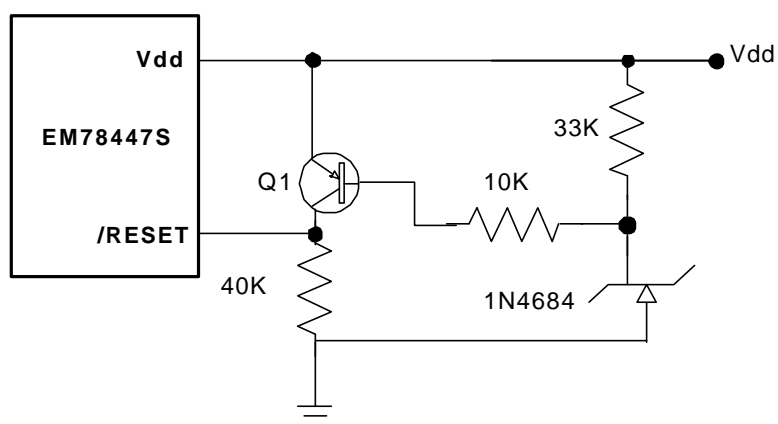


Fig. 16 Circuit 1 for the Residue Voltage Protection

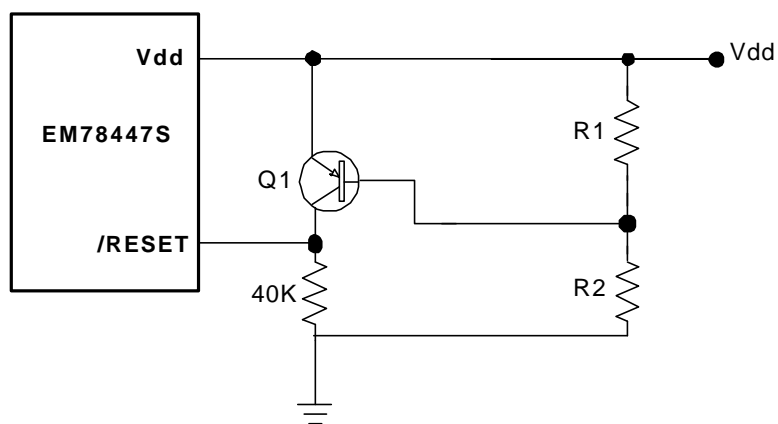


Fig. 17 Circuit 2 for the Residue Voltage Protection



4.12 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2",). In this case, the execution takes two instruction cycles.

Under certain conditions, if the instruction cycle specification is not suitable for some applications, they can be modified as follows:

- (A) Change one instruction cycle to consist of 4 oscillator periods.
- (B) Executed within two instruction cycles, "JMP", "CALL", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") instructions which were tested to be true. Also execute within two instruction cycles, the instructions that are written to the program counter.

Case (A) is selected by the CODE Option bit, called CLK. One instruction cycle consists of two oscillator clocks if CLK is low, and four oscillator clocks if CLK is high.

Note that once the 4 oscillator periods within one instruction cycle is selected as in Case (A), the internal clock source to TCC should be $CLK = Fosc/4$, not $Fosc/2$ as indicated in Fig. 5.

In addition, the instruction set has the following features:

- (1) Every bit of any register can be set, cleared, or tested directly.
- (2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The symbol "R" represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction. "b" represents a bit field designator that selects the value for the bit which is located in the register "R", and affects operation. "k" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None <Note1>
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None



EM78447S MASK ROM

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None <Note1>
0 0000 0010 0000	0020	TBL	R2+A → R2, Bits 8~9 of R2 unchanged	Z,C,DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b brrr rrrr	0xxx	BC R,b	0 → R(b)	None <Note2>
0 101b brrr rrrr	0xxx	BS R,b	1 → R(b)	None <Note3>
0 110b brrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b brrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP],	None



EM78447S MASK ROM

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
			(Page, k) → PC	
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1 1110 0000 0010	1E02	INT	PC+1 → [SP], 002H → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC

<Note1> This instruction is applicable to IOC5 ~ IOC7, IOCB, IOCE, IOCF only.

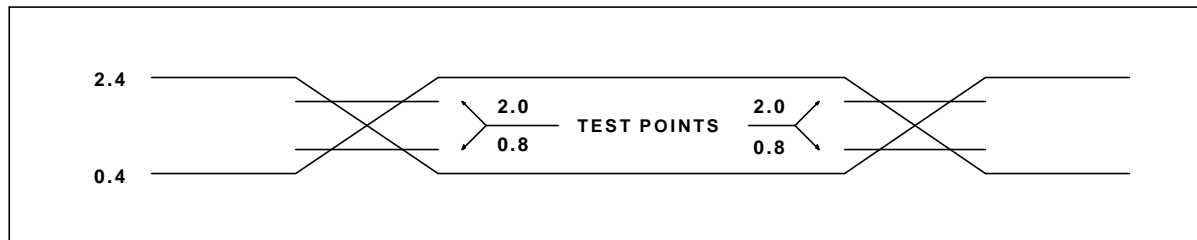
<Note2> This instruction is not recommended for R3F operation.

<Note3> This instruction cannot operate under R3F.



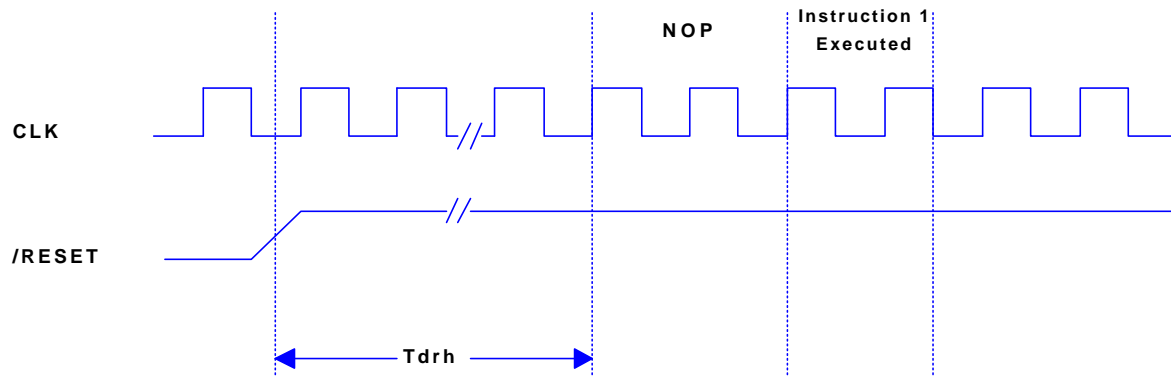
4.13 Timing Diagram

AC Test Input/Output Waveform

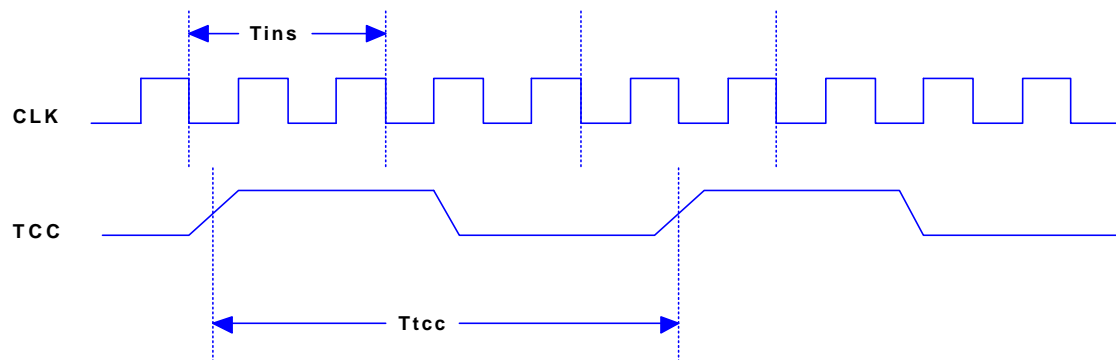


AC Testing : Input is driven at 2.4V for logic "1", and 0.4V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")





5. ABSOLUTE MAXIMUM RATINGS

Items	Rating		
Temperature under bias	0°C	to	70°C
Storage temperature	-65°C	to	150°C
Input voltage	-0.3V	to	+6.0V
Output voltage	-0.3V	to	+6.0V
Operating Frequency (2clk)	DC	to	20MHz



6. ELECTRICAL CHARACTERISTICS

6.1 DC Electrical Characteristic

(Ta= 0°C ~ 70 °C, VDD= 5.0V±5%, VSS= 0V)

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
FXT	XTAL: VDD to 3V	Two cycle with two clocks	DC		8.0	MHz
	XTAL: VDD to 5V	Two cycle with two clocks	DC		20.0	MHz
ERC	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	F±30%	950	F±30%	KHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS			±1	μA
VIH1	Input High Voltage (VDD=5V)	Ports 5, 6	2.0			V
VIL1	Input Low Voltage (VDD=5V)	Ports 5, 6			0.8	V
VIHT1	Input High Threshold Voltage (VDD=5V)	/RESET, TCC	2.0			V
VILT1	Input Low Threshold Voltage (VDD=5V)	/RESET, TCC			0.8	V
VIHX1	Clock Input High Voltage (VDD=5V)	OSCI	3.5			V
VILX1	Clock Input Low Voltage (VDD=5V)	OSCI			1.5	V
VIH2	Input High Voltage (VDD=3V)	Ports 5, 6	1.5			V
VIL2	Input Low Voltage (VDD=3V)	Ports 5, 6			0.4	V
VIHT2	Input High Threshold Voltage (VDD=3V)	/RESET, TCC	1.5			V
VILT2	Input Low Threshold Voltage (VDD=3V)	/RESET, TCC			0.4	V
VIHX2	Clock Input High Voltage (VDD=3V)	OSCI	2.1			V
VILX2	Clock Input Low Voltage (VDD=3V)	OSCI			0.9	V
VOH1	Output High Voltage (Ports 5, 6, 7)	IOH = -10.0 mA	2.4			V
VOL1	Output Low Voltage (Ports 5, 6)	IOL = 9.0 mA			0.4	V
VOL2	Output Low Voltage (Port7)	IOL = 14.0 mA			0.4	V
IPH	Pull-high current	Pull-high active, input pin at VSS	-50	-100	-240	μA
ISB1	Power down current	All input and I/O pins at VDD, output pin floating, WDT disabled			1	μA
ISB2	Power down current	All input and I/O pins at VDD, output pin floating, WDT enabled			8	μA
ICC1	Operating supply current (VDD=3V) at two cycles/four clocks	/RESET= 'High', Fosc=32KHz (Crystal type,CLKS="0"), output pin floating, WDT disabled	15	25	30	μA
ICC2	Operating supply current (VDD=3V) at two cycles/four clocks	/RESET= 'High', Fosc=32KHz (Crystal type,CLKS="0"), output pin floating, WDT enabled		30	35	μA
ICC3	Operating supply current (VDD=5V) at two cycles/two clocks	/RESET= 'High', Fosc=4MHz (Crystal type,CLKS="0"), output pin floating, WDT enabled			2.2	mA
ICC4	Operating supply current (VDD=5V) at two cycles/four clocks	/RESET= 'High', Fosc=10MHz (Crystal type,CLKS="0"), output pin floating, WDT enabled			5.0	mA



6.2 AC Electrical Characteristic

(Ta=0°C ~ 70 °C, VDD=5V±5%, VSS=0V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle		45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100		DC	ns
		RC type	500		DC	ns
Ttcc	TCC input period		(Tins+20)/N*			ns
Tdrh	Device reset hold time	Ta = 25°C	17.0	16.2	15.4	ms
Trst	/RESET pulse width	Ta = 25°C	2000			ns
Twdt	Watchdog timer period	Ta = 25°C	17.0	16.2	15.4	ms
Tset	Input pin setup time			0		ns
Thold	Input pin hold time			20		ns
Tdelay	Output pin delay time	Cload=20pF		50		ns

* N= selected prescaler ratio.



APPENDIX

Package Types:

MASK MCU	Package Type	Pin Count	Package Size
EM78447SAP	DIP	28	600 mil
EM78447SAM	SOP	28	300 mil
EM78447SAS	SSOP	28	209 mil
EM78447SBP	DIP	32	600 mil
EM78447SBWM	SOP	32	450 mil