



義隆電子股份有限公司

ELAN MICROELECTRONICS CORP.

EM78870

8-BIT MICRO-CONTROLLER

Version 2.1

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Version History

Specification Revision History		
Version	Content	Release Date
EM78870		
1.0	Initial version	2001/02/09
1.1	1. Add LCD 24x72 option 2. Change STACK layers from 16 to 32	2001/07/12
1.3	1. Remove SPI 32.768kHz spec. 2. Update application circuit 3. Update LCD driver ability spec.	2001/08/08
1.4	1. Update feature description 2. Update operational register table list 3. Update application circuit 4. Update RE page1,IOCE page 2	2001/08/29
1.5	1.Modify DC electrical character	2002/5/29
2.0	1.ADD DED function	2002/6/1
2.1	Remove DED function	2002/6/30



User Application Note

1. ROM, OTP, ICE

ROM	OTP	ICE
EM78870	EM78P870	EM78808 ICE

2. Main Function Difference

	EM78870	EM78P870
RAM	2.5K x 8	4K x 8



I. General Description

The EM78870 is an 8-bit RISC type microprocessor with low power, high speed CMOS technology. Integrated onto a single chip are on-chip watchdog (WDT), RAM, ROM, programmable real time clock /counter, internal interrupt, power down mode, LCD driver, build-in KEY TONE clock generation, Programming Tone generators, Serial Peripheral Interface(SPI), comparator and tri-state I/O. The EM78870 provides a single chip solution to design a message_display.

II. Feature

CPU

Operating voltage range : 2.2V~5.5V(Normal mode), 2.0V~5.5V(Green mode)

32K×13 on chip Program ROM

2.5K×8 on chip data RAM

144 byte working register

Up to 51 bi-directional tri-state I/O ports (32 shared with LCD Segment pins)

IO with internal Pull high, wake-up and interrupt functions

STACK: 32 level stack for subroutine nesting

TCC: 8-bit real time clock/counter (TCC) with 8-bit prescaler

COUNTER1: 8-bit counter with 8-bit prescaler can be an interrupt source

COUNTER2: 8-bit counter with 8-bit prescaler can be an interrupt source

Watch Dog : Programmable free running on chip watchdog timer

CPU modes:

Mode	CPU status	Main clock	32.768kHz clock status
Sleep mode	Turn off	Turn off	Turn off
Idle mode	Turn off	Turn off	Turn on
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on

12 interrupt source : 8 external , 4 internal

Key Scan : Port key scan function up to 16x4 keys

Sub-Clock: 32.768kHz crystal

Main-clock: 3.5826MHz multiplied by 0.25, 0.5, 1 or 3 generated by internal PLL

Key tone output (shared with IO) : 4kHz, 2kHz, 1kHz

Comparator: 3-channel comparators, internal (16 level) or external reference voltage (shared with IO)

Serial Peripheral Interface (SPI) : Interrupt flag available for the read buffer full, Programmable baud rates of communication, Three-wire synchronous communication. (shared with IO)

Programmable Tone Generators

Operation Voltage 2.2V 5.5V

Programmable Tone1 and Tone2 generators

Independent single tone generation for Tone1 and Tone2

Mixed dual tone generation by Tone1 and Tone2 with 2dB difference

LCD (8x80, 9x80, 16x80, 24x72)

Maximum common driver pins : 16/24

Maximum segment driver pins : 80(SEG0..SEG79)/72(SEG8..SEG79)

Shared COM16 ~ COM23 pins with SEG0 ~ SEG7 pins

1/4 bias for 8, 9 and 16 common mode and 1/5 bias for 24 common mode

1/8, 1/9, 1/16, 1/24 duty

16 Level LCD contrast control (software)

Internal resistor circuit for LCD bias

Internal voltage follower for better display

Package type

128-pin QFP : EM78870AQ (POVD disable), EM78870BQ (POVD enable), EM78P870H



130-pin die

III. Application

Cordless phones or any telephone product with large LCD needed

IV. Pin Configuration

COM9	1	104	SEG18
COM8	2	103	SEG19
COM7	3	102	SEG20
COM6	4	101	SEG21
COM5	5	100	SEG22
COM4	6	99	SEG23
COM3	7	98	SEG24
COM2	8	97	SEG25
COM1	9	96	SEG26
COM0	10	95	SEG27
VC5	11	94	SEG28
VC4	12	93	SEG29
VC3	13	92	SEG30
VC2	14	91	SEG31
VC1	15	90	SEG32
XIN	16	89	SEG33
XOUT	17	88	SEG34
VDD	18	87	SEG35
AVDD	18	86	SEG36
PLLC	19	85	SEG37
tone	20	88	SEG38
AVSS	21	83	SEG39
GND	21	82	SEG40
TEST	22	81	SEG41
/RESET	23	80	SEG42
P70/INT0	24	79	SEG43
P71/INT0	25	78	SEG44
P72/INT0	26	77	SEG45
P73/INT0	27	76	SEG46
P74/INT1	28	75	SEG47
P75/INT1	29	74	SEG48/PB0
P76/INT1	30	73	SEG49/PB1
P77/INT2	31	72	SEG50/PB2
P60/SCK	32	71	SEG51/PB3
P61/SDO	33	70	SEG52/PB4
P62/SDI	34	69	SEG53/PB5
P63/CMP1	35	68	SEG54/PB6
P64/CMP2	36	67	SEG55/PB7
P65/CMP3	37	66	SEG56/PC0
P66	38	65	SEG57/PC1
P67/KTONE	39	64	SEG58/PC2
	40	63	
	41	62	
	42	61	
	43	60	
	44	59	
	45	58	
	46	57	
	47	56	
	48	55	
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	77	26	
	78	25	
	79	24	
	80	23	
	81	22	
	82	21	
	83	21	
	84	20	
	85	19	
	86	18	
	87	18	
	88	17	
	89	16	
	90	15	
	91	14	
	92	13	
	93	12	
	94	11	
	95	10	
	96	9	
	97	8	
	98	7	
	99	6	
	100	5	
	101	4	
	102	3	
	103	2	
	104	1	
	105		
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	127		
	128		

Fig.1.1 Pin assignment (128-pin QFP)

SEG17	107	106	SEG18
SEG16	108	105	SEG19
SEG15	109	104	SEG20
SEG14	110	103	SEG21
SEG13	111	102	SEG22
SEG12	112	101	SEG23
SEG11	113	100	SEG24
SEG10	114	99	SEG25
SEG9	115	98	SEG26
SEG8	116	97	SEG27
COM23/SEG7	117	96	SEG28
COM22/SEG6	118	95	SEG29
COM21/SEG5	119	94	SEG30
COM20/SEG4	120	93	SEG31
COM19/SEG3	121	92	SEG32
COM18/SEG2	122	91	SEG33
COM17/SEG1	123	90	SEG34
COM16/SEG0	124	89	SEG35
COM15	125	88	SEG36
COM14	126	87	SEG37
COM13	127	86	SEG38
COM12	128	85	SEG39
COM11	129	84	SEG40
COM10	130	83	SEG41
		82	SEG42
		81	SEG43
		80	SEG44
		79	SEG45
		78	SEG46
		77	SEG47
		76	SEG48/PB0
		75	SEG49/PB1
		74	SEG50/PB2
		73	SEG51/PB3
		72	SEG52/PB4
		71	SEG53/PB5
		70	SEG54/PB6
		69	SEG55/PB7
		68	SEG56/PC0
		67	SEG57/PC1
		66	SEG58/PC2
		65	SEG59/PC3
		64	SEG60/PC4
		63	SEG61/PC5
		62	SEG62/PC6
		61	SEG63/PC7
		60	SEG64/PC8
		59	SEG65/PC9
		58	SEG66/PC10
		57	SEG67/PC11
		56	SEG68/PC12
		55	SEG69/PC13
		54	SEG70/PC14
		53	SEG71/PC15
		52	SEG72/PC16
		51	SEG73/PC17
		50	SEG74/PC18
		49	SEG75/PC19
		48	SEG76/PC20
		47	SEG77/PC21
		46	SEG78/PC22
		45	SEG79/PC23
		44	SEG80/PC24
		43	SEG81/PC25
		42	SEG82/PC26
		41	SEG83/PC27
		40	SEG84/PC28
		39	SEG85/PC29
		38	SEG86/PC30
		37	SEG87/PC31
		36	SEG88/PC32
		35	SEG89/PC33
		34	SEG90/PC34
		33	SEG91/PC35
		32	SEG92/PC36
		31	SEG93/PC37
		30	SEG94/PC38
		29	SEG95/PC39
		28	SEG96/PC40
		27	SEG97/PC41
		26	SEG98/PC42
		25	SEG99/PC43
		24	SEG100/PC44
		23	SEG101/PC45
		22	SEG102/PC46
		21	SEG103/PC47
		20	SEG104/PC48
		19	SEG105/PC49
		18	SEG106/PC50
		17	SEG107/PC51
		16	SEG108/PC52
		15	SEG109/PC53
		14	SEG110/PC54
		13	SEG111/PC55
		12	SEG112/PC56
		11	SEG113/PC57
		10	SEG114/PC58
		9	SEG115/PC59
		8	SEG116/PC60
		7	SEG117/PC61
		6	SEG118/PC62
		5	SEG119/PC63
		4	SEG120/PC64
		3	SEG121/PC65
		2	SEG122/PC66
		1	SEG123/PC67
		0	SEG124/PC68
			SEG125/PC69
			SEG126/PC70
			SEG127/PC71
			SEG128/PC72
			SEG129/PC73
			SEG130/PC74
			SEG131/PC75
			SEG132/PC76
			SEG133/PC77
			SEG134/PC78
			SEG135/PC79
			SEG136/PC80
			SEG137/PC81
			SEG138/PC82
			SEG139/PC83

Fig.1.2 Pin assignment (130-pin die)

** This specification is subject to be changed without notice.*

V.Functional Block Diagram

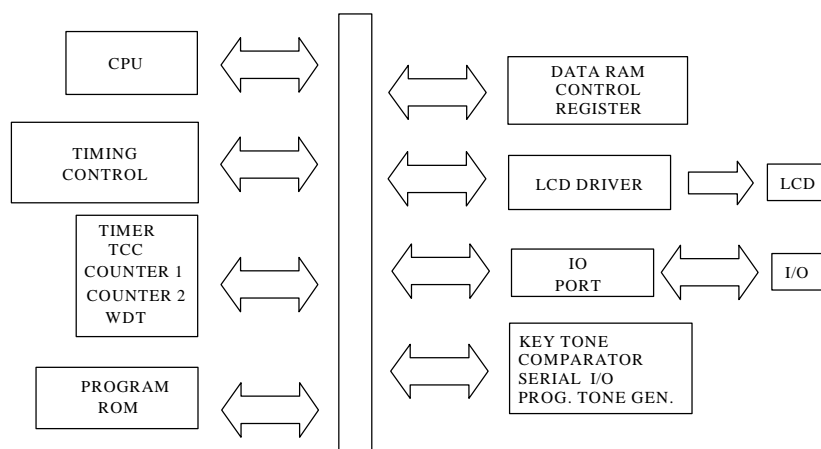


Fig.2 Block diagram1

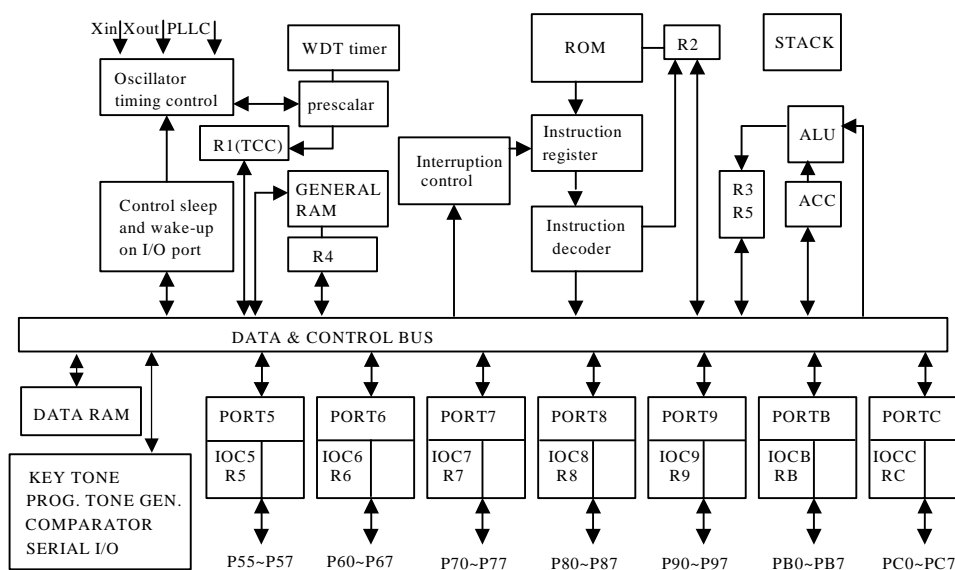


Fig.3 Block diagram2

VI. Pin Descriptions

PIN	I/O	DESCRIPTION
POWER		
VDD	POWER	Digital power
AVDD		Analog power
GND	POWER	Digital ground
AVSS		Analog ground
CLOCK		
XIN	I	Input pin for 32.768kHz oscillator
XOUT	O	Output pin for 32.768kHz oscillator
PLLC	I	Phase loop lock. Connect a capacitor 0.01u to 0.047u with GND.
LCD		
COM0..COM15	O	Common driver pins of LCD drivers
COM16..COM23	O (SEG0..SEG7)	COM16 to COM23 are shared with SEG0 to SEG7
SEG0..SEG7	O (COM16..COM23)	Segment driver pins of LCD drivers
SEG8...SEG47	O	SEG0 to SEG7 are shared with COM16 to COM23
SEG48..SEG55	O (I/O : PORTB)	SEG48 to SEG79 are shared with IO PORT
SEG56..SEG63	O (I/O : PORTC)	
SEG64..SEG71	O (I/O : PORT8)	
SEG72..SEG79	O (I/O : PORT9)	
VC1..VC5	I	Reference voltage input. Each one connect a capacitor (0.1u) with GND.
TONE, KTONE		
TONE	O	Programming tone output pin
KTONE	O (PORT67)	Key tone output. Shared with PORT67
SERIAL IO		
SCK	IO (PORT60)	Master : output pin, Slave : input pin. This pin is shared with PORT60.
SDO	O (PORT61)	Output pin for serial data transferring. This pin is shared with PORT61.
SDI	I (PORT62)	Input pin for receiving data. This pin shared with PORT62.
COMPARATOR		
CMP1	I (PORT63)	Comparator input pins. Shared with PORT63, PORT64 and PORT65.
CMP2	I (PORT64)	
CMP3	I (PORT65)	
IO		
P55 ~P57	I/O	PORT 5 can be INPUT or OUTPUT port each bit.
P60 ~P67	I/O	PORT 6 can be INPUT or OUTPUT port each bit. Internal pull high.
P70 ~ P77	I/O	PORT 7 can be INPUT or OUTPUT port each bit. Internal Pull high function. Auto key scan function. Interrupt function.
P80 ~ P87	I/O	PORT 8 can be INPUT or OUTPUT port each bit. Shared with LCD Segment signal.
P90 ~ P97	I/O	PORT 9 can be INPUT or OUTPUT port each bit. Shared with LCD Segment signal.
PB0 ~ PB7	I/O	PORT B can be INPUT or OUTPUT port each bit. Shared with LCD Segment signal.
PC0 ~ PC7	I/O	PORT C can be INPUT or OUTPUT port each bit. Shared with LCD Segment signal.
INT0	PORT70..73	Interrupt source which has the same interrupt flag. Any pin from PORT70 to PORT73 has a falling edge signal, it will generate a interruption.
INT1	PORT74..76	Interrupt source which has the same interrupt flag. Any pin from



		PORT74 to PORT76 has a falling edge signal, it will generate a interruption.
INT2	PORT77	Interrupt source. Once PORT77 has an edge triggering signal (controlled by CONT register), it will generate a interruption.
TEST	I	Test pin into test mode for factory test only. Connect it ground in application.
/RESET	I	Power Low reset

VII.Functional Descriptions

VII.1 Operational Registers

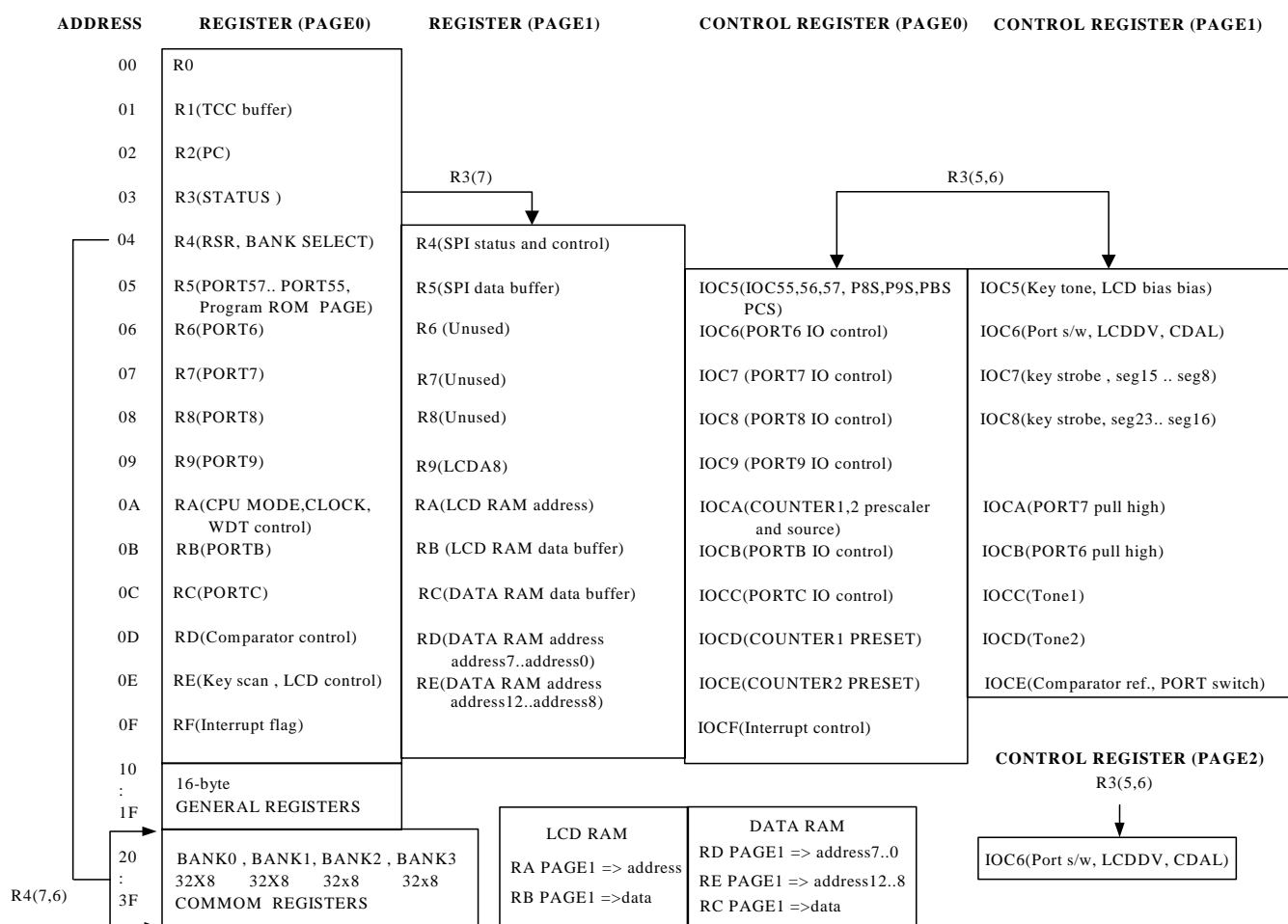


Fig.4 control register configuration

VII.2 Operational Register Table List

(1) Paged registers (R PAGE0, RPAGE1, IOC PAGE0, IOC PAGE1)

R0~R4 and RF are unpaged registers.

R PAGE0

Addr	Name	Bit	Function
00	R0		Indirect addressing register
01	R1		TCC
02	R2		Program counter
03	R3		Status, Page selection
	C	0	Carry flag
	DC	1	Auxiliary carry flag
	Z	2	Zero flag
	T	3	Time-out bit
	P	4	Power down bit
	IOCPAGE	5	Change IOC5 ~ IOCE to PAGE0/PAGE1

	IOC6P1S	6	Change IOC6 PAGE1 to option-A/option-B
	PAGE	7	Change R4 ~ RE to PAGE0/PAGE1
04	R4		RAM selection for common registers
	RSR0~RSR5	0~5	Indirect addressing for common registers R20 ~ R3F
	RB0~ RB1	6~7	Bank selection bits for common registers R20 ~ R3F
05	R5 PAGE0		PORT5 I/O data register, Program page selection
	PS0~PS4	0~4	Program page selection bits
	P55~P57	5~7	3-bit PORT5(5~7) I/O data register
06	R6 PAGE0		PORT6 I/O data register
	P60~P67	0~7	8-bit PORT6(0~7) I/O data register
07	R7 PAGE0		PORT7 I/O data register
	P70~P77	0~7	8-bit PORT7(0~7) I/O data register
08	R8 PAGE0		PORT8 I/O data register
	P80~P87	0~7	8-bit PORT8(0~7) I/O data register
09	R9 PAGE0		PORT9 I/O data register
	P90~P97	0~7	8-bit PORT9(0~7) I/O data register
0A	RA PAGE0		CPU power saving, PLL, Main clock selection, Watchdog timer
	WDTEN	0	Watchdog control bit
	1	1~2	Unused
	0	3	Unused
	CLK0~CLK1	4~5	Main clock selection bits
	PLLEN	6	PLL's power control bit which is CPU mode control register
	IDLE	7	SLEEP mode or IDLE mode selection after using "SLEEP"
0B	RB PAGE0		PORTB I/O data register
	PB0~PB7	0~7	8-bit PORTB(0~7) I/O data register
0C	RC PAGE0		PORTC I/O data register
	PC0~PC7	0~7	8-bit PORTC(0~7) I/O data register
0D	RD PAGE0		Comparator control
	CMP_B0~CMP_B3	0~3	Reference voltage selection of internal bias circuit for comparator
	CMPS0~CMPS1	4~5	Channel selection from CMP1 to CMP3 for comparator
	CMPFLAG	6	Comparator output flag
	CMPEN	7	Enable control bit of comparator
0E	RE PAGE0		Key scan, LCD control
	LCDM0~LCDM1	0~1	LCD common mode, bias select and COM/SEG switch control
	LCD0~LCD1	2~3	LCD operation function definition
	KEYSCAN	4	Key scan function enable control bit
	KEYSTRB	5	Key strobe enable control bit
	KEYCHK	6	Key check enable control bit
	1	7	Unused
0F	RF		Interrupt status register
	TCIF	0	Timer overflow interrupt flag for TCC
	CNT1	1	Timer overflow interrupt flag for COUNTER1
	CNT2	2	Timer overflow interrupt flag for COUNTER2
	INT0	3	Interrupt flag for external INT0 pin
	INT1	4	Interrupt flag for external INT1 pin
	INT2	5	Interrupt flag for external INT2 pin
	0	6	Unused

* This specification is subject to be changed without notice.

	RBF	7	Interrupt flag for SPI data complete
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R PAGE1

Addr	Name	Bit	Function
04	R4 PAGE1		SPI control register
	SBR0~SBR2	0~2	SPI baud rate selection bits
	SCES	3	SPI clock edge selection bit
	SE	4	SPI shift enable bit
	SRO	5	SPI read overflow bit
	SPIE	6	SPI enable bit
	RBF	7	SPI read buffer full flag
05	R5 PAGE1		SPI data buffer
	SPIB0~SPIB7	0~7	SPI data buffer
06	-		-
07	-		-
08	-		-
09	R9 PAGE1		LCD address MSB bit
	0	0~6	Unused
	LCDA8	7	MSB of LCD address for LCD RAM reading or writing
0A	RA PAGE1		LCD address
	LCDA0~LCDA7	0~7	LCD address for LCD RAM reading or writing
0B	RB PAGE1		LCD data buffer
	LCDD0~LCDD7	0~7	LCD data buffer for LCD RAM reading or writing
0C	RC PAGE1		
	RAMD0~RAMD7	0~7	Data RAM data buffer for RAM reading or writing
0D	RD PAGE1		Data RAM address0 ~ address7
	RAMA0~RAMA7	0~7	Data RAM address0 ~ address7 for RAM reading or writing
0E	RE PAGE1		Data RAM address8 ~ address11
	RAMA8~RAMA11	0~3	Data RAM address8 ~ address11 for RAM reading or writing
	0	5	Unused

IOC PAGE0

Addr	Name	Bit	Function
05	IOC5 PAGE0		PORT5 I/O control register, PORT switch
	P8SL	0	Switch low nibble I/O PORT8 or LCD segment output
	P8SH	1	Switch high nibble I/O PORT8 or LCD segment output
	P9SL	2	Switch low nibble I/O PORT9 or LCD segment output
	P9SH	3	Switch high nibble I/O PORT9 or LCD segment output
	0	4	Unused
	IOC55~IOC57	5~7	PORT5(5~7) I/O direction control register
06	IOC6 PAGE0		PORT6 I/O control register
	IOC60~IOC67	0~7	PORT6(0~7) I/O direction control register
07	IOC7 PAGE0		PORT7 I/O control register
	IOC70~IOC77	0~7	PORT7(0~7) I/O direction control register
08	IOC8 PAGE0		PORT8 I/O control register
	IOC80~IOC87	0~7	PORT8(0~7) I/O direction control register
09	IOC9 PAGE0		PORT9 I/O control register

	IOC90~IOC97	0~7	PORT9(0~7) I/O direction control register
0A	IOCA PAGE0		Counter1 and Counter2 clock and scale setting
	C1P0~C2P2	0~2	Counter1 scaling
	CNT1S	3	Counter1 clock source
	C2P0~C2P2	4~6	Counter2 scaling
	CNT2S	7	Counter2 clock source
0B	IOCB PAGE0		PORTB I/O control register
	IOCB0~IOCB7	0~7	PORTB(0~7) I/O direction control register
0C	IOCC PAGE0		PORTC I/O control register
	IOCC0~IOCC7	0~7	PORTC(0~7) I/O direction control register
0D	IOCD PAGE0		Counter1 data buffer
	CN10~CN17	0~7	Counter1 data buffer that user can read and write
0E	IOCE PAGE0		Counter2 data buffer
	CN20~CN27	0~7	Counter2 data buffer that user can read and write
0F	IOCF		Interrupt mask register
	TCIF	0	Interrupt enable bit for TCC
	CNT1	1	Interrupt enable bit for COUNTER1
	CNT2	2	Interrupt enable bit for COUNTER2
	INT0	3	Interrupt enable bit for external INT0 pin
	INT1	4	Interrupt enable bit for external INT1 pin
	INT2	5	Interrupt enable bit for external INT2 pin
	0	6	Unused
	RBF	7	Interrupt enable bit for SPI data complete

IOC PAGE1

Addr	Name	Bit	Function
05	IOC5 PAGE1		Key tone control, LCD bias control
	BIAS0~BIAS3	0~3	LCD operation voltage selection
	0	4	Unused
	KTS	5	Key tone output switch
	KT0~KT1	6~7	Key tone output frequency and its power control
06	IOC6 PAGE1		Empty
07	IOC7 PAGE1		Key strobe control register
	STRB8~STRB15	0~7	Key strobe control bits
08	IOC8 PAGE1		Key strobe control register
	STRB16~STRB23	0~7	Key strobe control bits
09	-		-
0A	IOCA PAGE1		PORT7 pull high control register
	PH70~PH77	0~7	PORT7(0~7) pull high control register
0B	IOCB PAGE1		PORT6 pull high control register
	PH60~PH67	0~7	PORT6(0~7) pull high control register
0C	IOCC PAGE1		TONE1 control register
	T10~T17	0~7	Tone generator1's frequency divider and power control
0D	IOCD PAGE1		TONE2 control register
	T20~T27	0~7	Tone generator2's frequency divider and power control
0E	IOCE PAGE1		Comparator reference voltage type, PORT switch
	0	0~3	Unused

	CMPIN1	4	Switch for controlling PORT63 IO PORT or a comparator input
	CMPIN1	5	Switch for controlling PORT64 IO PORT or a comparator input
	CMPIN1	6	Switch for controlling PORT65 IO PORT or a comparator input
	CMPREF	7	Switch for comparator reference voltage type

IOC PAGE 2

06	IOC6 PAGE2		PORT switch, LCD driving ability control
	0	0~2	Unused
	LCDDV0~LCDDV1	3~4	LCD driver's driving ability control
	PBS	5	Switch I/O PORTB or LCD segment output
	PCSL	6	Switch low nibble I/O PORTC or LCD segment output
	PCSH	7	Switch high nibble I/O PORTC or LCD segment output
0E	IOCE PAGE2		
	VRSEL	7	Reference voltage VR selection bit for Comparator

(2) Unpage registers (Common registers)

In addition to R0~R4 and RF, other unpagged registers are as list below.

Addr	Name	Bit	Function
10	R10		Common register
:	:	:	:
1F	R1F		Common register
20	R20		4 – bank common register
:	:	:	:
3F	R3F		4 – bank common register

(3) Unaddressable register

Name	Bit	Function
ACC		Accumulator : Internal data transfer and instruction operand holding
CONT		Control register
PSR0~PSR2	0~2	TCC/WDT prescaler bits
PAB	3	Prescaler assignment bit
-	4	(unused)
TS	5	TCC signal source
INT	6	INT enable flag
INT_EDGE	7	Interrupt edge type of P70

VII.3 Operational Register Detail Description

R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is useful as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

Example:

```
Mov  a,@0x20      ;store a address at R4 for indirect addressing
Mov  0x04,A
Mov  a,@0xAA      ;write data 0xAA to R20 at bank0 through R0
Mov  0x00,A
```

R1 (TCC)

TCC data buffer. Increased by 16.384kHz or by the instruction cycle clock (controlled by CONT register).
Written and read by the program as any other register.

R2 (Program Counter)

The structure is depicted in Fig. 5.

Generates $32K \times 13$ on-chip PROGRAM ROM addresses to the relative programming instruction codes.

"JMP" instruction allows the direct loading of the low 10 program counter bits.

"CALL" instruction loads the low 10 bits of the PC, PC+1, and then push into the stack.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.

"MOV R2,A" allows the loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0".

"ADD R2,A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits are cleared to "0".

"TBL" allows a relative address be added to the current PC, and contents of the ninth and tenth bits don't change. The most significant bit (A10~A14) will be loaded with the content of bit PS0~PS3 in the status register (R5) upon the execution of a "JMP", "CALL", "ADD R2,A", or "MOV R2,A" instruction.

If a interrupt trigger, PROGRAM ROM will jump to address8 at page0. The CPU will store ACC,R3 status and R5 PAGE automatically, it will restore after instruction RETI.

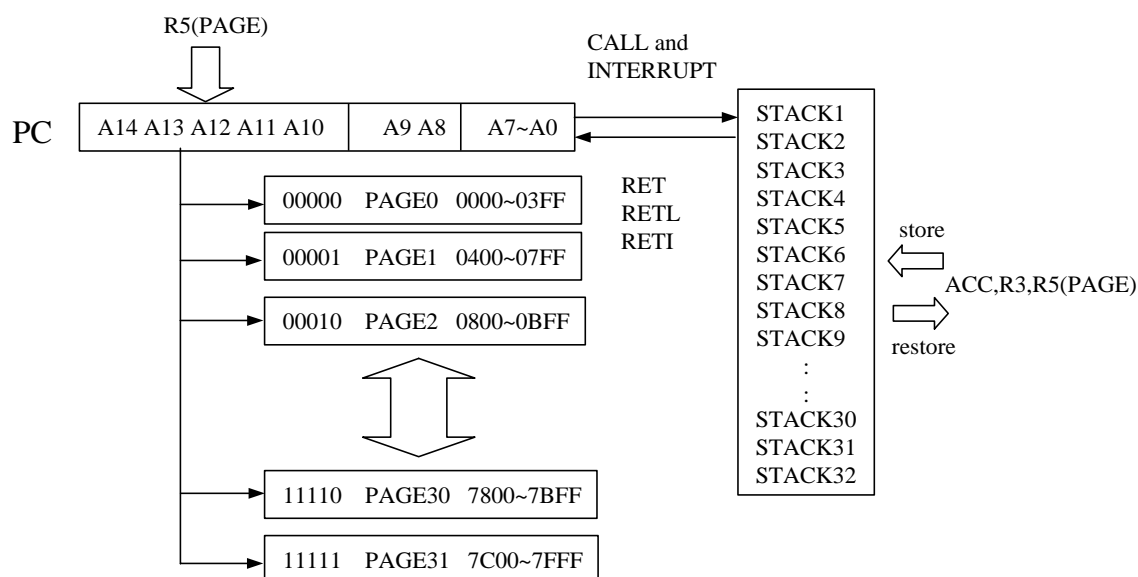


Fig.5 Program counter organization

R3 (Status Register)

7	6	5	4	3	2	1	0
PAGE	IOC6P1S	IOCPAGE	P	T	Z	DC	C

Bit 0 (C) : Carry flag

Bit 1 (DC) : Auxiliary carry flag

Bit 2 (Z) : Zero flag

Bit 3 (P) : Power down bit.

Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 4 (T) : Time-out bit.

Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

EVENT	T	P	REMARK
WDT wake up from sleep mode	0	0	
WDT time out (not sleep mode)	0	1	
/RESET wake up from sleep	1	0	
Power up	1	1	
Low pulse on /RESET	x	X	x : don't care

Bit 5(IOC5PAGE) : change IOC5 ~ IOCE to another page

Please refer to Fig.4 control register configuration for details.

0/1 → page0 / page1

Bit 6(IOC6P1S) : change IOC6 PAGE1 to another option register

Please refer to Fig.4 control register configuration for details.

0/1 → page1 option-A/page1 option-B

Bit 7(PAGE) : change R4 ~ RE to another page

Please refer to Fig.4 control register configuration for details.

0/1 → page0 / page1

R4 (RAM selection for common registers R20 ~ R3F, SPI control)

PAGE0 (RAM selection register)

7	6	5	4	3	2	1	0
RB1	RB0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0

Bit 0 ~ Bit 5 (RSR0 ~ RSR5) : Indirect addressing for common registers R20 ~ R3F

RSR bits are used to select up to 32 registers (R20 to R3F) in the indirect addressing mode.

Bit 6 ~ Bit 7 (RB0 ~ RB1) : Bank selection bits for common registers R20 ~ R3F

These selection bits are used to determine which bank is activated among the 4 banks for 32 register (R20 to R3F)..

Please refer to Fig.4 control register configuration for details.

PAGE1 (SPI control register)

7	6	5	4	3	2	1	0
RBF	SPIE	SRO	SE	SCES	SBR2	SBR1	SBR0

Fig. 6 shows how SPI to communicate with other device by SPI module. If SPI is a master controller, it sends clock through the SCK pin. An 8-bit data is transmitted and received at the same time. If SPI, however, is defined as a slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted on a basis of both the clock rate and the selected edge.

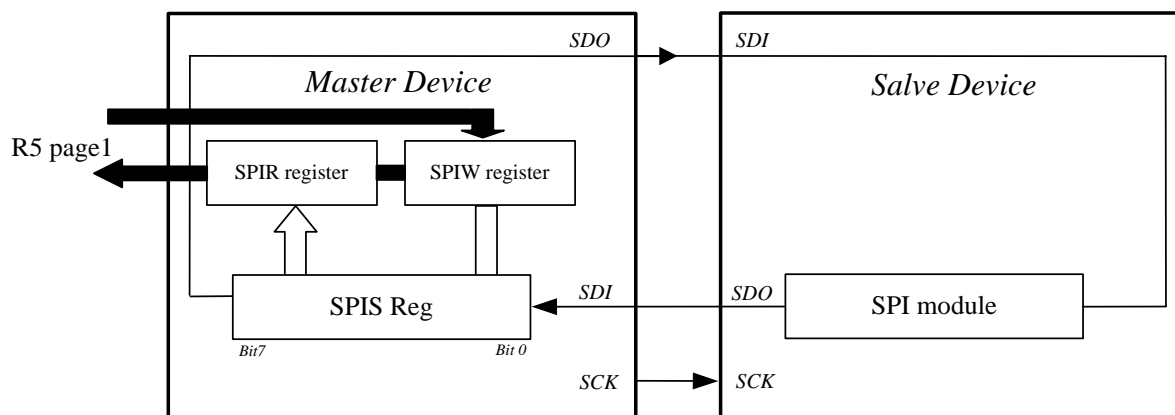


Fig.6 Single SPI Master / Slave Communication

Bit 0 ~ Bit 2 (SBR0 ~ SBR2) : SPI baud rate selection bits

SBRs2(Bit 2)	SBRs1(Bit 1)	SBRs0(Bit 0)	Mode	Baud rate
0	0	0	Master	Fsco
0	0	1	Master	Fsco/2
0	1	0	Master	Fsco/4
0	1	1	Master	Fsco/8
1	0	0	Master	Fsco/16
1	0	1	Master	Fsco/32
1	1	0	Slave	
1	1	1	x	x

<Note> F_{sco} = CPU instruction clock

For example :

If PLL enable and RA PAGE0 (Bit5, Bit4)=(1,1), instruction clock is $3.58\text{MHz}/2 \rightarrow F_{\text{SCO}}=3.5862\text{MHz}/2$

If PLL enable and RA PAGE0 (Bit5, Bit4)=(0,0), instruction clock is $0.895\text{MHz}/2 \rightarrow F_{\text{SCO}}=0.895\text{MHz}/2$

If PLL disable, instruction clock is $32.768\text{kHz}/2 \rightarrow F_{\text{SCO}}=32.768\text{kHz}/2$.

Bit 3 (SCES) : SPI clock edge selection bit

1 → Data shifts out on falling edge, and shifts in on rising edge. Data is hold during the high level.

0 → Data shifts out on rising edge, and shifts in on falling edge. Data is hold during the low level.

Bit 4 (SE) : SPI shift enable bit

1 → Start to shift, and keep on 1 while the current byte is still being transmitted.

0 → Reset as soon as the shifting is complete, and the next byte is ready to shift.

<Note> This bit has to be reset in software.

Bit 5 (SRO) : SPI read overflow bit

1 ➔ A new data is received while the previous data is still being hold in the SPIB register. In this situation, the data in SPIB register will be destroyed. To avoid setting this bit, users had better to read SPIB register even if the transmission is implemented only.

0 \Rightarrow No overflow

<Note> This can only occur in slave mode.

Bit 6 (SPIE) : SPI enable bit

1 ➔ Enable SPI mode

0 ➔ Disable SPI mode

Bit 7 (RBF) : SPI read buffer full flag

1 ➔ Receive is finished, SPIB is full.

0 ➔ Receive is not finish yet, SPIB is empty.

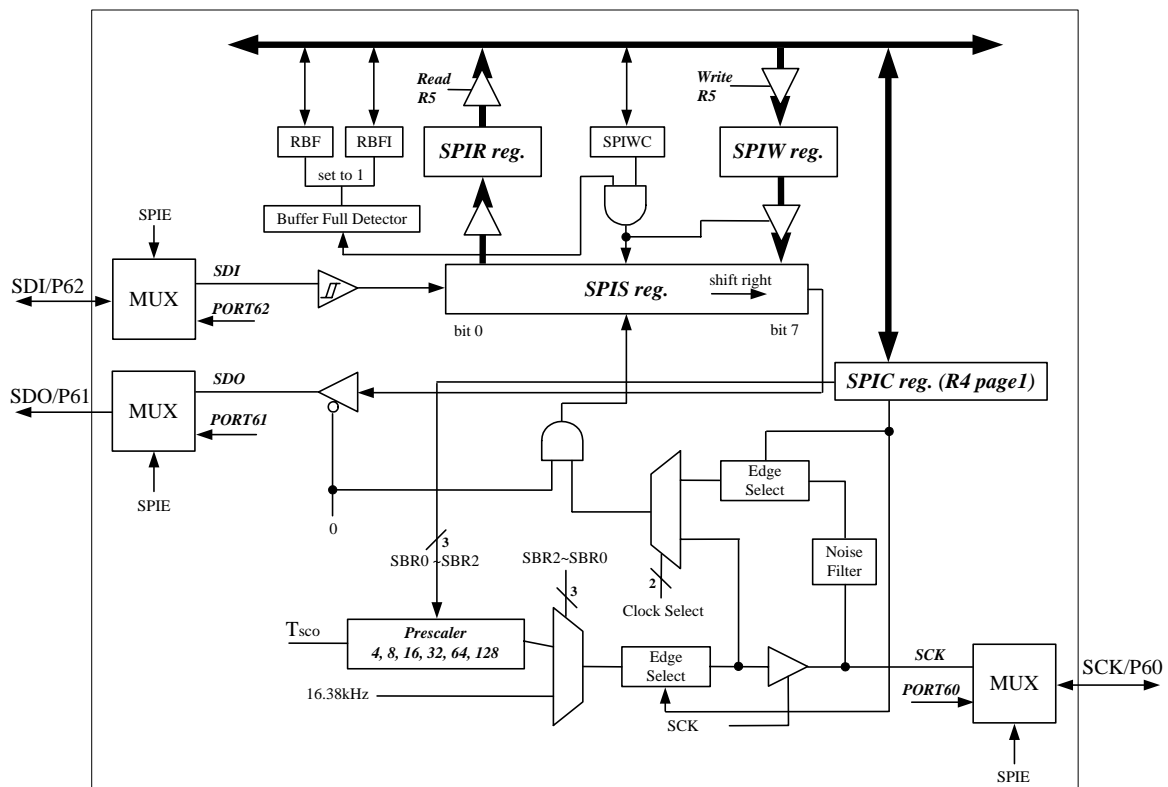


Fig.7 SPI structure

SPIC reg. : SPI control register

SDO/P61 : Serial data out

SDI/P62 : Serial data in

SCK/P60 : Serial clock.

RBF : Set by buffer full detector, and reset in software.

RBF : Interrupt flag. Set by buffer full detector, and reset in software.

Buffer Full Detector : Sets to 1, while an 8-bit shifting is complete.

SE : Loads the data in SPIW register, and begin to shift

SPIE : SPI control register

SPIS reg. : Shifting byte out and in. The MSB will be shifted first. Both the SPIS register and the SPIW register are loaded at the same time. Once data being written to, SPIS starts transmission / reception. The received data will be moved to the SPIR register, as the shifting of the 8-bit data is complete. The RBF (Read Buffer Full) flag and the RBFI(Read Buffer Full Interrupt) flag are set.

SPIR reg. : Read buffer. The buffer will be updated as the 8-bit shifting is complete. The data must be read before the next reception is finished. The RBF flag is cleared as the SPIR register read.

SPIW reg. : Write buffer. The buffer will deny any write until the 8-bit shifting is complete. The SE bit will be kept in 1 if the communication is still under going. This flag must be cleared as the shifting is finished. Users can determine if the next write attempt is available.

SBR2 ~ SBR0: Programming the clock frequency/rates and sources.

Clock select : Selecting either the internal instruction clock or the external 16.338KHz clock as the shifting clock.

Edge Select : Selecting the appropriate clock edges by programming the SCES bit

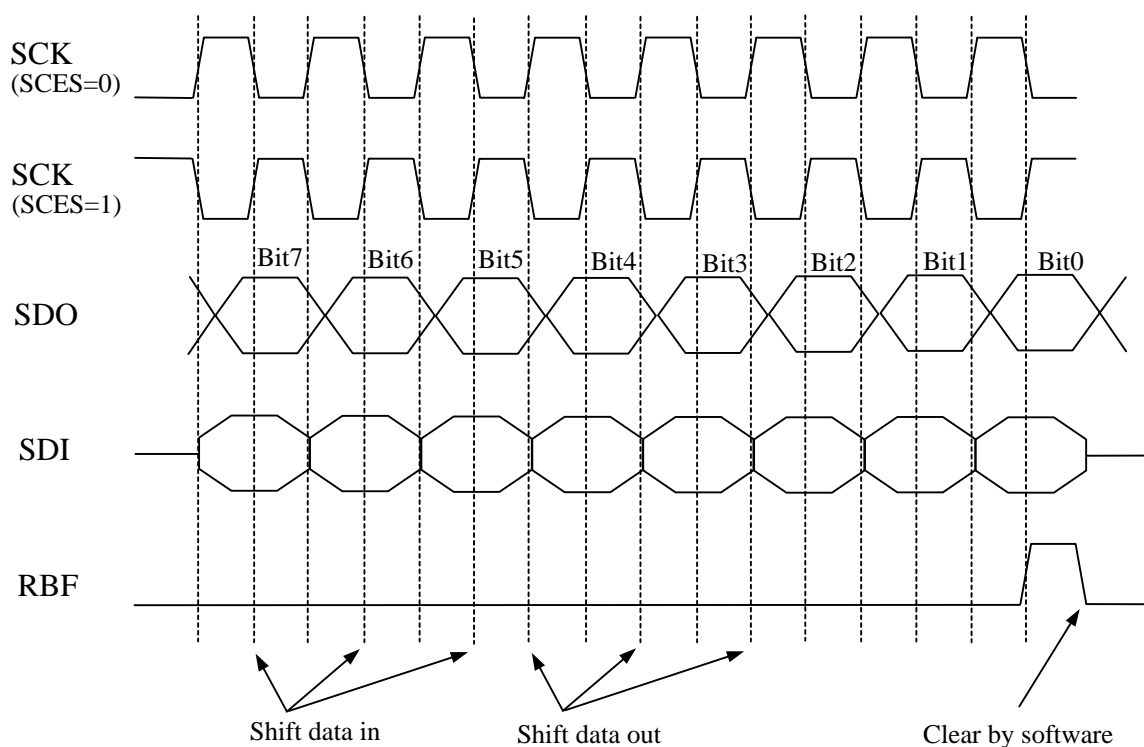


Fig.8 SPI timing

R5 (PORT5 I/O data, Program page selection, SPI data)

PAGE0 (PORT5 I/O data register, Program page register)

7	6	5	4	3	2	1	0
R57	R56	R55	PS4	PS3	PS2	PS1	PS0

Bit 0 ~ Bit 4 (PS0 ~ PS4) : Program page selection bits

PS4	PS3	PS2	PS1	PS0	Program memory page (Address)
0	0	0	0	0	Page 0
0	0	0	0	1	Page 1
0	0	0	1	0	Page 2
0	0	0	1	1	Page 3
:	:	:	:	:	:
:	:	:	:	:	:
1	1	1	1	0	Page 30
1	1	1	1	1	Page 31

User can use PAGE instruction to change page to maintain program page by user. Otherwise, user can use far jump (FJMP) or far call (FCALL) instructions to program user's code. And the program page is maintained by EMC's compiler. It will change user's program by inserting instructions within program.

Bit 5 ~ Bit 7 (P55 ~ P57) : 3-bit PORT5(5~7) I/O data register

User can use IOC register to define input or output each bit.

PAGE1 (SPI data buffer)

7	6	5	4	3	2	1	0
SPIB7	SPIB6	SPIB5	SPIB4	SPIB3	SPIB2	SPIB1	SPIB0

Bit 0 ~ Bit 7 (SPIB0 ~ SPIB7) : SPI data buffer

If you write data to this register, the data will write to SPIW register. If you read this data, it will read the data from SPIR register. Please refer to figure7

R6 (PORT6 I/O data)

PAGE0 (PORT6 I/O data register)

7	6	5	4	3	2	1	0
P67	P66	P65	P64	P63	P62	P61	P60

Bit 0 ~ Bit 8 (P60 ~ P67) : 8-bit PORT6(0~7) I/O data register

User can use IOC register to define input or output each bit.

R7 (PORT7 I/O data)

PAGE0 (PORT7 I/O data register)

7	6	5	4	3	2	1	0
P77	P76	P75	P74	P73	P72	P71	P70

Bit 0 ~ Bit 7 (P70 ~ P77) : 8-bit PORT7(0~7) I/O data register

User can use IOC register to define input or output each bit.

R8 (PORT8 I/O data)

PAGE0 (PORT8 I/O data register)

7	6	5	4	3	2	1	0
P87	P86	P85	P84	P83	P82	P81	P80

Bit 0 ~ Bit 7 (P80 ~ P87) : 8-bit PORT8(0~7) I/O data register

User can use IOC register to define input or output each bit.

R9 (PORT9 I/O data, extra LCD address bit)

PAGE0 (PORT9 I/O data register)

7	6	5	4	3	2	1	0
P97	P96	P95	P94	P93	P92	P91	P90

Bit 0 ~ Bit 7 (P90 ~ P97) : 8-bit PORT9(0~7) I/O data register

User can use IOC register to define input or output each bit.

PAGE1 (LCD address MSB bit)

7	6	5	4	3	2	1	0
LCDA8	0	0	0	0	0	0	0

Bit 0 ~ Bit6 = 0 : unused

Bit 7 (LCDA8) : MSB of LCD address for LCD RAM reading or writing

Other LCD address bits LCDA7 ~ LCDA0 are set from RA PAGE1 Bit 7 ~ Bit 0.

For LCD address access over 0xFFH, set this bit to "1"; otherwise set this bit to "0".

RA (CPU power saving, PLL, Main clock selection, Watchdog timer, LCD address)

PAGE0 (CPU power saving bit, PLL, Main clock selection bits, Watchdog timer enable bit)

7	6	5	4	3	2	1	0
IDLE	PLLEN	CLK1	CLK0	0	1	1	WDTEN

Bit 0 (WDTEN) : Watch dog control register

User can use WDTC instruction to clear watch dog counter. The counter 's clock source is 32768/2 Hz. If the prescaler assigns to TCC. Watch dog will time out by $(1/32768) * 2 * 256 = 15.616\text{ms}$. If the prescaler assigns to WDT, the time of time out will be more times depending on the ratio of prescaler.

0/1 → disable/enable

Bit 1~ Bit 2 = 1 : unused

Bit 3 = 0 : unused

Bit 4 ~ Bit 5 (CLK0 ~ CLK1) : Main clock selection bits

User can choose different frequency of main clock by CLK1 and CLK2. All the clock selection is list below.

PLLEN	CLK1	CLK0	Sub clock	MAIN clock	CPU clock
1	0	0	32.768kHz	895.658kHz	895.658kHz (Normal mode)
1	0	1	32.768kHz	1.7913MHz	1.7913MHz (Normal mode)
1	1	0	32.768kHz	10.7479MHz	10.7479MHz (Normal mode)
1	1	1	32.768kHz	3.5826MHz	3.5826MHz (Normal mode)
0	Don't care	don't care	32.768kHz	don't care	32.768kHz (Green mode)
0	Don't care	don't care	32.768kHz	don't care	32.768kHz (Green mode)
0	Don't care	don't care	32.768kHz	don't care	32.768kHz (Green mode)
0	Don't care	don't care	32.768kHz	don't care	32.768kHz (Green mode)

Bit 6 (PLLEN) : PLL enable control bit

It is CPU mode control register. If PLL is enabled, CPU will operate at normal mode (high frequency, main clock); otherwise, it will run at green mode (low frequency, 32768 Hz).

0/1 → disable/enable

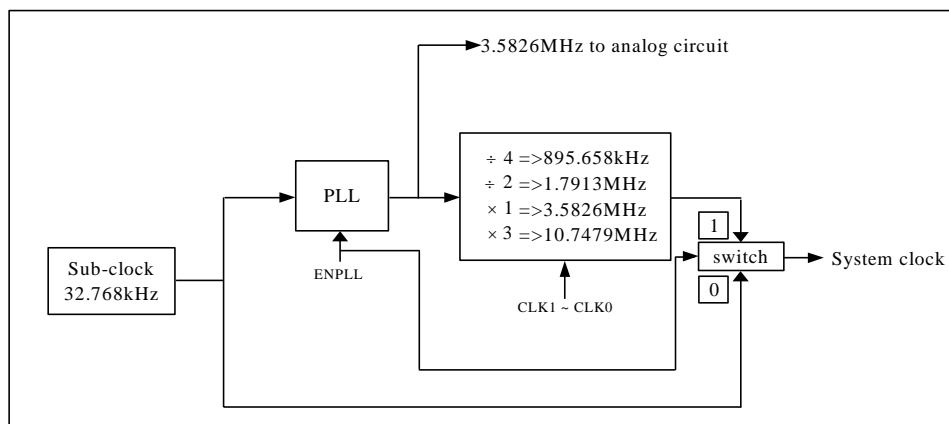


Fig.9. The relation between 32.768kHz and PLL

Bit 7(IDLE) : Power saving mode control register

When PLL is disabled, user can set this bit after using "SLEP" instruction for SLEEP mode or IDLE mode selection

0/1 → SLEEP mode/IDLE mode.

This bit will decide SLEP instruction which mode to go.

The status after wake-up and the wake-up sources list as the table below.

Wakeup signal	SLEEP mode	IDLE mode	GREEN mode	NORMAL mode
	RA(7,6)=(0,0) + SLEP	RA(7,6)=(1,0) + SLEP	RA(7,6)=(x,0) no SLEP	RA(7,6)=(x,1) no SLEP
TCC time out IOCF bit0=1 And "ENI"	No function	(1)Wake-up (2)Interrupt (jump to address 8 at page0) (3)after RETI instruction, jump to SLEP Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
COUNTER1 time out IOCF bit1=1 And "ENI"	No function	(1)Wake-up (2)Interrupt (jump to address 8 at page0) (3)after RETI instruction, jump to SLEP Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
COUNTER2 time out IOCF bit2=1 And "ENI"	No function	(1)Wake-up (2)Interrupt (jump to address 8 at page0) (3)after RETI instruction, jump to SLEP Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
WDT time out	RESET and Jump to address 0	(1)Wake-up (2)Next instruction	RESET and Jump to address 0	RESET and Jump to address 0

PORT7 IOCF bit3 or bit4 or bit5 =1 And "ENI"	RESET and Jump to address 0	(1)Wake-up (2)Interrupt (jump to address 8 at page0) (3)after RETI instruction, jump to SLEP Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
---	--------------------------------	--	--	--

<Note> PORT70 ~ PORT73 's wakeup function is controlled by IOCF bit3 and ENI instruction. They are falling edge trigger.

PORT74 ~ PORT76 's wakeup function is controlled by IOCF bit4 and ENI instruction. They are falling edge trigger.

PORT77 's wakeup function is controlled by IOCF bit5 and ENI instruction. It's falling edge or rising edge trigger (controlled by CONT register).

PAGE1 (LCD address)

7	6	5	4	3	2	1	0
LCDA7	LCDA6	LCDA5	LCDA 4	LCDA 3	LCDA 2	LCDA 1	LCDA 0

Bit 0 ~ Bit 7 (LCDA0 ~ LCDA7) : LCD address for LCD RAM reading or writing

The data in the LCD RAM correspond to the COMMON and SEGMENT signals as the table .

COM23 ~ COM16 (set R9 PAGE1 bit7=1)	COM15 ~COM8 (set R9 PAGE1 bit7=0)	COM7 ~ COM0 (set R9 PAGE1 bit7=0)	
Address 100H	Address 80H	Address 00H	SEG0
Address 101H	Address 81H	Address 01H	SEG1
Address 102H	Address 82H	Address 02H	SEG1
:	:	:	:
:	:	:	:
:	:	:	:
Address 14EH	Address CEH	Address 4EH	SEG78
Address 14FH	Address CFH	Address 4FH	SEG79
Address 150H	Address D0H	Address 50H	Empty
:	:	:	:
Address 17FH	Address FFH	Address 7FH	Empty

RB (PORTB I/O data, LCD data)

PAGE0 (PORTB I/O data register)

7	6	5	4	3	2	1	0
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0

Bit 0 ~ Bit 7 (PB0 ~ PB7) : 8-bit PORTB(0~7) I/O data register

User can use IOC register to define input or output each bit.

PAGE1 (LCD data buffer)

7	6	5	4	3	2	1	0
LCDD7	LCDD6	LCDD5	LCDD4	LCDD3	LCDD2	LCDD1	LCDD0

Bit 0 ~ Bit 7 (LCDD0 ~ LCDD7) : LCD data buffer for LCD RAM reading or writing

Ex.

```

MOV      A,@0
MOV      R9_PAGE1,A
MOV      RA_PAGE1,A          ;ADDRESS
MOV      A,@0XAA
MOV      RB_PAGE1,A          ;WRITE DATA 0XAA TO LCD RAM
MOV      A,RB_PAGE1          ;READ DATA FROM LCD RAM
:
```

RC (PORTC I/O data, Data RAM data)

PAGE0 (PORTC I/O data register)

7	6	5	4	3	2	1	0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

Bit 0 ~ Bit 7 (PC0 ~ PC7) : 8-bit PORTC(0~7) I/O data register

User can use IOC register to define input or output each bit.

PAGE1 (Data RAM data buffer)

7	6	5	4	3	2	1	0
RAMD7	DRAMD6	RAMD5	RAMD4	RAMD3	RAMD2	RAMD1	RAMD0

Bit 0 ~ Bit 7 (RAMD0 ~ RAMD7) : Data RAM data buffer for RAM reading or writing.

Ex.

```
MOV      A,@1
MOV      RD_PAGE1,A
MOV      A,@0
MOV      RE_PAGE1,A
MOV      A,@0x55
MOV      RC_PAGE1,A           ;write data 0x55 to DATA RAM which address is "0001".
MOV      A,RC_PAGE1          ;read data
```

:

RD (Comparator control, Data RAM address(0 ~ 7))

PAGE0 (Comparator control bits)

7	6	5	4	3	2	1	0
CMPEN	CMPFLAG	CMPS1	CMPS0	CMP_B3	CMP_B2	CMP_B1	CMP_B0

If user define PORT63 , PORT64 or PORT65 (by CMPIN1, CMPIN2, CMPIN3 at IOCE page1) as a comparator input or PORT6. User can use this register to control comparator's function.

Bit 0 ~ Bit 3 (CMP_B0 ~ CMP_B3) : Reference voltage selection of internal bias circuit for comparator.

Reference voltage for comparator = $VDD \times (n + 0.5) / 16$, $n = 0$ to 15

Bit 4 ~ Bit 5 (CMPS0 ~ CMPS1) : Channel selection from CMP1 to CMP3 for comparator

CMPS1	CMPS0	Input
0	0	CMP1
0	1	CMP2
1	0	CMP3
1	1	Reserved

Bit 6 (CMPFLAG) : Comparator output flag

0 → Input voltage < reference voltage

1 → Input voltage > reference voltage

Bit 7 (CMPEN) : Enable control bit of comparator.

0/1 → disable/enable

The relation between these registers shown in Fig.10.

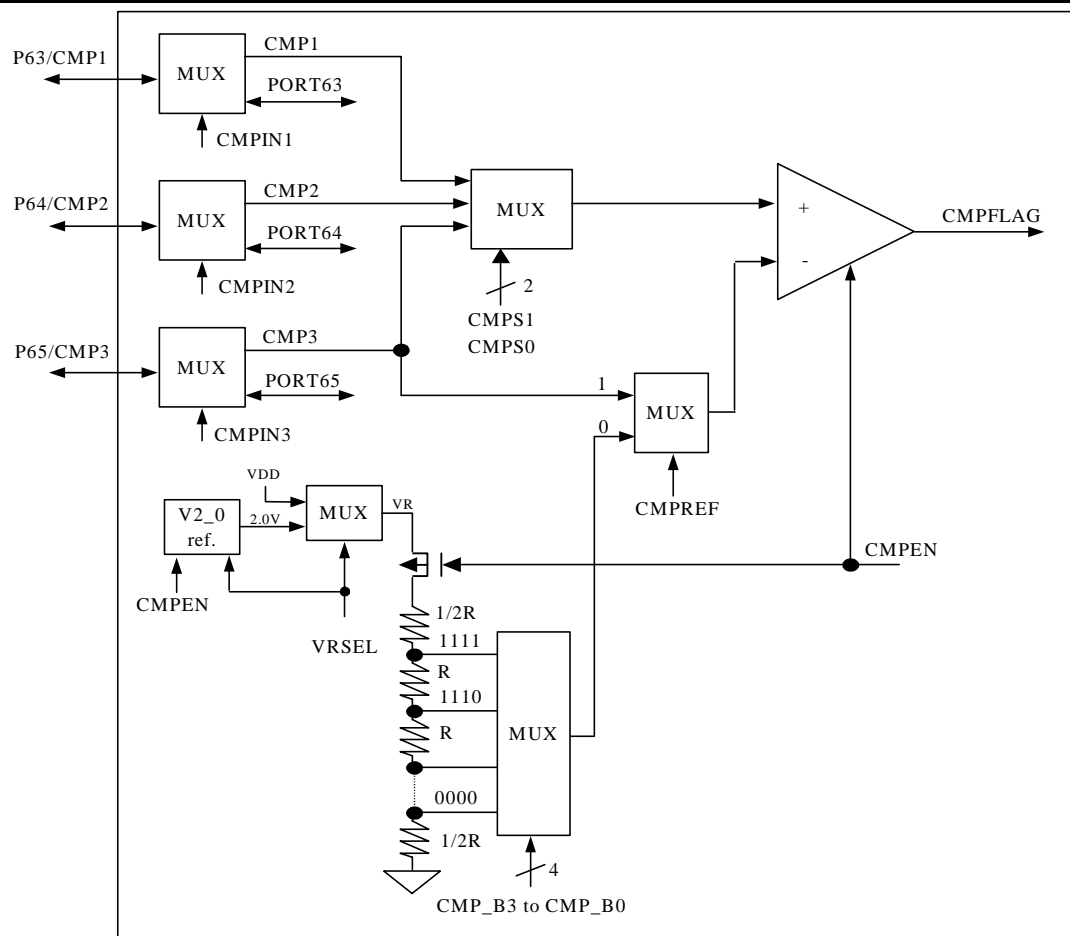


Fig.10. Comparator circuit

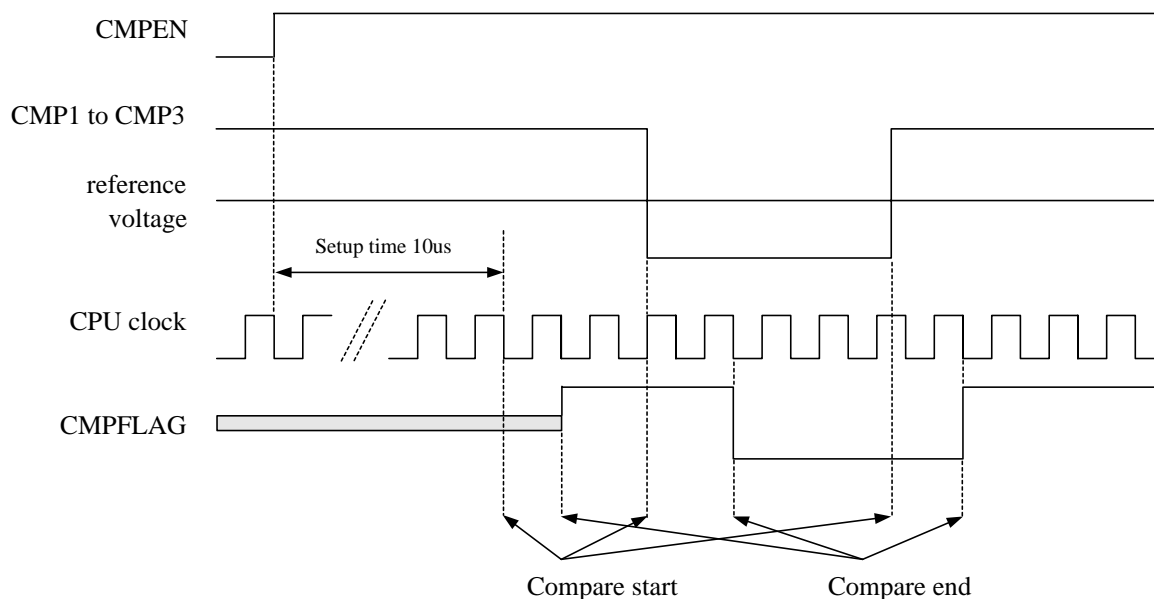


Fig.11. Comparator timing

PAGE1 (Data RAM address0 ~ address7)

7	6	5	4	3	2	1	0
RAMA7	RAMA6	RAMA5	RAMA4	RAMA3	RAMA2	RAMA1	RAMA0

Bit 0 ~ Bit 7 (RAMA0 ~ RAMA7) : Data RAM address (address0 to address7) for RAM reading or writing

RE (Key scan, LCD control, Data RAM addresss(8 ~ 10))

PAGE0 (Key scan control, LCD control)

7	6	5	4	3	2	1	0
1	KEYCHK	KEYSTRB	KEYSCAN	LCD1	LCD0	LCDM1	LCDM0

Bit 0 ~ Bit 1 (LCDM0 ~ LCDM1) : LCD common mode, bias select and COM/SEG switch control bits

LCDM1, LCDM0	COM output mode	LCD bias	COM/SEG switch
0,0	16 common	1/4 bias	SEG0 ~ SEG7 select
0,1	9 common	1/4 bias	SEG0 ~ SEG7 select
1,0	8 common	1/4 bias	SEG0 ~ SEG7 select
1,1	24 common	1/5 bias	COM16 ~ COM23 select

<Note> When 8, 9 and 16 LCD common mode is set, COM16/SEG0 pin ~ COM23/SEG7 pin are also set to SEG0 ~ SEG7 and LCD bias is 1/4 bias. When 24 LCD common mode is set, COM16/SEG0 pin ~ COM23/SEG7 pin are also set to COM16 ~ COM23 and LCD bias is 1/5 bias.

Bit 2 ~ Bit 3 (LCD0 ~ LCD1) : LCD operation function definition.

LCD1, LCD0	LCD operation
0,0	Disable
0,1	Blanking
1,0	Reserved
1,1	LCD enable

<Note> Key strobe and Key check functions should be normal operating whenever LCD is enabled or disabled.

The controller can drive LCD directly. LCD block is made up of LCD driver, display RAM, segment output pins, common output pins and LCD operating bias pins.

Duty, the number of segment, the number of common and frame frequency are determined by LCD mode register RE PAGE0 Bit 0~ Bit 1.

When 8, 9 or 16 LCD commons are used, LCD operating bias pins VC1, VC2, VC4 and VC5 need to be connected 0.1uF capacitors to the ground (VC3 is not necessary). When 24 LCD common is used, all LCD operating bias pins VC1 ~ VC5 need to be connected 0.1uF capacitors to the ground.

LCD driver can be controlled as different driving ability (refer to IOC6 PAGE1 Option-B register).

The basic structure contains a timing control which uses the basic frequency 32.768kHz to generate the proper timing for different duty and display access. RE PAGE1 register is a command register for LCD driver and display. The LCD display (disable, enable, blanking) is controlled by RE PAGE0 Bit 2 ~ Bit 3 and the driving duty is decided by RE PAGE Bit 0 ~ Bit 2. LCD display data is stored in data RAM which address and data access controlled by registers R9, RA PAGE1 and RB PAGE1.

User can regulate the contrast of LCD display by IOC5 PAGE1 (BIAS3..BIAS0). Up to 16 levels contrast is convenient for better display. And the internal voltage follower can afford large driving source.

COM signal : The number of COM pins varies according to the duty cycle used, as following:

in 1/8 duty mode COM8 ~ COM15 must be open.

In 1/9 duty mode COM9~ COM15 must be open

in 1/16 duty mode COM0 ~ COM15 pins must be used.

in 1/24 duty mode COM0 ~ COM23 pins must be used.

duty	COM0 ~ COM7	COM8	COM9	..	COM15	COM15 ~ COM23
1/8	o	x	x	..	x	x
1/9	o	o	x	..	x	x
1/16	o	o	o	..	o	x
1/24	o	o	o	..	o	o

x : open, o : select

SEG signal: The segment signal pins are connected to the corresponding display RAM. The high byte to the low byte Bit 0 ~ Bit 7 are correlated to COM0 ~ COM23 respectively. When a bit of display RAM is 1, a select signal is sent to the corresponding segment pin, and when the bit is 0, a non-select signal is sent to the corresponding segment pin.

Bit 4 (KEYSCAN) : Key scan function enable control bit

0/1 → disable/enable

If you enable key scan function LCD waveform will have a small pulse within a period like Fig.12.

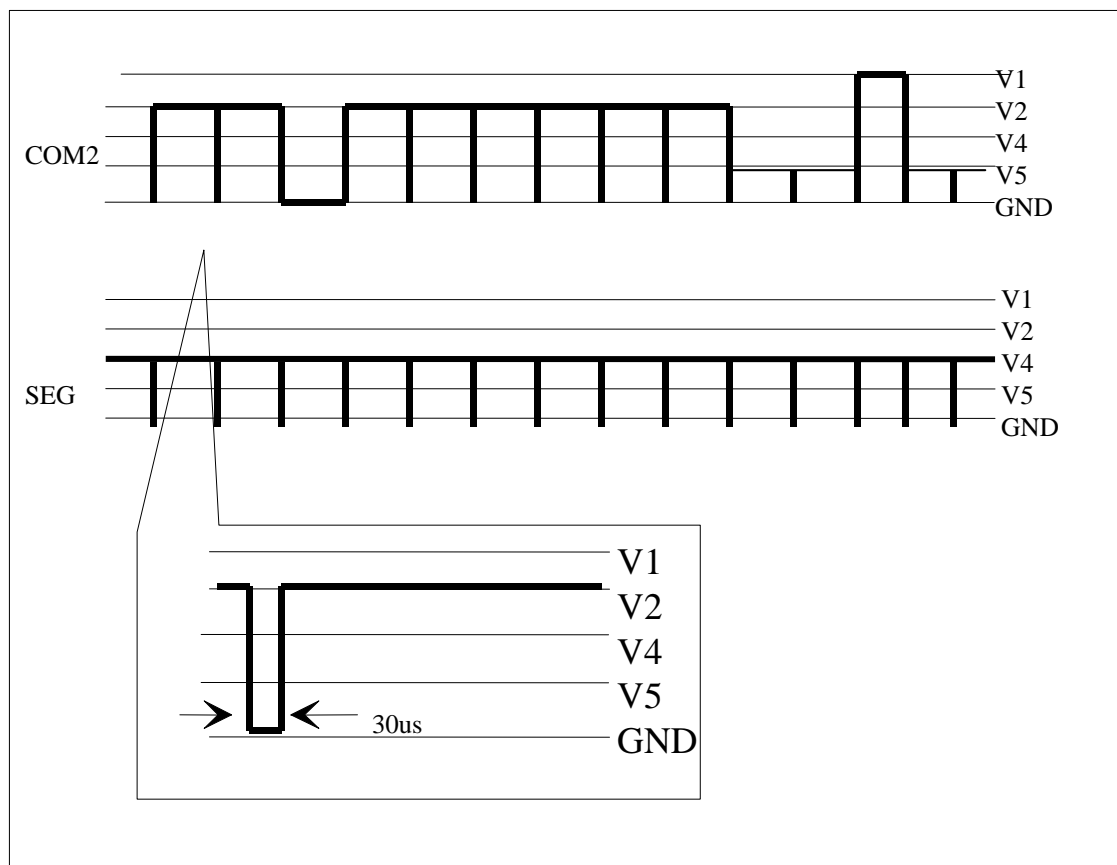


Fig.12. key scan waveform for 1/8, 1/9, 1/16 duty

Bit 5 (KEYSTRB) : Key strobe enable control bit

0/1 → disable/enable

key strobe signal , if you set this bit , segment will switch to strobe signal temporally and output zero signal (one instruction long) one by one from segment 8 to segment 23. During one segment strobe time, CPU will check port7(0:3) equal to "1111" or not. If not, CPU will latch a zero at IOC7 PAGE1 and IOC8 PAGE1 one by one depends on which segment strobe.

After strobe, this bit will be cleared . Fig.13 is key strobe signal.

STROBE	REGISTER															
	IOC7(0)	IOC7(1)	IOC7(2)	IOC7(3)	IOC7(4)	IOC7(5)	IOC7(6)	IOC7(7)	IOC8(0)	IOC8(1)	IOC8(2)	IOC8(3)	IOC8(4)	IOC8(5)	IOC8(6)	IOC8(7)
SEG8	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
SEG9	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
SEG10	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
SEG11	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
SEG12	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
SEG13	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
SEG14	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
SEG15	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
SEG16	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
SEG17	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
SEG18	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
SEG19	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
SEG20	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
SEG21	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
SEG22	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
SEG23	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Fig.13 key strobe signal

Bit 6 (KEYCHK) : Key check enable control bit

0 → disable key check function.

1 → enable key check function. SEG8 to SEG23 will keep low level.

Figure 14 is relationship between KEYSKAN, KEYSTROBE , KETCHECK and segments.

And figure 16 is key scan flow by interrupt trigger.

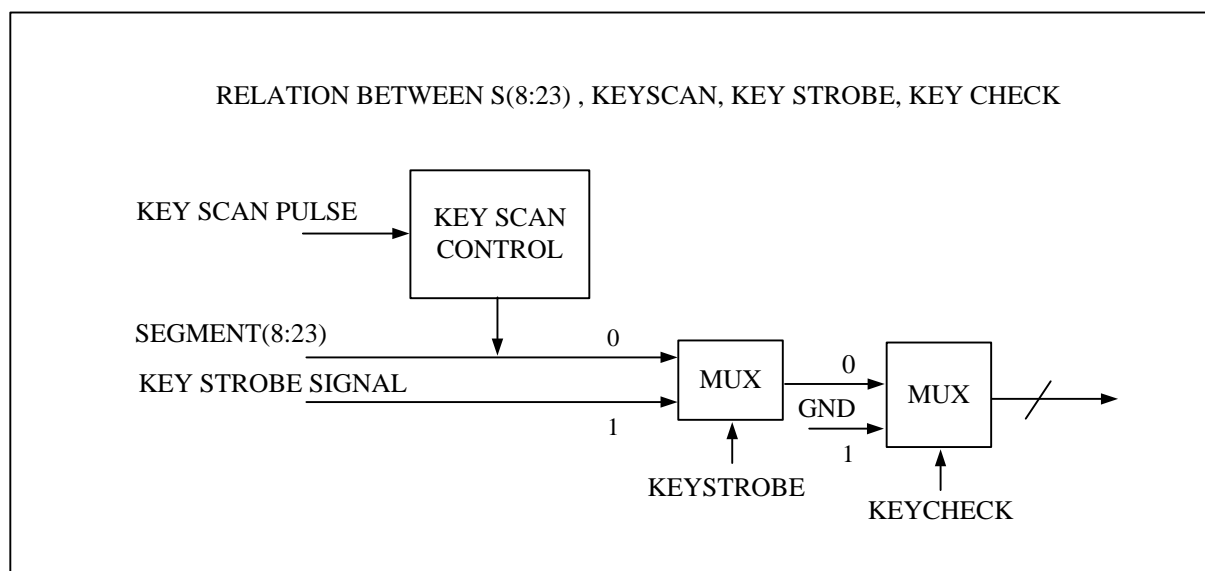


Fig.14 KEYSKAN, KEYSTROBE , KETCHECK and segments.

Bit 7 = 1 : unused

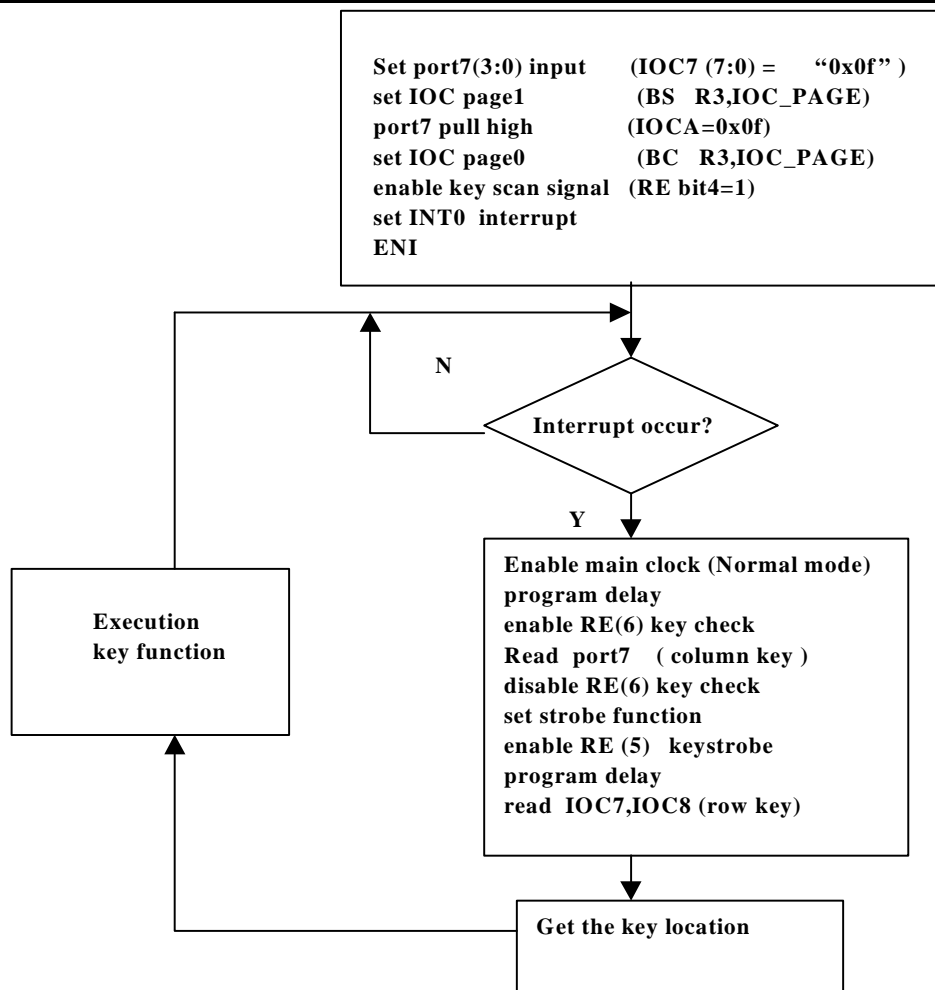


Fig.15 key scan flow by interrupt trigger

PAGE1 (Data RAM address8 ~ address11)

7	6	5	4	3	2	1	0
		0	0	RAM11	RAMA10	RAMA9	RAMA8

Bit 0 ~ Bit 3 (RAMA8 ~ RAMA11) : Data RAM address (address8 to address11) for RAM reading.

Bit 4 , Bit 7 = 0 : unused

RF (Interrupt flags)

7	6	5	4	3	2	1	0
RBF	0	INT2	INT1	INT0	CNT2	CNT1	TCIF

"1" means interrupt request, "0" means non-interrupt

Bit 0 (TCIF) : TCC timer overflow interrupt flag

Set when TCC timer overflows .

Bit 1 (CNT1) : Counter1 timer overflow interrupt flag

Set when counter1 timer overflows .

Bit 2 (CNT2) : Counter2 timer overflow interrupt flag

Set when counter2 timer overflows .

Bit 3 (INT0) : External INT0 pin interrupt flag

If PORT70 ,PORT71,PORT72 or PORT73 has a falling edge trigger signal. CPU will set this bit.

Bit 4 (INT1) : External INT1 pin interrupt flag

If PORT74 ,PORT75 or PORT76 has a falling edge trigger signal. CPU will set this bit.

Bit 5 (INT2) : External INT2 pin interrupt flag

If PORT77 has a falling edge or rising edge (controlled by CONT register) trigger signal. CPU will set this bit.

Bit 6 = 0 : unused

Bit 7 (RBF) : Interrupt flag for SPI data complete

If serial IO 's RBF signal has a rising edge signal (RBF set to "1" when transfer data completely), CPU will set this bit.

IOCF is the interrupt mask register. User can read and clear.

Trigger edge as the table

Signal	Trigger	<Note>
TCC	Time out	
COUNTER1	Time out	
COUNTER2	Time out	
INT0	Falling edge	
INT1	Falling edge	
INT2	Falling/Falling&rising edge	Controlled by CONT register
RBF	Rising edge	

R10~R3F (General Purpose Register)

R10~R3F (Banks 0 ~ 3) : All of them are general purpose registers.

VII.4 Special Purpose Registers

A (Accumulator)

Internal data transfer, or instruction operand holding

It's not an addressable register.

CONT (Control Register)

7	6	5	4	3	2	1	0
INT_EDGE	INT	TS	-	PAB	PSR2	PSR1	PSR0

Bit 0 ~ Bit 2 (PSR0 ~ PSR2) : TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC rate	WDT rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3(PAB) : Prescaler assignment bit

0/1 → TCC/WDT

Bit 4 : undefined

Bit 5(TS) : TCC signal source

0 → Instruction clock

1 → 16.384kHz

Instruction clock = MCU clock/2, Refer to RA Bit 4 ~ Bit 6 for PLL and Main clock selection. See Fig.16.

Bit 6 (INT) : INT enable flag

0 → interrupt masked by DISI or hardware interrupt

1 → interrupt enabled by ENI/RETI instructions

Bit 7 (INT_EDGE) : interrupt edge type of P70

0 ⇒ P70 's interruption source is a rising edge signal and falling edge signal.

1 → P70 's interruption source is a falling edge signal.

CONT register is readable (CONTR) and writable (CONTW).

TCC and WDT :

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only at the same time.

An 8 bit counter is available for TCC or WDT determined by the status of the bit 3 (PAB) of the CONT register.

See the prescaler ratio in CONT register.

Fig.16 depicts the circuit diagram of TCC/WDT.

Both TCC and prescaler will be cleared by instructions which write to TCC each time.

The prescaler will be cleared by the WDT and SLEP instructions, when assigned to WDT mode.

The prescaler will not be cleared by SLEP instructions, when assigned to TCC mode.

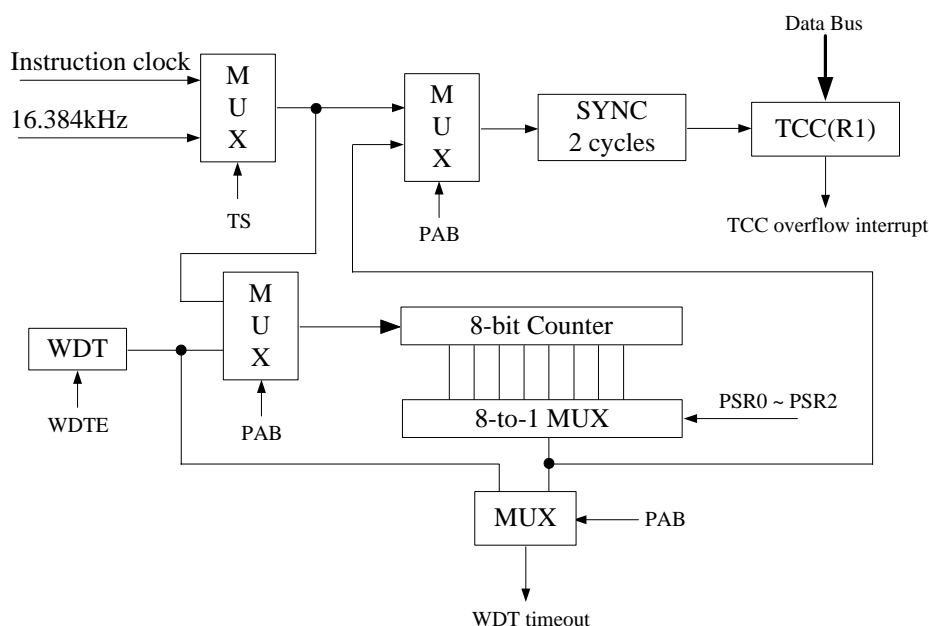


Fig.16 Block diagram of TCC WDT

IOC5 (PORT5 I/O control, PORT switch, Key tone, LCD bias)

PAGE0 (PORT5 I/O control register, PORT switch)

7	6	5	4	3	2	1	0
IOC57	IOC56	IOC55	0	P9SH	P9SL	P8SH	P8SL

Bit 0 (P8SL) : Switch low nibble I/O PORT8 or LCD segment output for share pins SEGxx/P8x pins

0 → select normal P80 ~ P83 for low nibble PORT8

- 1 → select SEG64 ~ SEG67 output for LCD SEGMENT output.
- Bit 1 (P8SH) : Switch high nibble I/O PORT8 or LCD segment output for share pins SEGxx/P8x pins
- 0 → select normal P84 ~ P87 for high nibble PORT8
- 1 → select SEG68 ~ SEG71 output for LCD SEGMENT output.
- Bit 2 (P9SL) : Switch low nibble I/O PORT9 or LCD segment output for share pins SEGxx/P9x pins
- 0 → select normal P90 ~ P93 for low nibble PORT9
- 1 → select SEG72 ~ SEG75 output for LCD SEGMENT output.
- Bit 3 (P9SH) : Switch high nibble I/O PORT9 or LCD segment output for share pins SEGxx/P9x pins
- 0 → select normal P94 ~ P97 for high nibble PORT9
- 1 → select SEG76 ~ SEG79 output for LCD SEGMENT output.*Bit 4:general register
- Bit 4 = 0 : unused
- Bit 5 ~ Bit 7 (IOC55 ~ IOC57) : PORT5 I/O direction control registers.
- 0 → put the relative I/O pin as output
- 1 → put the relative I/O pin into high impedance

PAGE1 (Key tone control, LCD bias control)

7	6	5	4	3	2	1	0
KT1	KT0	KTS	0	BIAS3	BIAS2	BIAS1	BIAS0

Bit 0 ~ Bit 3 (BIAS0 ~ BIAS3) : LCD operation voltage selection

$$V1 = VDD * (5 - n/15)/5$$

(BIAS3 to BIAS0)	V1 voltage	Example (VDD=5V)
0000	$VDD * (5-0/15)/5$	5V
0001	$VDD * (5-1/15)/5$	4.93V
0010	$VDD * (5-2/15)/5$	4.86V
0011	$VDD * (5-3/15)/5$	4.80V
0100	$VDD * (5-4/15)/5$	4.73V
:	:	:
1101	$VDD * (5-13/15)/5$	4.13V
1110	$VDD * (5-14/15)/5$	4.07V
1111	$VDD * (5-15/15)/5$	4.0V

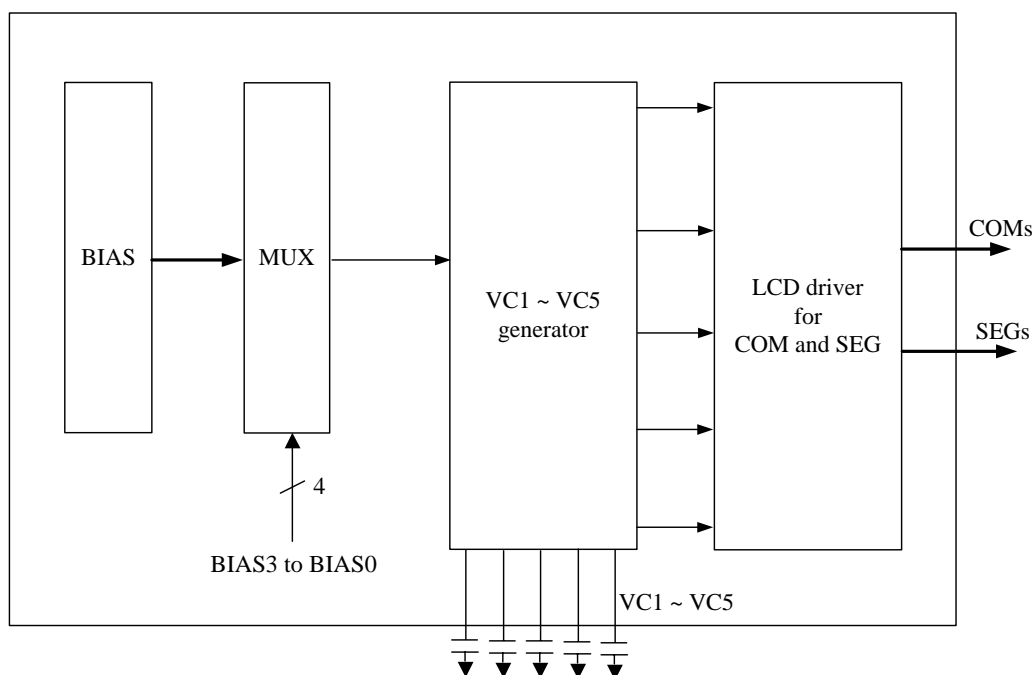


Fig.17. The relation between bias and V1 to V5

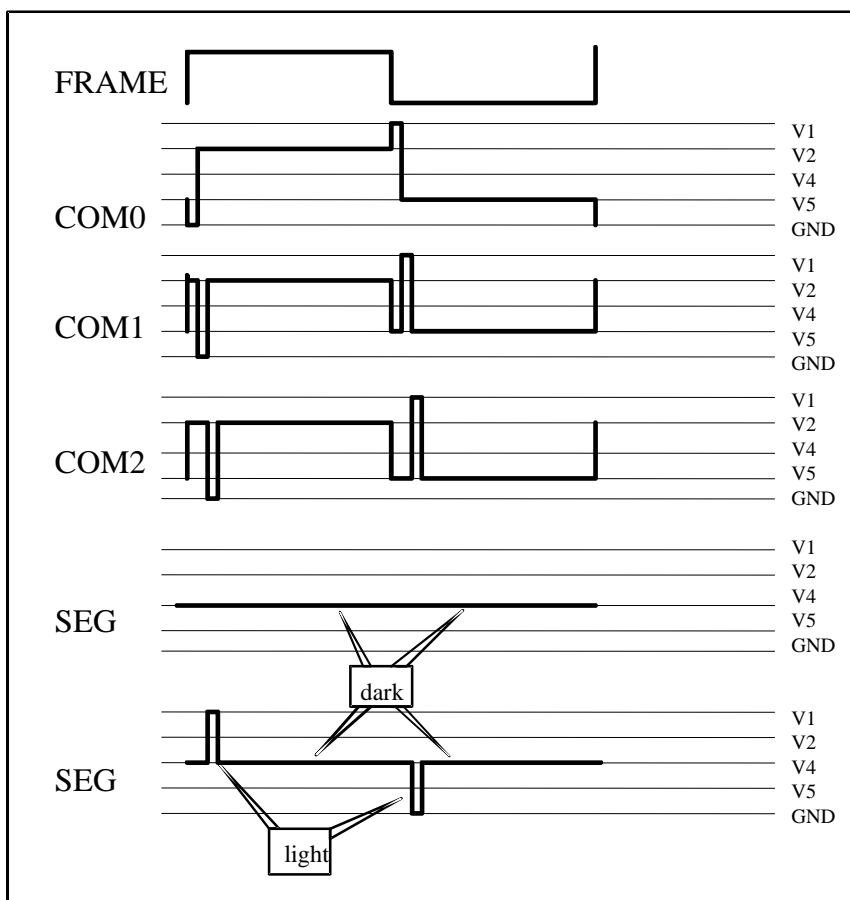


Fig.18a LCD waveform (1/4 bias) for 1/8 duty, 1/9 duty, 1/16 duty

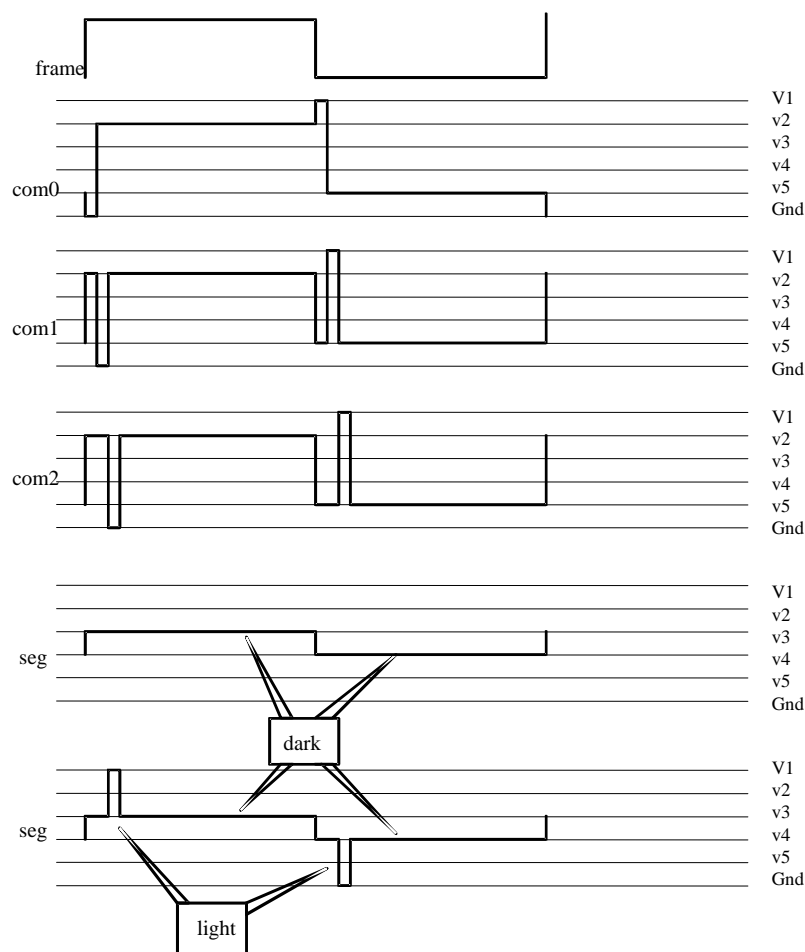


Fig.18b LCD waveform (1/5 bias) for 1/24 duty

Bit 4 = 0 : unused

Bit 5 (KTS) : Key tone output switch

0 → normal PORT67

1 → key tone output .

Bit 6 ~ Bit 7 (KT0 ~ KT1) : Key tone output frequency and its power control

KT1	KT0	Key tone frequency and power
0	0	32.768KHz/32 = 1.024kHz clock and enable
0	1	32.768KHz/16 = 2.048kHz clock and enable
1	0	32.768KHz/8 = 4.096kHz clock and enable
1	1	Power off key tone

IOC6 (PORT6 I/O control, PORT switch, LCD driving control)

PAGE0 (PORT6 I/O control register)

7	6	5	4	3	2	1	0
IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60

Bit 0 ~ Bit 7 (IOC60 ~ IOC67) : PORT6(0~7) I/O direction control register

0 → put the relative I/O pin as output

1 → put the relative I/O pin into high impedance

PAGE1

(empty register)

PAGE 2 (PORT switch, LCD driving ability control)

7	6	5	4	3	2	1	0
PCSH	PCSL	PBS	LCDDV1	LCDDV0	0	0	0

Bit 0 ~ Bit 2 = 0 : unused

Bit 3 ~ Bit 4 (LCDDV0 ~ LCDDV1) : LCD driver's driving ability control

LCDDV1	LCDDV0	Driving mode
0	0	Normal mode (ratio = 1)
0	1	Weak mode (ratio = 1/2)
1	0	Strong mode (ratio = 2)
1	1	Maximum mode (ratio = 4)

LCDDV0 ~ LCDDV1 are used to select the driving ability of LCD driver. The driving ability is Maximum mode > Strong mode > Normal mode > Weak mode by 1/2 ratio individually. The larger driving ability it is selected, the larger output loading of LCD driver output can be afforded and the more current consumption is occurred. It depends on user's application.

Bit 5 (PBS) : Switch I/O PORTB or LCD segment output for share pins SEGxx/PBx

0 → select normal PB0 ~ PB7 for PORTB

1 → select SEG48 ~ SEG55 output for LCD SEGMENT output.

Bit 6 (PCSL) : Switch low nibble I/O PORTC or LCD segment output for share pins SEGxx/PCx

0 → select normal PC0 ~ PC3 for low nibble PORTC

1 → select SEG56 ~ SEG59 output for LCD SEGMENT output.

Bit 7 (PCSH) : Switch high nibble I/O PORTC or LCD segment output for share pins SEGxx/PCx

0 → select normal PC4 ~ PC7 for high nibble PORTC

1 → select SEG60 ~ SEG63 output for LCD SEGMENT output.

IOC7 (PORT7 I/O control, Key strobe(8~15))
PAGE0 (PORT7 I/O control register)

7	6	5	4	3	2	1	0
IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70

Bit 0 ~ Bit 7 (IOC70 ~ IOC77) : PORT7(0~7) I/O direction control register

0 → put the relative I/O pin as output

1 → put the relative I/O pin into high impedance

PAGE1 (Key strobe control register)

7	6	5	4	3	2	1	0
STRB15	STRB14	STRB13	STRB12	STRB11	STRB10	STRB9	STRB8

Bit 0 ~ Bit 7 (STRB8 ~ STRB15) : Key strobe control bits

These key strobe control registers correspond to SEGMENT8 to SEGMENT15. Please refer KEYSTOBE explanation (RE page0).

IOC8 (PORT8 I/O control, , Key strobe(16~23))
PAGE0 (PORT8 I/O control register)

7	6	5	4	3	2	1	0
IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80

Bit 0 ~ Bit 7 (IOC80 ~ IOC87) : PORT8(0~7) I/O direction control register

0 → put the relative I/O pin as output

1 → put the relative I/O pin into high impedance

PAGE1 (Key strobe control register)

7	6	5	4	3	2	1	0
STRB23	STRB22	STRB21	STRB20	STRB19	STRB18	STRB17	STRB16

Bit 0 ~ Bit 7 (STRB16 ~ STRB23) : Key strobe control bits

These key strobe control registers correspond to SEGMENT16 to SEGMENT23. Please refer KEYSTOBE explanation (RE page0).

IOC9 (PORT9 I/O control)

PAGE0 (PORT9 I/O control register)

7	6	5	4	3	2	1	0
IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90

Bit 0 ~ Bit 7 (IOC90 ~ IOC97) : PORT9(0~7) I/O direction control register

0 → put the relative I/O pin as output

1 → put the relative I/O pin into high impedance

IOCA (CN1's and CN2's clock and scaling, PORT7 pull high control)

PAGE0 (Counter1's and Counter2's clock and scale setting)

7	6	5	4	3	2	1	0
CNT2S	C2P2	C2P1	C2P0	CNT1S	C1P2	C1P1	C1P0

Bit 0 ~ Bit 2 (C1P0 ~ C1P2) : Counter1 scaling

C1P2	C1P1	C1P0	COUNTER1
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (CNT1S) : Counter1 clock source

0/1 → 16.384kHz/MCU clock

Bit 4 ~ Bit 6 (C2P0 ~ C2P2) : Counter2 scaling

C2P2	C2P1	C2P0	COUNTER2
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 7 (CNT2S) : Counter2 clock source

0/1 → 16.384kHz/MCU clock

PAGE1 (PORT7 pull high control register)

7	6	5	4	3	2	1	0
PH77	PH76	PH75	PH74	PH73	PH72	PH71	PH70

Bit 0 ~ Bit 7 (PH70 ~ PH77) : PORT7(0~7) pull high control register

0 → disable pull high function.

1 → enable pull high function

IOCB (PORTB I/O control, PORT6 pull high control)

PAGE0 (PORTB I/O control register)

7	6	5	4	3	2	1	0
IOCB7	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0

Bit 0 ~ Bit 7 (IOCB0 ~ IOCB7) : PORTB(0~7) I/O direction control register

0 → put the relative I/O pin as output

1 → put the relative I/O pin into high impedance

PAGE1 (PORT6 pull high control register)

7	6	5	4	3	2	1	0
PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60

Bit 0 ~ Bit 7 (PH60 ~ PH67) : PORT6(0~7) pull high control register

0 → disable pull high function.

1 → enable pull high function

IOCC (PORTC I/O control, TONE1 control)

PAGE0 (PORT9 I/O control register)

7	6	5	4	3	2	1	0
IOCC7	IOCC6	IOCC5	IOCC4	IOCC3	IOCC2	IOCC1	IOCC0

Bit 0 ~ Bit 7 (IOCC0 ~ IOCC7) : PORTC(0~7) I/O direction control register

0 → put the relative I/O pin as output

1 → put the relative I/O pin into high impedance

PAGE1 (TONE1 control register)

7	6	5	4	3	2	1	0
T17	T16	T15	T14	T13	T12	T11	T10

Bit 0 ~ Bit 7(T10 ~ T17) : Tone generator1's frequency divider and power control

Please Run in Normal mode .

Clock source = 111957Hz

T17~T10 = '11111111' => Tone generator1 will has 439Hz SIN wave output.

:

T17~T10 = '00000010' => Tone generator1 will has 55978Hz SIN wave output.

T17~T10 = '00000001' => DC bias voltage output

T17~T10 = '00000000' => Power off

Built-in tone generator can generate dialing tone signals for telephone of dialing tone type or just a single tone. In DTMF application, there are two kinds of tone. One is the group of row frequency (TONE1), the other is the group of column frequency (TONE2), each group has 4 kinds of frequency, user can get 16 kinds of DTMF frequency totally. Tone generator contains a row frequency sine wave generator for generating the DTMF signal which selected by IOCC and a column frequency sine wave generator for generating the DTMF signal which selected by IOCD. This block can generate single tone by filling one of these two register.

If all the values are low, the power of tone generators will turn off .

		TONE2 (IOCD PAGE1) High group freq.			
		1203.8 (0X5D)	1332.8(0X54)	1473.1(0X4C)	1646.4(0X44)
TONE1(IOCC PAGE1) Low group freq.	699.7Hz(0x0A0)	1	2	3	A
	772.1Hz(0x091)	4	5	6	B
	854.6Hz(0x083)	7	8	9	C
	940.8Hz(0x077)	*	0	#	D

Also TONE1 and TONE2 are an asynchronous tone generator so the both can be used to generate Caller ID FSK signal. In FSK generator application, TONE1 or TONE2 can generate 1200Hz Mark bit and 2200Hz Space bit for Bell202 or 1300Hz Mark bit and 2100Hz Space bit for V.23. See the following table.

TONE1(IOCC PAGE1) or TONE2(IOCD PAGE1)	Freq. (Hz)	
0x5D	1203.8	Bell202 FSK Mark bit
0x33	2195.2	Bell202 FSK Space bit
0x56	1301.8	V.23 FSK Mark bit
0x35	2112.4	V.23 FSK Space bit

IOCD (Counter1 data, TONE2 control)

PAGE0 (Counter1 data buffer)

7	6	5	4	3	2	1	0
CN17	CN16	CN15	CN14	CN13	CN12	CN11	CN10

Bit 0 ~ Bit 7 (CN10 ~ CN17) : Counter1's data buffer

User can read and write this buffer. Counter1 is a eight bit up-counter with 8-bit prescaler that user can use IOCD to preset and read the counter. (write = preset) After a interruption, it will reload the preset value.

Example: write: IOW 0x0D ; write the data at accumulator to counter1 (preset)

Example: read: IOR 0x0D ;read IOCD data and write to accumulator

PAGE1 (TONE2 control register)

7	6	5	4	3	2	1	0
T27	T26	T25	T24	T23	T22	T21	T20

Bit 0 ~ Bit 7(T20 ~ T27) : Tone generator 2's frequency divider and power control

Please Run in Normal mode .

Clock source = 111957Hz

T27~T20 = '11111111' => Tone generator2 will has 439Hz SIN wave output.

:

T27~T20 = '00000010' => Tone generator2 will has 55978Hz SIN wave output.

T27~T20 = '00000001' => DC bias voltage output

T27~T20 = '00000000' => Power off

IOCE (Counter2 data, Comparator and OP control)

PAGE0 (Counter2 data buffer, Comparator control, OP control)

7	6	5	4	3	2	1	0
CN27	CN26	CN25	CN24	CN23	CN22	CN21	CN20

Bit 0 ~ Bit 7 (CN20 ~ CN27) : Counter2's data buffer

User can read and write this buffer. Counter2 is a eight bit up-counter with 8-bit prescaler that user can use IOCD to preset and read the counter. (write = preset) After a interruption, it will reload the preset value.

Example: write: IOW 0x0D ; write the data at accumulator to counter1 (preset)

Example: read: IOR 0x0D ;read IOCD data and write to accumulator

PAGE1 (Comparator reference voltage type, PORT switch)

7	6	5	4	3	2	1	0
CMPREF	CMPIN3	CMPIN2	CMPIN1	0	0	0	0

Bit 0 ~ Bit 3 = 0 : unused

Bit 4 (CMPIN1) : Switch for controlling PORT63 as IO PORT or a comparator input.

0 → IO PORT63

1 → comparator input

Bit5 (CMPIN2) : Switch for controlling PORT64 as IO PORT or a comparator input.

0 → IO PORT64

1 → comparator input

Bit 6 (CMPIN3) : Switch for controlling PORT65 as IO PORT or a comparator input.

0 → IO PORT65

1 → comparator input

Bit 7 (CMPREF) : Switch for comparator reference voltage type

0 → internal reference voltage

1 → external reference voltage

PAGE2 (Reference voltage VR selection)

7	6	5	4	3	2	1	0
VRSEL							

Bit 0~6 : Unused

Bit 7 (VRSEL) : Reference voltage VR selection bit for Comparator

0/1 → VR = VDD/VR = 2.0V, When this bit is set to "0", V2_0 ref. circuit will be powered off.

2.0V ref. circuit is only powered on when this bit and RD page0 bit 7(CMPEN) are all set to "1".

IOCF (Interrupt Mask Register)

7	6	5	4	3	2	1	0
RBF	0	INT2	INT1	INT0	CNT2	CNT1	TCIF

Bit 0 ~ Bit 5,7 are interrupt mask enable bits.

0 → disable interrupt

1 → enable interrupt

Bit 6 = 0 : unused

VII.5 I/O Port

The I/O registers are bi-directional tri-state I/O ports. The I/O ports can be defined as "input" or "output" pins by the I/O control registers under program control. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig.19.

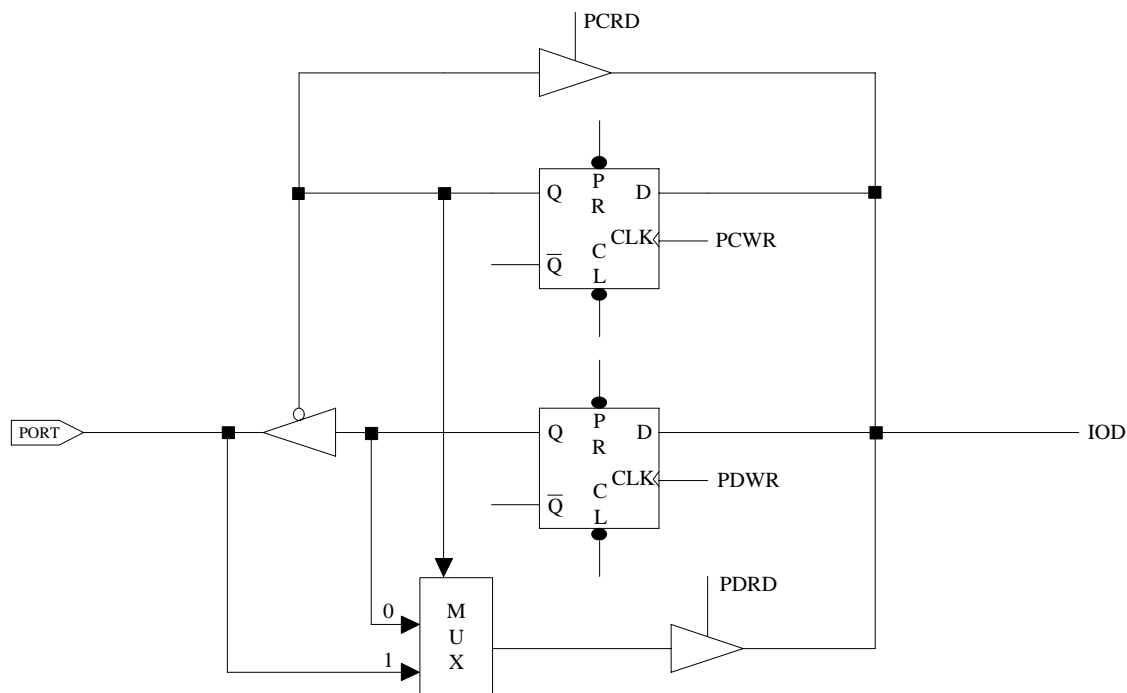


Fig.19 The circuit of I/O port and I/O control register

VII.6 RESET

The RESET can be caused by

- (1) Power on voltage detector reset (POVD) and power on reset
- (2) WDT timeout. (if enabled and in GREEN or NORMAL mode)
- (3) /RESET pin pull low

<Note> At case (1), POVD is controlled by CODE OPTION. If you enable POVD, CPU will reset at 2V under. And CPU will consume more current about 3uA . And the power on reset is a circuit always enable. It will reset CPU at about 1.4V and consume about 0.5uA.

Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- When power on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
- The Watchdog timer and prescaler counter are cleared.
- The Watchdog timer is disabled.
- The CONT register is set to all "1"
- The other register (bit7..bit0)

A Address	R register Page0	R register Page1	IOC Register Page0	IOC Register page1	IOC Register Page2
3	000xxxxx				
4	00xxxxxx	00000000			
5	xxx00000	xxxxxxx	11100000	00000000	
6	xxxxxxx	xxxxxxx	11111111	-	00000000
7	xxxxxxx	Xxxxxxxx	11111111	11111111	
8	xxxxxxx	Xxxxxxxx	11111111	11111111	
9	xxxxxxx	x0000000	11111111	-	
A	00000110	Xxxxxxxx	00000000	00000000	
B	xxxxxxx	Xxxxxxxx	11111111	00000000	
C	xxxxxxx	Xxxxxxxx	11111111	00000000	
D	00000000	Xxxxxxxx	00000000	00000000	
E	10000000	000xxxxx	00000000	00000000	00000000
F	00000000	-	00000000	-	

VII.7 wake-up

The controller has two types of sleep mode for power saving.

- (1) SLEEP mode , RA(7)=0 + "SLEP" instruction .

The controller will turn off all the CPU and crystal. Other circuit with power control like key tone control or PLL control (which has enable register), user has to turn it off by software.

- (2) IDLE mode , RA(7)=1 + "SLEP" instruction.

The controller will turn CPU off, but the crystal.

Wake-up from SLEEP mode

- (1) DT time out
- (2) external interrupt
- (3) /RESET pull low

All these cases will reset controller , and run the program at address zero. The status just like the power on reset. Be sure to enable circuit at case (1) or (2).

Wake-up from IDLE mode

- (1) WDT time out
- (2) external interrupt
- (3) internal interrupt like counters

All these cases , user has to enable circuit before entering IDLE mode. After wake-up, all the register will keep values just like into "SLEP" instruction before.

At case (2) or (3) , controller will wake up and jump to address eight for interruption sub-routine. After finish sub-routine ("RETI" instruction), program will jump to the next instruction from "SLEP" instruction.

VII.8 Interrupt

RF is the interrupt status register which records the interrupt request in flag bits. IOCF is the interrupt mask register. TCC timer, Counter1 and Counter2 are internal interrupt source. P70 ~ P77(INT0 ~ INT1) are external interrupt input which interrupt sources are come from the external. If the interrupts are happened by these interrupt sources, then RF register will generate '1' flag to corresponding register if you enable IOCF register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) generated, will cause the next instruction to be fetched from address 008H. Once in the interrupt service routine the source of the interrupt can be determined by polling the flag bits in the RF register. The interrupt flag bit must be cleared in software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

VII.10 Instruction Set

Instruction set has the following features:

- (1) Every bit of any register can be set, cleared, or tested directly.
- (2) The I/O register can be regarded as general register. That is, the same instruction can operates on I/O register. The symbol "R" represents a register designator which specifies which one of the 64 registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator which selects the number of the bit, located in the register "R", affected by the operation. "k" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED	Instruction cycle
0 0000 0000 0000	0000	NOP	No Operation	None	1
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C	1
0 0000 0000 0010	0002	CONTW	A → CONT	None	1
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P	1
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P	1
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None	1
0 0000 0001 0000	0010	ENI	Enable Interrupt	None	1
0 0000 0001 0001	0011	DISI	Disable Interrupt	None	1
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None	2
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None	2
0 0000 0001 0100	0014	CONTR	CONT → A	None	1
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None	1
0 0000 0010 0000	0020	TBL	R2+A → R2 bits 9,10 do not clear	Z,C,DC	2

0	0000	01rr	rrrr	00rr	MOV R,A	$A \rightarrow R$	None	1
0	0000	1000	0000	0080	CLRA	$0 \rightarrow A$	Z	1
0	0000	11rr	rrrr	00rr	CLR R	$0 \rightarrow R$	Z	1
0	0001	00rr	rrrr	01rr	SUB A,R	$R-A \rightarrow A$	Z,C,DC	1
0	0001	01rr	rrrr	01rr	SUB R,A	$R-A \rightarrow R$	Z,C,DC	1
0	0001	10rr	rrrr	01rr	DECA R	$R-1 \rightarrow A$	Z	1
0	0001	11rr	rrrr	01rr	DEC R	$R-1 \rightarrow R$	Z	1
0	0010	00rr	rrrr	02rr	OR A,R	$A \vee R \rightarrow A$	Z	1
0	0010	01rr	rrrr	02rr	OR R,A	$A \vee R \rightarrow R$	Z	1
0	0010	10rr	rrrr	02rr	AND A,R	$A \& R \rightarrow A$	Z	1
0	0010	11rr	rrrr	02rr	AND R,A	$A \& R \rightarrow R$	Z	1
0	0011	00rr	rrrr	03rr	XOR A,R	$A \oplus R \rightarrow A$	Z	1
0	0011	01rr	rrrr	03rr	XOR R,A	$A \oplus R \rightarrow R$	Z	1
0	0011	10rr	rrrr	03rr	ADD A,R	$A + R \rightarrow A$	Z,C,DC	1
0	0011	11rr	rrrr	03rr	ADD R,A	$A + R \rightarrow R$	Z,C,DC	1
0	0100	00rr	rrrr	04rr	MOV A,R	$R \rightarrow A$	Z	1
0	0100	01rr	rrrr	04rr	MOV R,R	$R \rightarrow R$	Z	1
0	0100	10rr	rrrr	04rr	COMA R	$\neg R \rightarrow A$	Z	1
0	0100	11rr	rrrr	04rr	COM R	$\neg R \rightarrow R$	Z	1
0	0101	00rr	rrrr	05rr	INCA R	$R+1 \rightarrow A$	Z	1
0	0101	01rr	rrrr	05rr	INC R	$R+1 \rightarrow R$	Z	1
0	0101	10rr	rrrr	05rr	DJZA R	$R-1 \rightarrow A$, skip if zero	None	2 if skip
0	0101	11rr	rrrr	05rr	DJZ R	$R-1 \rightarrow R$, skip if zero	None	2 if skip
0	0110	00rr	rrrr	06rr	RRCA R	$R(n) \rightarrow A(n-1)$ $R(0) \rightarrow C, C \rightarrow A(7)$	C	1
0	0110	01rr	rrrr	06rr	RRC R	$R(n) \rightarrow R(n-1)$ $R(0) \rightarrow C, C \rightarrow R(7)$	C	1
0	0110	10rr	rrrr	06rr	RLCA R	$R(n) \rightarrow A(n+1)$ $R(7) \rightarrow C, C \rightarrow A(0)$	C	1
0	0110	11rr	rrrr	06rr	RLC R	$R(n) \rightarrow R(n+1)$ $R(7) \rightarrow C, C \rightarrow R(0)$	C	1
0	0111	00rr	rrrr	07rr	SWAPA R	$R(0-3) \rightarrow A(4-7)$ $R(4-7) \rightarrow A(0-3)$	None	1
0	0111	01rr	rrrr	07rr	SWAP R	$R(0-3) \leftrightarrow R(4-7)$	None	1
0	0111	10rr	rrrr	07rr	JZA R	$R+1 \rightarrow A$, skip if zero	None	2 if skip
0	0111	11rr	rrrr	07rr	JZ R	$R+1 \rightarrow R$, skip if zero	None	2 if skip
0	100b	bbrr	rrrr	0xxx	BC R,b	$0 \rightarrow R(b)$	None	1
0	101b	bbrr	rrrr	0xxx	BS R,b	$1 \rightarrow R(b)$	None	1
0	110b	bbrr	rrrr	0xxx	JBC R,b	if $R(b)=0$, skip	None	2 if skip
0	111b	bbrr	rrrr	0xxx	JBS R,b	if $R(b)=1$, skip	None	2 if skip
1	00kk	kkkk	kkkk	1kkk	CALL k	$PC+1 \rightarrow [SP]$ $(Page, k) \rightarrow PC$	None	2
1	01kk	kkkk	kkkk	1kkk	JMP k	$(Page, k) \rightarrow PC$	None	2
1	1000	kkkk	kkkk	18kk	MOV A,k	$k \rightarrow A$	None	1
1	1001	kkkk	kkkk	19kk	OR A,k	$A \vee k \rightarrow A$	Z	1
1	1010	kkkk	kkkk	1Akk	AND A,k	$A \& k \rightarrow A$	Z	1



1	1011	kkkk	kkkk	1Bkk	XOR A,k	$A \oplus k \rightarrow A$	Z	1
1	1100	kkkk	kkkk	1Ckk	RETL k	$k \rightarrow A, [\text{Top of Stack}] \rightarrow \text{PC}$	None	2
1	1101	kkkk	kkkk	1Dkk	SUB A,k	$k - A \rightarrow A$	Z,C,DC	1
1	1110	0000	0001	1E01	INT	$\text{PC} + 1 \rightarrow [\text{SP}]$ $001\text{H} \rightarrow \text{PC}$	None	1
1	1110	100k	kkkk	1E8k	PAGE k	$K \rightarrow R5(4:0)$	None	1
1	1111	kkkk	kkkk	1Fkk	ADD A,k	$k + A \rightarrow A$	Z,C,DC	1

VII.10 CODE Option Register

The controller has one CODE option register which is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

7	6	5	4	3	2	1	0
							/POVD

Bit 0 (/POVD) : Power on voltage detector, 0/1 => enable/disable

/POVD	2.2V /POVD reset	2.2V power on reset	sleep mode current
1	No	Yes (2.2V)	1uA
0	Yes (2.2V)	No	15uA

Bit 1 ~ Bit 7 : unused, must be "0"s.

VIII. Absolute Operation Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
DC SUPPLY VOLTAGE	V _{dd}	-0.3 To 6	V
INPUT VOLTAGE	V _{in}	-0.5 TO V _{dd} +0.5	V
OPERATING TEMPERATURE RANGE	T _a	0 TO 70	

IX DC Electrical Characteristic

(Operation current consumption for Analog circuit under VDD=5V VSS=0V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{CMP}	Operation current for comparator	VDD=5V, PT power on		0.17		mA

(T_a=0°C ~ 70°C, VDD=5V±5%, VSS=0V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IIL1	Input Leakage Current for input pins	V _{IN} = VDD, VSS			±1	μA
IIL2	Input Leakage Current for bi-directional pins	V _{IN} = VDD, VSS			±1	μA
VIH	Input High Voltage		2.5			V
VIL	Input Low Voltage				0.8	V
VIHT	Input High Threshold Voltage	/RESET, TCC, RDET1	2.0			V
VILT	Input Low Threshold Voltage	/RESET, TCC, RDET1			0.8	V
VIHX	Clock Input High Voltage	OSCI	3.5			V
VILX	Clock Input Low Voltage	OSCI			1.5	V
VOH1	Output High Voltage (port5,8,9,B,C)	IOH = -5mA	2.4			V
	(port6,7)	IOH = -8mA	2.4			V
VOL1	Output Low Voltage (port5,8,9,B,C)	IOL = 5mA			0.4	V
	(port6,7)	IOL = 8mA			0.4	V
IPH	Pull-high current	Pull-high active input pin at VSS		-10	-15	μA
ISB1	Power down current (SLEEP mode)	All input and I/O pin at VDD, output pin floating, WDT disabled		1	4	μA
ISB2	Low clock current (GREEN mode)	CLK=32.768KHz, All analog circuit disable, All input and I/O pin at VDD, output pin floating, WDT		50	80	μA

* This specification is subject to be changed without notice.

		disabled, LCD enable				
ISB3	Power down current (IDLE mode)	All input and I/O pin at VDD, output pin floating, WDT disabled		20	30	μA
ICC	Operating supply current (NORMAL mode)	/RESET=High, PLL enable CLK=3.5826MHz, output pin floating, LCD enable, all analog circuit disable		1.3	1.8	mA

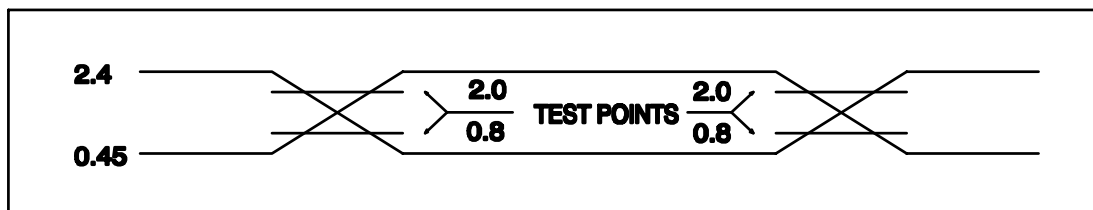
IX AC Electrical Characteristic

(Ta=0°C ~ 70°C, VDD=5V, VSS=0V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle		45	50	55	%
Tins	Instruction cycle time	32.768kHz 3.5826MHz		60 550		us ns
Tdrh	Device delay hold time			16		ms
Ttcc	TCC input period	<Note 1>	(Tins+20)/N			ns
Twtd	Watchdog timer period	Ta = 25°C		16		ms

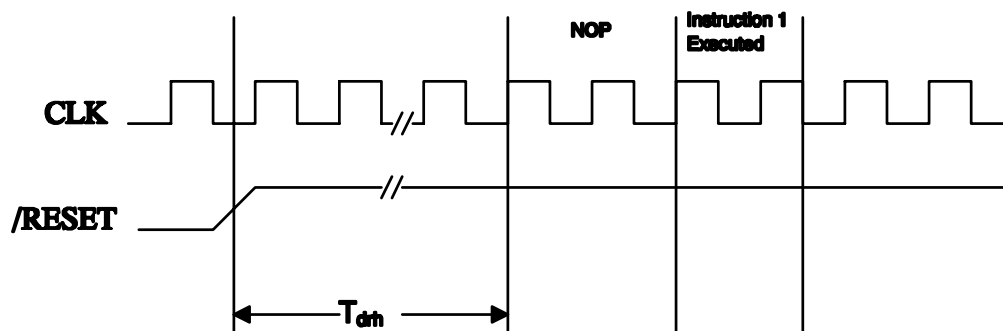
XI. Timing Diagrams

AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing



TCC Input Timing

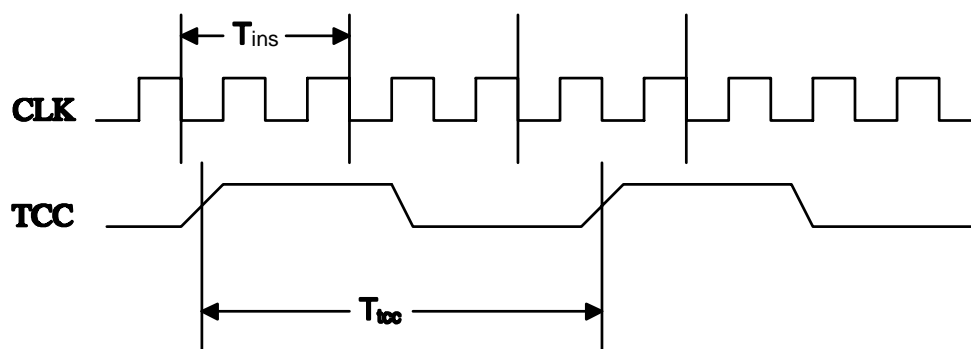


Fig.20 timing

XII. Application Circuit

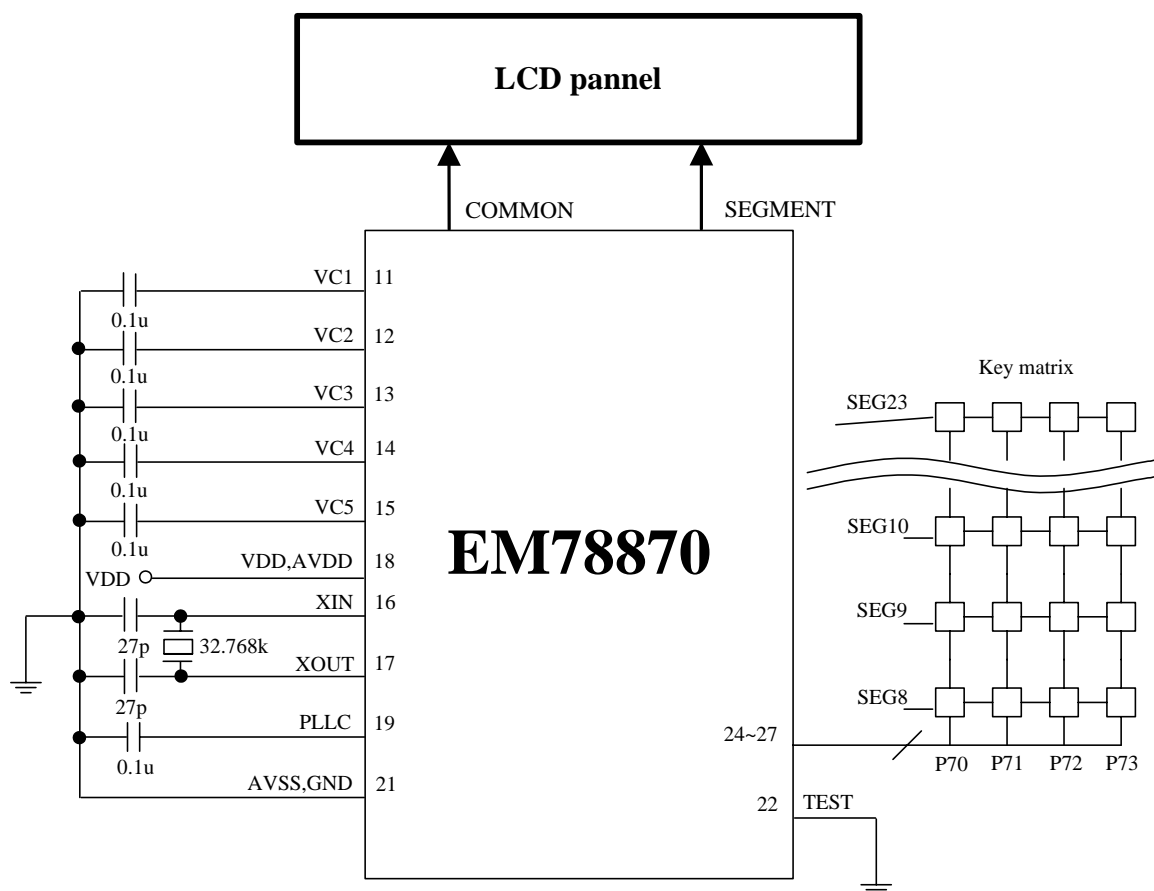


Fig.21 Application circuit