MF768-02

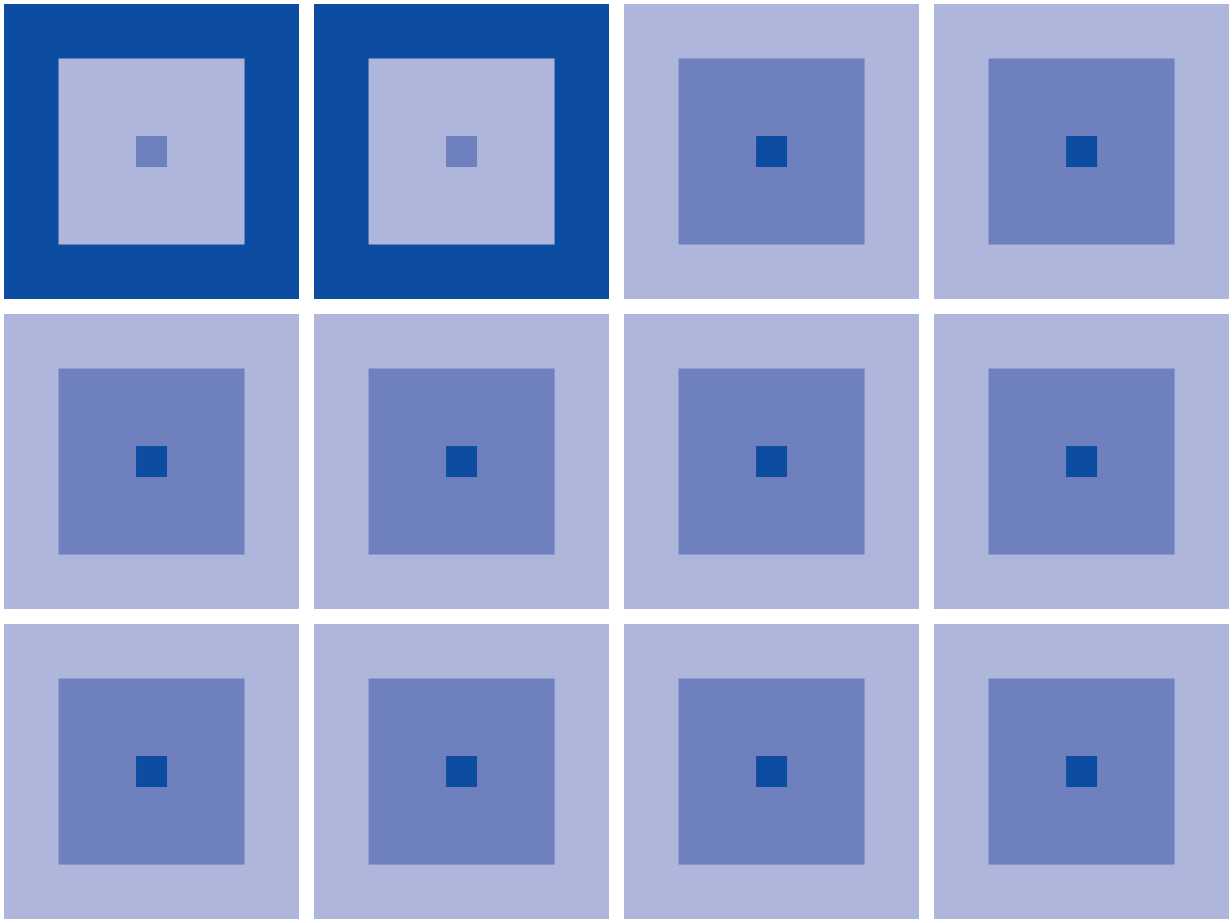
EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

S1C621C0

Technical Manual

S1C621C0 Technical Hardware



SEIKO EPSON CORPORATION

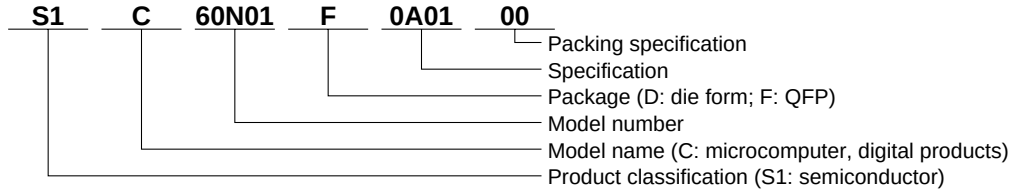
ENERGY SAVING EPSON

The information of the product number change

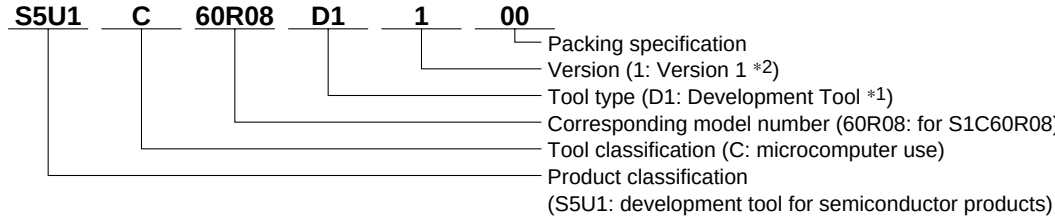
Starting April 1, 2001, the product number will be changed as listed below. To order from April 1, 2001 please use the new product number. For further information, please contact Epson sales representative.

Configuration of product number

Devices



Development tools



*1: For details about tool types, see the tables below. (In some manuals, tool types are represented by one digit.)
*2: Actual versions are not written in the manuals.

Comparison table between new and previous number

S1C60 Family processors

Previous No.	New No.
E0C6001	S1C60N01
E0C6002	S1C60N02
E0C6003	S1C60N03
E0C6004	S1C60N04
E0C6005	S1C60N05
E0C6006	S1C60N06
E0C6007	S1C60N07
E0C6008	S1C60N08
E0C6009	S1C60N09
E0C6011	S1C60N11
E0C6013	S1C60N13
E0C6014	S1C60140
E0C60R08	S1C60R08

S1C62 Family processors

Previous No.	New No.
E0C621A	S1C621A0
E0C6215	S1C62150
E0C621C	S1C621C0
E0C6S27	S1C6S2N7
E0C6S37	S1C6S3N7
E0C623A	S1C6N3A0
E0C623E	S1C6N3E0
E0C6S32	S1C6S3N2
E0C6233	S1C62N33
E0C6235	S1C62N35
E0C623B	S1C6N3B0
E0C6244	S1C62440
E0C624A	S1C624A0
E0C6S46	S1C6S460

Previous No.	New No.
E0C6247	S1C62470
E0C6248	S1C62480
E0C6S48	S1C6S480
E0C624C	S1C624C0
E0C6251	S1C62N51
E0C6256	S1C62560
E0C6292	S1C62920
E0C6262	S1C62N62
E0C6266	S1C62660
E0C6274	S1C62740
E0C6281	S1C62N81
E0C6282	S1C62N82
E0C62M2	S1C62M20
E0C62T3	S1C62T30

Comparison table between new and previous number of development tools

Development tools for the S1C60/62 Family

Previous No.	New No.
ASM62	S5U1C62000A
DEV6001	S5U1C60N01D
DEV6002	S5U1C60N02D
DEV6003	S5U1C60N03D
DEV6004	S5U1C60N04D
DEV6005	S5U1C60N05D
DEV6006	S5U1C60N06D
DEV6007	S5U1C60N07D
DEV6008	S5U1C60N08D
DEV6009	S5U1C60N09D
DEV6011	S5U1C60N11D
DEV60R08	S5U1C60R08D
DEV621A	S5U1C621A0D
DEV621C	S5U1C621C0D
DEV623B	S5U1C623B0D
DEV6244	S5U1C62440D
DEV624A	S5U1C624A0D
DEV624C	S5U1C624C0D
DEV6248	S5U1C62480D
DEV6247	S5U1C62470D

Previous No.	New No.
DEV6262	S5U1C62620D
DEV6266	S5U1C62660D
DEV6274	S5U1C62740D
DEV6292	S5U1C62920D
DEV62M2	S5U1C62M20D
DEV6233	S5U1C62N33D
DEV6235	S5U1C62N35D
DEV6251	S5U1C62N51D
DEV6256	S5U1C62560D
DEV6281	S5U1C62N81D
DEV6282	S5U1C62N82D
DEV6S27	S5U1C6S2N7D
DEV6S32	S5U1C6S3N2D
DEV6S37	S5U1C6S3N7D
EVA6008	S5U1C60N08E
EVA6011	S5U1C60N11E
EVA621AR	S5U1C621A0E2
EVA621C	S5U1C621C0E
EVA6237	S5U1C62N37E
EVA623A	S5U1C623A0E

Previous No.	New No.
EVA623B	S5U1C623B0E
EVA623E	S5U1C623E0E
EVA6247	S5U1C62470E
EVA6248	S5U1C62480E
EVA6251R	S5U1C62N51E1
EVA6256	S5U1C62N56E
EVA6262	S5U1C62620E
EVA6266	S5U1C62660E
EVA6274	S5U1C62740E
EVA6281	S5U1C62N81E
EVA6282	S5U1C62N82E
EVA62M1	S5U1C62M10E
EVA62T3	S5U1C62T30E
EVA6S27	S5U1C6S2N7E
EVA6S32R	S5U1C6S3N2E2
ICE62R	S5U1C62000H
KIT6003	S5U1C60N03K
KIT6004	S5U1C60N04K
KIT6007	S5U1C60N07K

S1C621C0 Technical Manual

PREFACE

This manual explains the function of the S1C621C0, the circuit configurations, and details the controlling method.

CONTENTS

CHAPTER 1 OVERVIEW

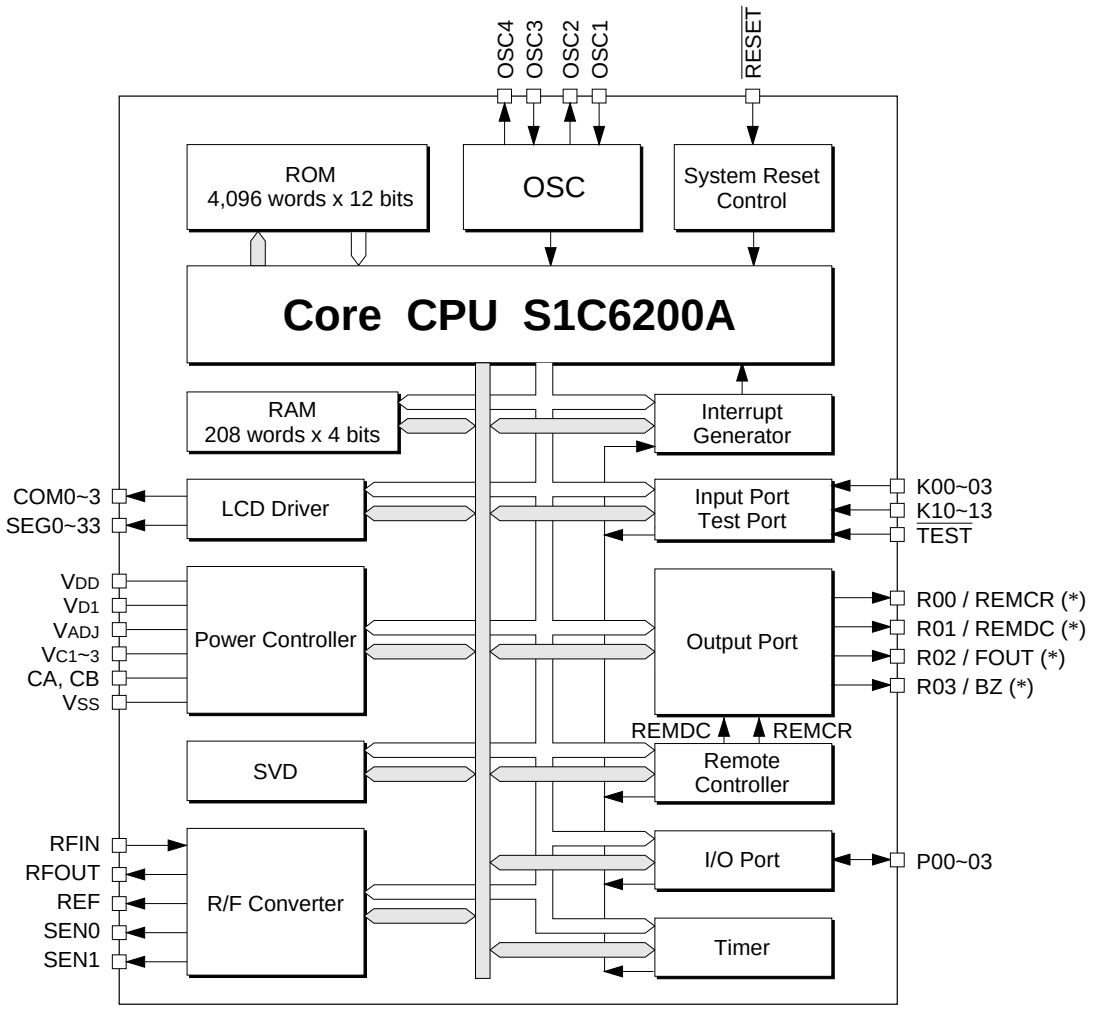
The S1C621C0 is a single-chip microcomputer made up of the 4-bit core CPU S1C6200A, ROM (4,096 words, 12 bits to a word), RAM (208 words, 4 bits to a word), R/F converter, SVD circuit, LCD driver, watchdog timer and time base counter.
The S1C621C0 is most suitable for remote controllers with temperature measurement functions, such as a remote control unit for an air conditioner.

1.1 Features

OSC1 oscillation circuit	Crystal oscillation circuit: 32.768 kHz (Typ.)		
OSC3 oscillation circuit	Ceramic or CR oscillation circuit (*1): 455 kHz (Typ.), 1 MHz (Max.)		
Instruction set	108 types		
Instruction execution time (differ depending on instruction)	During operation at 32 kHz:	153 µsec, 214 µsec, 366 µsec	
	During operation at 455 kHz:	11 µsec, 15 µsec, 26 µsec	
	During operation at 1 MHz:	5 µsec, 7 µsec, 12 µsec	
ROM capacity	4,096 words × 12 bits		
RAM capacity	208 words × 4 bits		
Input port	8 bits (Pull up resistors may be supplemented *1)		
Output port	4 bits (Complementary output or Nch open drain output may be selected *1) May be set to buzzer, clock and REM (carrier, DC) outputs (*2)		
I/O port	4 bits		
LCD driver	34 segments × 1 to 4 commons Static drive or 1/2–1/4 duty dynamic drive may be selected (*2)		
Remote controller	Infrared remote-control carrier output and DC output (level output) Soft-timer mode or hard-timer mode may be selected (*2)		
R/F converter	1 reference resistance × 2 sensors, 16-bit counter DC bias sensor may be connected		
Time base counter	Clock timer: 1 system		
Watchdog timer	Built-in		
SVD circuit (supply voltage detection)	2.3 ± 0.15 V		
External interrupt	Input port interrupt:	2 systems	
Internal interrupt	Timer interrupt:	1 system	
	Remote controller interrupt:	1 system	
	R/F converter interrupt:	1 system	
Supply voltage	2.2–5.5 V		
Current consumption	During HALT:	3 µA	(3 V)
	During operation:	7 µA	(3 V, 32 kHz)
		170 µA	(3 V, 455 kHz)
		250 µA	(3 V, 1 MHz)
Package	QFP5-80pin or chip		

*1 May be selected with mask option.
*2 May be selected with software.

1.2 Block Diagram

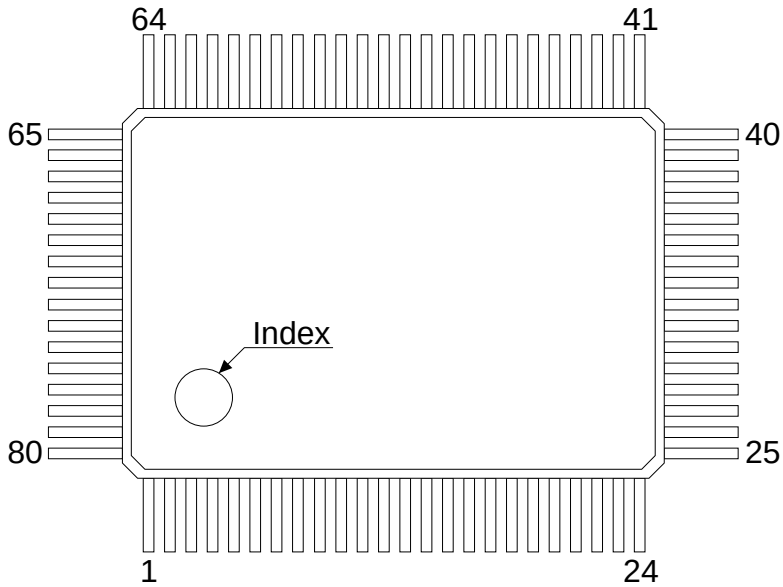


* Output is selected by software

Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

QFP5-80pin (plastic)



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	REF	21	R02	41	CA	61	SEG14
2	N.C.	22	R01	42	CB	62	SEG15
3	N.C.	23	R00	43	COM0	63	SEG16
4	SEN0	24	$\overline{\text{TEST}}$	44	COM1	64	SEG17
5	SEN1	25	K13	45	COM2	65	SEG18
6	N.C.	26	K12	46	COM3	66	SEG19
7	N.C.	27	K11	47	SEG0	67	SEG20
8	N.C.	28	K10	48	SEG1	68	SEG21
9	RFIN	29	K03	49	SEG2	69	SEG22
10	RFOUT	30	K02	50	SEG3	70	SEG23
11	V_{SS}	31	K01	51	SEG4	71	SEG24
12	N.C.	32	K00	52	SEG5	72	SEG25
13	OSC1	33	P03	53	SEG6	73	SEG26
14	OSC2	34	P02	54	SEG7	74	SEG27
15	V_{D1}	35	P01	55	SEG8	75	SEG28
16	OSC3	36	P00	56	SEG9	76	SEG29
17	OSC4	37	V_{ADJ}	57	SEG10	77	SEG30
18	V_{DD}	38	V_{C1}	58	SEG11	78	SEG31
19	$\overline{\text{RESET}}$	39	V_{C2}	59	SEG12	79	SEG32
20	R03	40	V_{C3}	60	SEG13	80	SEG33

N.C. = No Connection

Fig. 1.3.1 Pin layout diagram (QFP5-80pin)

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.	In/Out	Function
V_{DD}	18	(I)	Power supply pin (+)
V_{SS}	11	(I)	Power supply pin (–)
V_{D1}	15	O	Oscillation and internal logic system regulated voltage output pin
V_{C1}	38	O	LCD system regulated voltage output pin
V_{C2}	39	O	LCD system booster voltage output pin ($V_{C1} \times 2$)
V_{C3}	40	O	LCD system booster voltage output pin ($V_{C1} \times 3$)
V_{ADJ}	37	I	V_{C1} voltage adjustment pin
CA, CB	41, 42	–	Voltage booster capacitor connecting pin
OSC1	13	I	Crystal oscillation input pin
OSC2	14	O	Crystal oscillation output pin
OSC3	16	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	17	O	Ceramic or CR oscillation output pin (selected by mask option)
COM0~COM3	43~46	O	LCD common output pin (static or 1/2–1/4 duty dynamic drive, programmable)
SEG0~SEG33	47~80	O	LCD segment output pin (DC output may be selected by mask option)
K00~K03	32~29	I	Input port pin
K10~K13	28~25	I	Input port pin
P00~P03	36~33	I/O	I/O port pin
R00	23	O	Output port pin (DC or REMCR output may be selected by software)
R01	22	O	Output port pin (DC or REMDC output may be selected by software)
R02	21	O	Output port pin (DC or FOUT output may be selected by software)
R03	20	O	Output port pin (DC or BZ output may be selected by software)
REF	1	O	Reference resistance connecting pin for R/F converter
SEN0, SEN1	4, 5	O	Sensor connecting pin for R/F converter
RFIN	9	I	R/F converter CR oscillation input pin
RFOUT	10	O	R/F converter oscillation frequency output pin
$\overline{\text{RESET}}$	19	I	Initial reset input pin
$\overline{\text{TEST}}$	24	I	Testing input pin

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

The S1C621C0 operating power voltage is as follows:

2.2 V to 5.5 V

The S1C621C0 operates when a single power supply within the above range is applied between VDD and VSS. The IC itself can generate the voltage necessary for the internal circuits with the following built-in power supply circuit.

Table 2.1.1 Power supply circuit and output voltage

Circuit	Power supply circuit	Output voltage
Oscillation and internal circuits	Oscillation system regulated voltage circuit	VD1
LCD driver	LCD system regulated voltage circuit and LCD system voltage booster circuit	VC1–VC3

Note: • External loads cannot be driven by the regulated voltage and voltage booster circuits' output voltages.

• See Chapter 7, "ELECTRICAL CHARACTERISTICS" for voltage values.

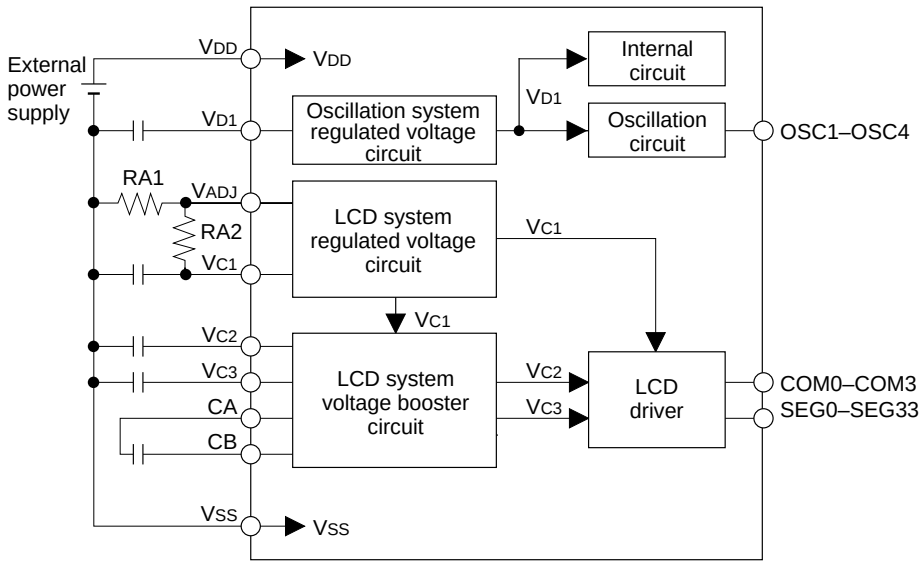


Fig. 2.1.1 Configuration of power supply

2.1.1 Voltage <V_{D1}> for oscillation circuit and internal circuits

V_{D1} is the voltage for the oscillation circuit and the internal logic circuits, and is generated by the oscillation system regulated voltage circuit for stabilizing the oscillation.
Making V_{SS} the standard (GND level), the oscillation system regulated voltage circuit generates V_{D1} from the supply voltage that is input from the V_{DD}–V_{SS} terminals.

2.1.2 Voltage <V_{C1}, V_{C2} and V_{C3}> for LCD driving

V_{C1}, V_{C2} and V_{C3} are the voltages for LCD drive, and are generated by the LCD system regulated voltage circuit and the LCD system voltage booster circuit to stabilize the display quality.
V_{C1} is generated by the LCD system regulated voltage circuit with V_{SS} as the standard from the supply voltage input from the V_{DD}–V_{SS} terminals.
V_{C2} and V_{C3} are respectively double and triple obtained from the LCD system voltage booster circuit.
The V_{C1} voltage can be adjusted to match the LCD panel characteristics by applying feedback to the V_{ADJ} terminal using resistances RA1 and RA2 as shown in Figure 2.1.2.1.
The voltage V_{C1} (V_{SS} standard) is shown by the following expression:

$V_{C1} \approx 1 + RA2/RA1$

Example:

V_{C1}	RA1	RA2
Approx. 1 V	∞	0 Ω
Approx. 1.5 V	2 MΩ	1 MΩ

See Chapter 7, "ELECTRICAL CHARACTERISTICS" for the voltage value.

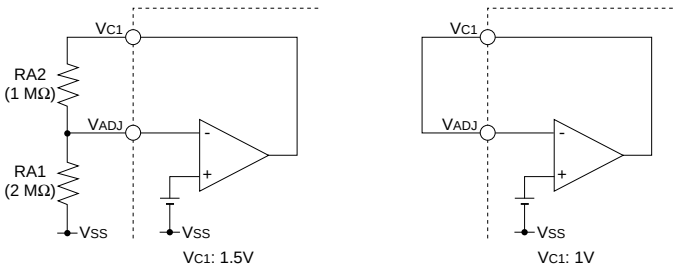


Fig. 2.1.2.1 V_{C1} adjustment circuit

2.2 Initial Reset

To initialize the S1C621C0 circuits, initial reset must be executed. There are two ways of doing this.

(1) External initial reset by the $\overline{\text{RESET}}$ terminal
(2) Initial reset by the watchdog timer

Be sure to use reset function (1) when turning the power on and be sure to initialize securely. In normal operation, the circuit may be initialized by any of the above two types.

Figure 2.2.1 shows the configuration of the initial reset circuit.

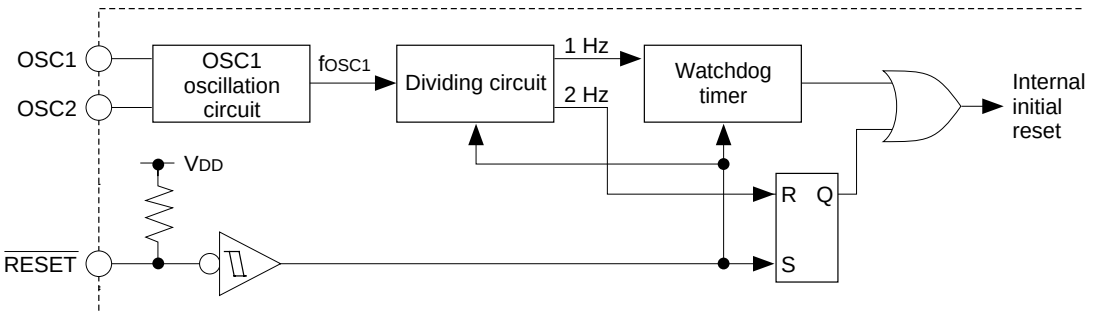


Fig. 2.2.1 Configuration of the initial reset circuit

2.2.1 Reset terminal (RESET)

Initial reset can be executed externally by setting the reset terminal to a low level (VSS). After that the initial reset is released by setting the reset terminal to a high level (VDD) and the CPU starts operation.
The reset input signal is maintained by the RS latch and becomes the internal initial reset signal. The RS latch is designed to be released by a 2 Hz signal (high) that is divided by the OSC1 clock. Therefore in normal operation, a maximum of 250 msec (when fOSC1 = 32 kHz) is needed until the internal initial reset is released after the reset terminal goes to high level. Be sure to maintain a reset input of 0.1 msec or more.
However, when turning the power on, the reset terminal should be set at a low level as in the timing shown in Figure 2.2.1.1.

The reset terminal should be set to 0.1·VDD or less (low level) until the supply voltage becomes 2.2 V or more.
After that, a level of 0.4·VDD or less should be maintained more than 2.0 msec.

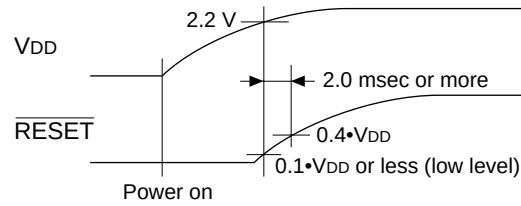


Fig. 2.2.1.1 Initial reset at power on

2.2.2 Watchdog timer

If the CPU runs away for some reason, the watchdog timer will detect this situation and output an initial reset signal. See Section 4.2, "Resetting Watchdog Timer", for details.
As with the oscillation detection circuit, you should not do an initial reset at power-on using this function.

2.2.3 Internal register at initial resetting

Initial reset initializes the CPU as shown in the table below.

Table 2.2.3.1 Initial values

CPU core			
Name	Symbol	Number of bits	Setting value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
New page pointer	NPP	4	1H
Stack pointer	SP	8	Undefined
Index register IX	IX	11	Undefined
Index register IY	IY	11	Undefined
Register pointer	RP	4	Undefined
General-purpose register A	A	4	Undefined
General-purpose register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	4	Undefined
Display memory	4	Undefined
Other peripheral circuits	—	*

* See Section 4.1, "Memory Map".

2.3 Test Terminal (TEST)

This terminal is used at the time of the factory inspection of the IC. During normal operation, connect the TEST to VDD.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The S1C621C0 employs the 4-bit core CPU S1C6200A for the CPU, so that register configuration, instructions and so forth are virtually identical to those in other family processors using the S1C6200A.
Refer to "S1C6200/6200A Core CPU Manual" for details about the S1C6200A.
Note the following points with regard to the S1C621C0:

(1) The SLEEP operation is not assumed, so the SLP instruction cannot be used.

(2) RAM is set up to four pages, so only the three low-order bits are valid for the page portion (XP, YP) of the index register that specifies addresses. (The one high-order bit is ignored.)

3.2 ROM

The built-in ROM, a mask ROM for loading the program, has a capacity of 4,096 steps, 12 bits each. The program area is configured of 16 pages (0–15) with 256 steps each (00H–FFH). After initial reset, the program beginning address is page 1, step 00H. The interrupt vector is allocated to each page 1, steps 02H–0BH.

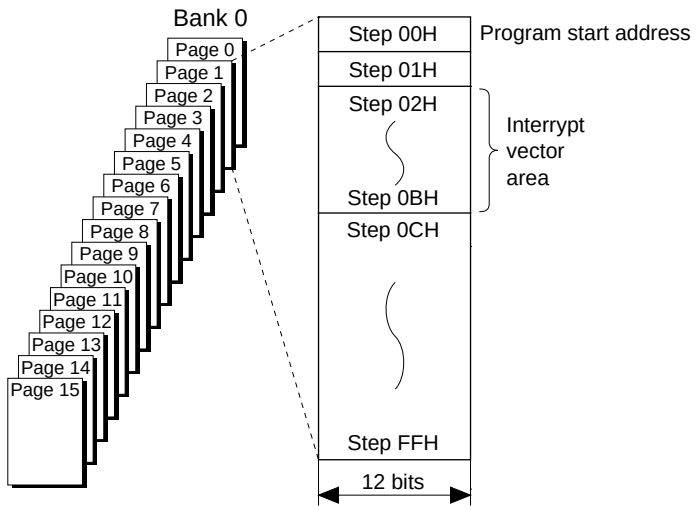


Fig. 3.2.1 ROM configuration

3.3 RAM

The RAM, a data memory storing a variety of data, has a capacity of 208 words, each of four bits. When programming, keep the following points in mind.

(1) Part of the data memory can be used as stack area when subroutine calls and saving registers, so be careful not to overlap the data area and stack area.

(2) Subroutine calls and interrupts take up three words of the stack area.

(3) The data memory 000H–00FH is for the register pointers (RP), and is the addressable memory register area.

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

Peripheral circuits (timer, I/O, and so on) of the S1C621C0 are memory mapped, and interfaced with the CPU. Thus, all the peripheral circuits can be controlled by using the memory operation command to access the I/O memory in the memory map.
The following sections describe how the peripheral circuits operation.

4.1 Memory Map

Data memory of the S1C621C0 has an address space of 297 words, of which 48 words are allocated to display memory and 41 words to I/O memory.
Figure 4.1.1 presents the overall memory maps of the S1C621C0, and Tables 4.1.1(a)–(c) the peripheral circuits' (I/O space) memory maps.
In the S1C621C0 the same I/O memory has been laid out for each page 80H–FCH. As a result, the I/O memory can be accessed without changing over the data memory page. The same result is obtained for I/O memory changes and for readable/writable address references, no matter on what page it is done.

Note: • *The display memory area can be assigned to 050H–07FH or 450H–47FH by software.*

When page 0 (050H–07FH) is selected: read/write is enabled.
When page 4 (450H–47FH) is selected: write only is enabled.

If page 0 is selected, RAM (48 words) is used as the display memory area.

- *Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.*

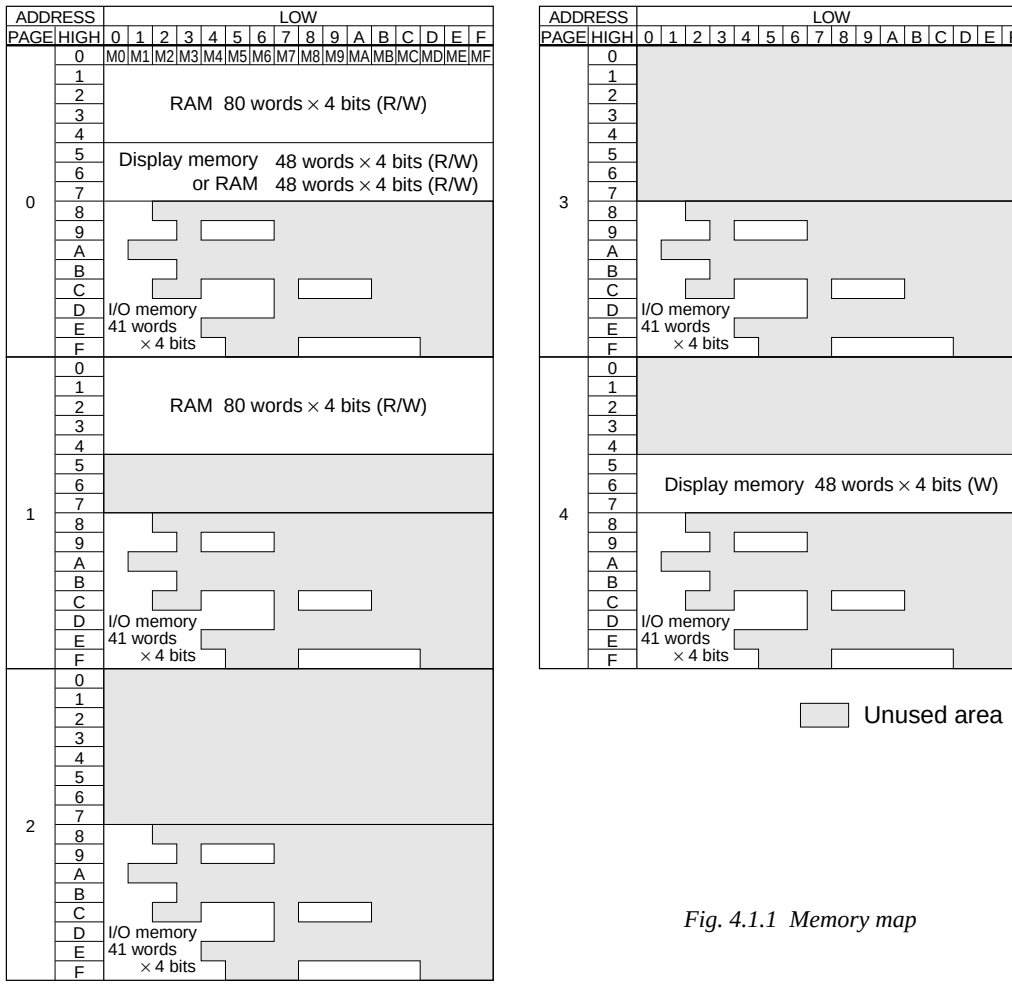


Fig. 4.1.1 Memory map

Table 4.1.1(a) I/O memory map (80H–B2H)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
80H	0	0	SVDDT	SVDON	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	Supply voltage detection data
					SVDON	0	On	Off	SVD circuit On/Off
81H	0	0	CLKCHG	OSCC	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 scillation On/Off
90H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	Interrupt selection register (K00–K03)
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
91H	K03	K02	K01	K00	K03	– *2	High	Low	Input port K00–K03
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
92H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	Input comparison register (K00–K03)
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
94H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	Interrupt selection register (K10–K13)
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
95H	K13	K12	K11	K10	K13	– *2	High	Low	Input port K10–K13
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
96H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	Input comparison register (K10–K13)
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	
A0H	R03 (BZ)	R02 (FOUT)	R01 (REMDC)	R00 (REMCR)	R03	0	High	Low	Output port R03
					R02	0	High	Low	Output port R02
	R/W				R01	0	High	Low	Output port R01
					R00	0	High	Low	Output port R00

Fix at "0" during BZ, FOUT, REMDC and REMCR output

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
B0H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	I/O control register (P00–P03)
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
B1H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	Pull up control register (P00–P03)
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
B2H	P03	P02	P01	P00	P03	1	High	Low	I/O port P00–P03
					P02	1	High	Low	
	R/W				P01	1	High	Low	
					P00	1	High	Low	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

Table 4.1.1(b) I/O memory map (C0H–D6H)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C0H	LDMS	STCD	LDTY1	LDTY0	LDMS	0	0p(R/W)	4p(W)	LCD display memory area selection
					STCD	0	Static	Dynamic	LCD drive switch
	R/W				LDTY1	0			LCD drive duty selection
					LDTY0	0			0: 1/2, 1: 1/3, 2&3: 1/4
C1H	0	0	LOFF	LPWR	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		LOFF	0	All off	Normal	LCD display control
					LPWR	0	On	Off	LCD power supply On/Off
C4H	BZE	0	0	BZFQ	BZE	0	Enable	Disable	Buzzer output enable
					0 *5	– *2			Unused
	R/W	R		R/W	0 *5	– *2			Unused
					BZFQ	0	4,096 Hz	2,048 Hz	Buzzer frequency selection
C5H	FOUTE	0	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					0 *5	– *2			Unused
	R/W	R	R/W		FOFQ1	0			FOUT frequency selection
					FOFQ0	0			0: 512 Hz, 1: 4,096 Hz, 2: f_{OSC1}, 3: f_{OSC3}
C6H	0	0	0	WDRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			W	0 *5	– *2			Unused
					WDRST*5	Reset	Reset	–	Watchdog timer reset
C8H	0	0	TMRUN	TMRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W	W	TMRUN	0	Run	Stop	Clock timer Run/Stop
					TMRST*5	Reset	Reset	–	Clock timer reset
C9H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
CAH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
D0H	DBGOS	RFDBG	RFCLK	RFPWR	DBGOS	0	Sensor	Ref.-R	R/F converter debugging element selection
					RFDBG	0	Debug	Normal	R/F converter debug mode selection
	R/W				RFCLK	0	OSC3	OSC1	R/F converter clock source selection
					RFPWR	0	1	0	Reserved register
D1H	0	0	0	SENS0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					SENS0	0	SEN1	SEN0	Sensor selection
D2H	OVTBC	OVMC	RFRUN	0	OVTBC	0	Overflow	Non-ov	Time base counter overflow flag *6
					OVMC	0	Overflow	Non-ov	Measurement counter overflow flag *6
	R/W			R	RFRUN	0	Run	Stop	R/F converter Run/Stop
					0 *5	– *2			Unused
D3H	MC03	MC02	MC01	MC00	MC03	– *3			Measurement counter MC00–MC03
					MC02	– *3			
	R/W				MC01	– *3			
					MC00	– *3			
D4H	MC07	MC06	MC05	MC04	MC07	– *3			Measurement counter MC04–MC07
					MC06	– *3			
	R/W				MC05	– *3			
					MC04	– *3			
D5H	MC11	MC10	MC09	MC08	MC11	– *3			Measurement counter MC08–MC11
					MC10	– *3			
	R/W				MC09	– *3			
					MC08	– *3			
D6H	MC15	MC14	MC13	MC12	MC15	– *3			Measurement counter MC12–MC15
					MC14	– *3			
	R/W				MC13	– *3			
					MC12	– *3			

Table 4.1.1(c) I/O memory map (E0H–FCH)

address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E0H	0	REMSO	REMDC	REMCR	0 *5	– *2			Unused
					REMSO	0	On	Off	REM soft-timer output control
	R	R/W			REMDC	0	On	Off	REM DC output control
					REMCR	0	On	Off	REM carrier output control
E1H	RCDIV	RCDTY	RT1	RT0	RCDIV	0	fosc3/12	fosc3/8	REM carrier cycle selection
					RCDTY	0			REM carrier duty selection *6
	R/W				RT1	0			REM τ cycle selection
					RT0	0			0: 1/12, 1: 1/16, 2:1/20, 3: 1/32 (x fcarrier)
E2H	RIC3	RIC2	RIC1	RIC0	RIC3	1			REM interrupt τ cycle selection
					RIC2	1			0H = 1τ ... FH = 16τ
	R/W				RIC1	1			
					RIC0	1			
E3H	ROUT3	ROUT2	ROUT1	ROUT0	ROUT3	0			REM carrier output width selection
					ROUT2	0			0H = 0τ ... FH = 15τ
	R/W				ROUT1	0			
					ROUT0	0			
F0H	0	0	0	EIREM	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIREM	0	Enable	Mask	Interrupt mask register (Remote controller)
F1H	0	0	0	EIRF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIRF	0	Enable	Mask	Interrupt mask register (R/F converter)
F2H	0	0	0	EIK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
F3H	0	0	0	EIK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
F4H	0	EIT2	EIT1	EIT0	0 *5	– *2			Unused
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R	R/W			EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
F8H	0	0	0	IREM	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IREM *4	0	Yes	No	Interrupt factor flag (Remote controller)
F9H	0	0	0	IRF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IRF *4	0	Yes	No	Interrupt factor flag (R/F converter)
FAH	0	0	0	IK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
FBH	0	0	0	IK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
FCH	0	IT2	IT1	IT0	0 *5	– *2			Unused
					IT2 *4	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R				IT1 *4	0	Yes	No	Interrupt factor flag (Clock timer 8 Hz)
					IT0 *4	0	Yes	No	Interrupt factor flag (Clock timer 32 Hz)

4.2 Resetting Watchdog Timer

4.2.1 Configuration of watchdog timer

The S1C621C0 incorporates a watchdog timer as the source oscillator for OSC1 (dividing clock = 1 Hz). The watchdog timer must be reset cyclically by the software. If reset is not executed in at least 3 or 4 seconds, the initial reset signal is output automatically for the CPU.
Figure 4.2.1.1 is the block diagram of the watchdog timer.

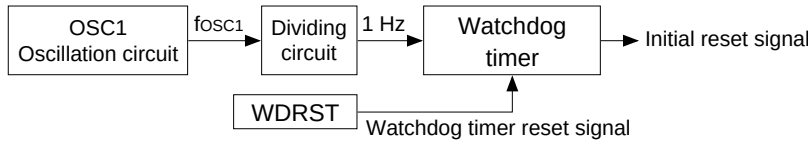


Fig. 4.2.1.1 Watchdog timer block diagram

The watchdog timer, configured of a 2-bit binary counter, generates the initial reset signal internally by overflow of the last stage (1/4 Hz).
Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.
The watchdog timer operates in the HALT mode. If the HALT status continues for 3 or 4 seconds, the initial reset signal restarts operation.

4.2.2 Control of watchdog timer

Table 4.2.2.1 lists the watchdog timer's control bit and its address.

Table 4.2.2.1 Control bit of watchdog timer

Address *7	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
C6H	0	0	0	WDRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			W	0 *5	– *2			Unused
					WDRST*5	Reset	Reset	–	Watchdog timer reset

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

WDRST: Watchdog timer reset (C6H•D0)
This is the bit for resetting the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Always "0"

When "1" is written to WDRST, the watchdog timer is reset, and the operation restarts immediately after this. When "0" is written to WDRST, no operation results.
This bit is dedicated for writing, and is always "0" for reading.

4.2.3 Programming note

When the watchdog timer is being used, the software must reset it within 3-second cycles.

4.3 Oscillation Circuit

4.3.1 Configuration of oscillation circuit

The S1C621C0 has two oscillation circuits (OSC1 and OSC3). The OSC1 oscillation circuit generates main clock of 32.768 kHz (Typ.). The OSC3 oscillation circuit generates sub-clock to drive the CPU and some peripheral circuits (remote controller, R/F converter and FOUT output) in high-speed.
Figure 4.3.1.1 is the block diagram of this oscillation system.

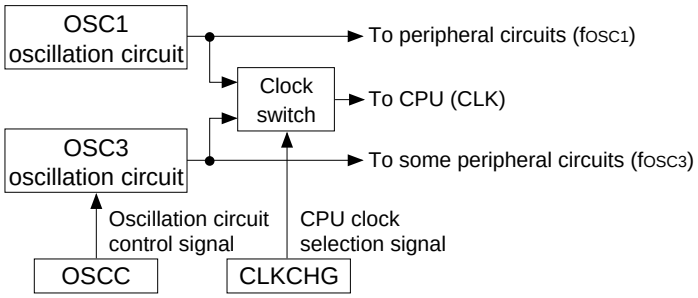


Fig. 4.3.1.1 Oscillation system

At initial reset, the OSC1 oscillation circuit is selected for the CPU operating clock and the OSC3 oscillation circuit is in stop status.
Turning the OSC3 oscillation circuit on and off and switching the system clock (OSC1↔OSC3) can be controlled by the software. The OSC3 oscillation circuit should be used when the CPU and some peripheral circuits need high-speed operation. If it is not necessary, stop the OSC3 oscillation and use OSC1 as the operating clock to reduce current consumption.

4.3.2 OSC1 oscillation circuit

The OSC1 oscillation circuit generates 32.768 kHz (Typ.) system clock.
The OSC1 oscillation clock is used as the system clock when the CPU and the peripheral circuits operate in low-speed (low current consumption). Furthermore, even when OSC3 is used as the system clock, it is still used as the clock source for the clock timer and the watchdog timer.
Figure 4.3.2.1 is the block diagram of the OSC1 oscillation circuit.

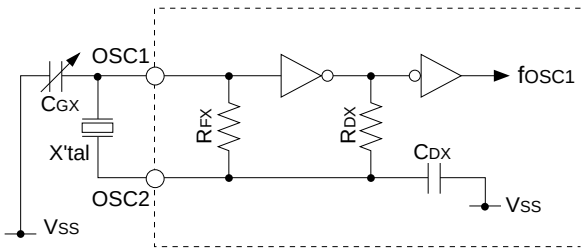
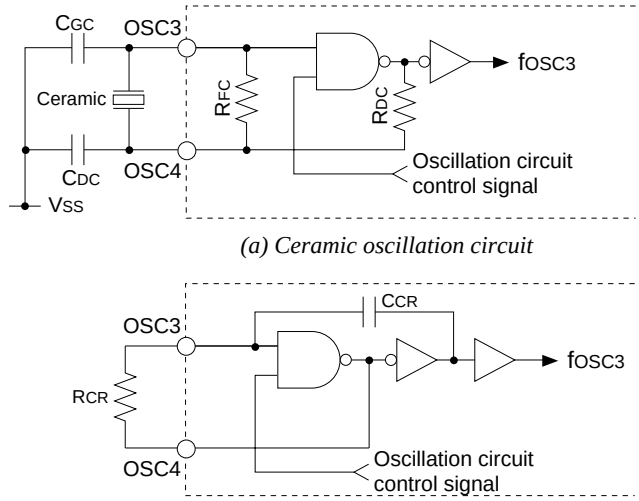


Fig. 4.3.2.1 OSC1 oscillation circuit

As Figure 4.3.2.1 indicates, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator X'tal (Typ. 32.768 kHz) between terminals OSC1 and OSC2 to the trimmer capacitor CGX (5–25 pF) between terminals OSC1 and VSS.

4.3.3 OSC3 oscillation circuit

The OSC3 oscillation circuit generates the system clock to drive the CPU and some peripheral circuits (remote controller, R/F converter and FOUT output) in high-speed.
Either ceramic oscillation or CR oscillation can be selected by the mask option for the oscillation circuit type.
Figure 4.3.3.1 is the block diagram of the OSC3 oscillation circuit.



(a) Ceramic oscillation circuit

(b) CR oscillation circuit

Fig. 4.3.3.1 OSC3 oscillation circuit

When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (Typ. 455 kHz, Max. 1 MHz) between terminals OSC3 and OSC4 to the two capacitors (C_{GC} and C_{DC}) located between terminals OSC3 and OSC4 and V_{SS}.
When CR oscillation is selected, the CR oscillation circuit can be configured simply by connecting the resistor (R_{CR}) between terminals OSC3 and OSC4.

4.3.4 CPU clock switching

The CPU system clock can be switched between OSC1 and OSC3 by the software.
When the CPU operates by OSC1, turning the OSC3 oscillation circuit off can save power.
If high-speed operation is required, turn the OSC3 oscillation circuit on and switch the system clock to OSC3. In this case, switch the clock to OSC3 after 5 msec or more time has elapsed since this time is necessary for stabilizing the oscillation after turning the OSC3 oscillation circuit on. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
When switching from OSC3 to OSC1, turn the OSC3 oscillation circuit off immediately after the clock is switched to OSC1.

4.3.5 Clock frequency and instruction execution time

Table 4.3.5.1 shows the instruction execution time according to each frequency of the system clock.

Table 4.3.5.1 Clock frequency and instruction execution time

Clock frequency	Instruction execution time (µsec)		
	5-clock instruction	7-clock instruction	12-clock instruction
OSC1: 32.768 kHz	152.6	213.6	366.2
OSC3: 455 kHz	11.0	15.4	26.4
OSC3: 1 MHz	5.0	7.0	12.0

4.3.6 Control of oscillation circuit

Table 4.3.6.1 lists the control bits and their addresses for the oscillation circuit.

Table 4.3.6.1 Control bits of oscillation circuit

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
81H	0	0	CLKCHG	OSCC	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

OSCC: OSC3 oscillation ON/OFF (81H•D0)

Controls oscillation ON / OFF for the OSC3 oscillation circuit.

When "1" is written: OSC3 oscillation ON
When "0" is written: OSC3 oscillation OFF
Reading: Valid

When it is necessary to operate the CPU and some peripheral circuits (remote controller, R / F converter, FOUT output) at high speed, set OSCC to "1". At other times, set it to "0" to resume current consumption.
At initial reset, this register is set to "0".

CLKCHG: CPU clock switch (81H•D1)

The CPU's operation clock is selected with this register.

When "1" is written: OSC3 clock is selected
When "0" is written: OSC1 clock is selected
Reading: Valid

When the CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0".
When switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON (OSCC = "1"). This time is necessary to stabilize the OSC3 oscillation.
At initial reset, this register is set to "0".

4.3.7 Programming notes

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

OSC1 → OSC3
1. Set OSCC to "1" (OSC3 oscillation ON)
2. Maintain 5 msec or more
3. Set CLKCHG to "1" (OSC1 → OSC3)

OSC3 → OSC1
1. Set CLKCHG to "0" (OSC3 → OSC1)
2. Set OSCC to "0" (OSC3 oscillation OFF)

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for turning the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(3) If it is not necessary to operate the CPU in high-speed and the OSC3 clock is not needed for some peripheral circuits, turn the OSC3 oscillation circuit off (CLKCHG = "0", OSCC = "0") to reduce current consumption.

4.4 Input Ports (K00–K03, K10–K13)

4.4.1 Configuration of input ports

The S1C621C0 has 8 bits (4-bit × 2) general-purpose input ports. Each of the input port terminals (K00–K03, K10–K13) provides internal pull up resistor. Pull up resistor can be selected for each bit with the mask option.
Figure 4.4.1.1 shows the configuration of input port.

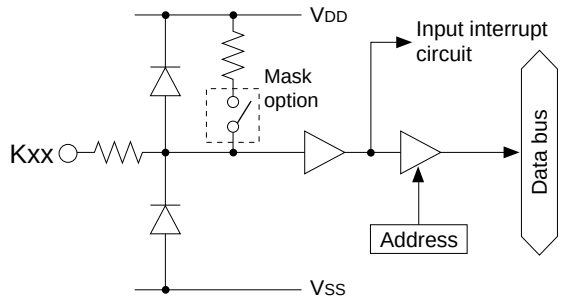


Fig. 4.4.1.1 Configuration of input port

Each of the input port terminals is directly connected to the data bus via a 3-state buffer, and the status of the input signal at the time of the input port reading is loaded as an input data.

4.4.2 Mask option

Internal pull up resistor can be selected for each of the 8 bits of the input ports (K00–K03, K10–K13) with the input port mask option.
Selection of "With pull up resistor" with the mask option suits input from the push switch, key matrix, and so forth.
When input ports are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN}$ + load capacitance on board) × 1.6 [sec]
R_{IN}: pull up resistance (Max. value)
C_{IN}: terminal capacitance (Max. value)

When "Gate direct" is selected, the port can be used for slide switch input and interfacing with other LSIs. In this case, take care that the floating status does not occur for the input.

Select "With pull up resistor" for input ports that are not being used.

4.4.3 Interrupt function

All 8 bits of the input ports (K00–K03, K10–K13) provide the interrupt function. The conditions for issuing an interrupt can be set by the software. Further, whether to mask the interrupt function can be selected by the software.
Figure 4.4.3.1 shows the configuration of K00–K03 (K10–K13) interrupt circuit.

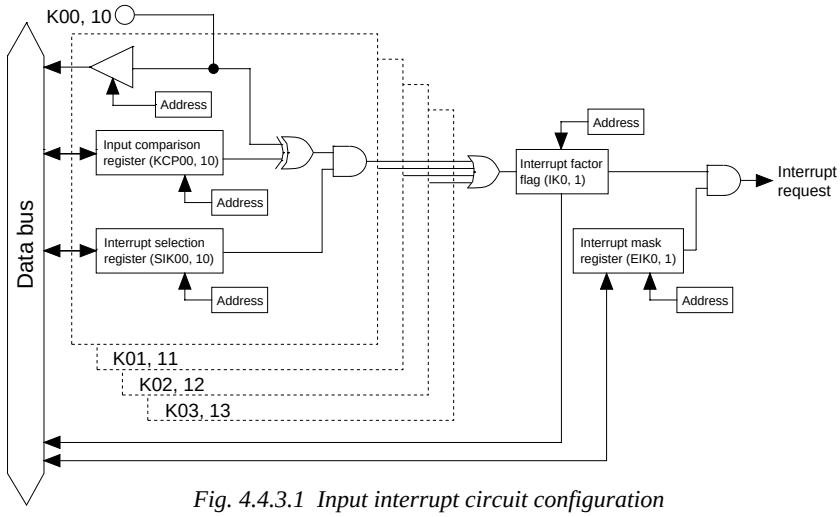


Fig. 4.4.3.1 Input interrupt circuit configuration

The interrupt selection register (SIK) and input comparison register (KCP) are individually set for the input ports K00–K03 and K10–K13, and can specify the terminal for generating interrupt and interrupt timing.
The interrupt selection register (SIK00–SIK03, SIK10–SIK13) select what input of K00–K03 and K10–K13 to use for the interrupt. Writing "1" into an interrupt selection register incorporates that input port into the interrupt generation conditions. The changing the input port where the interrupt selection register has been set to "0" does not affect the generation of the interrupt.
The input interrupt timing can select that the interrupt be generated at the rising edge of the input or that it be generated at the falling edge according to the set value of the input comparison register (KCP00–KCP03).
By setting these two conditions, the interrupt for K00–K03 and K10–K13 (4 bits unit) are generated when an input port in which an interrupt has been enabled by the input selection register and the content of the input comparison register have been changed from matching to no matching.
The interrupt mask registers EIK0 and EIK1 enable the interrupt mask to be selected for K00–K03 and K10–K13, respectively.
When the interrupt is generated, the interrupt factor flag (IK0 for K00–K03, IK1 for K10–K13) is set to "1".
Figure 4.4.3.2 shows an example of an interrupt for K00–K03.

Interrupt selection register

SIK03	SIK02	SIK01	SIK00
1	1	1	0

Input comparison register

KCP03	KCP02	KCP01	KCP00
1	0	1	0

With the above setting, the interrupt of K00–K03 is generated under the following condition:

Input port

	K03	K02	K01	K00	
(1)	1	0	1	0	(Initial value)
(2)	1	0	1	1	
(3)	0	0	1	1	→ Interrupt generation
(4)	0	1	1	1	

Because K00 interrupt is set to disable, interrupt will be generated when no matching occurs between the contents of the 3 bits K01–K03 and the 3 bits input comparison register KCP01–KCP03.

Fig. 4.4.3.2 Example of interrupt of K00–K03

K00 interrupt is disabled by the interrupt selection register (SIK00), so that an interrupt does not occur at (2). At (3), K03 changes to "0"; the data of the terminal that is interrupt enabled no longer matches the data of the input comparison register, so that interrupt occurs. As already explained, the condition for the interrupt to occur is the change in the port data and contents of the input comparison register from matching to no matching. Hence, in (4), when the no matching status changes to another no matching status, an interrupt does not occur. Further, terminals that have been masked for interrupt do not affect the conditions for interrupt generation.

4.4.4 Control of input ports

Table 4.4.4.1 lists the input ports control bits and their addresses.

Table 4.4.4.1 Input port control bits

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
90H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	Interrupt selection register (K00–K03)
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
91H	K03	K02	K01	K00	K03	– *2	High	Low	Input port K00–K03
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
92H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	Input comparison register (K00–K03)
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
94H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	Interrupt selection register (K10–K13)
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
95H	K13	K12	K11	K10	K13	– *2	High	Low	Input port K10–K13
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
96H	KCP13	KCP12	KCP11	KCP1	KCP13	1	↓	↑	Input comparison register (K10–K13)
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	
F2H	0	0	0	EIK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
F3H	0	0	0	EIK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FAH	0	0	0	IK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
FBH	0	0	0	IK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

K00–K03, K10–K13: Input port data (91H, 95H)

Input data of the input port terminals can be read with these registers.

When "1" is read:	High level
When "0" is read:	Low level
Writing:	Invalid

The reading is "1" when the terminal voltage of the 8 bits of the input ports (K00–K03, K10–K13) goes high (V_{DD}), and "0" when the voltage goes low (V_{SS}).
These bits are dedicated for reading, so writing cannot be done.

KCP00–KCP03, KCP10–KCP13: Input comparison registers (92H, 96H)

Interrupt conditions for terminals K00–K03 and K10–K13 can be set with these registers.

When "1" is written:	Falling edge
When "0" is written:	Rising edge
Reading:	Valid

The interrupt conditions can be set for the rising or falling edge of input for each of the eight bits (K00–K03 and K10–K13), through the input comparison registers (KCP00–KCP03 and KCP10–KCP13).
For KCP00–KCP03, a comparison is done only with the ports that are enabled by the interrupt among K00–K03 by means of the SIK00–SIK03 registers. For KCP10–KCP13, a comparison is done only with the ports that are enabled by the interrupt among K10–K13 by means of the SIK10–SIK13 registers.
At initial reset, these registers are set to "1".

SIK00–SIK03, SIK10–SIK13: Interrupt selection registers (90H, 94H)

Selects the port to be used for the K00–K03 and K10–K13 input interrupt.

When "1" is written:	Enable
When "0" is written:	Disable
Reading:	Valid

Enables the interrupt for the input ports (K00–K03, K10–K13) for which "1" has been written into the interrupt selection register (SIK00–SIK03, SIK10–SIK13). The input port set for "0" does not affect the interrupt generation condition.
At initial reset, these registers are set to "0".

EIK0, EIK1: Interrupt mask registers (F3H•D0, F2H•D0)

Masking the interrupt of the input port can be selected with these registers.

When "1" is written:	Enable
When "0" is written:	Mask
Reading:	Valid

With these registers, masking of the input port can be selected for each of the two systems (K00–K03, K10–K13).
At initial reset, these registers are all set to "0".

IK0, IK1: Interrupt factor flags (FBH•D0, FAH•D0)

These flags indicate the occurrence of input interrupt.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

The interrupt factor flags IK0 and IK1 are associated with K00–K03 and K10–K13, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred.
These flags are set to "1" by generating the corresponding interrupt factor regardless of the interrupt mask register (EIK0, EIK1) settings.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.
These flags are reset when the software reads them.
At initial reset, these flags are set to "0".

4.4.5 Programming notes

(1) When input ports are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN}$ + load capacitance on board) $\times$ 1.6 [sec]
R_{IN}: pull up resistance (Max. value)
C_{IN}: terminal capacitance (Max. value)

(2) When the input comparison register (KCP00–KCP03, KCP10–KCP13) is set, the interrupt factor flag (IK0, IK1) may be set to "1" depending on the status of the input port terminal. Consequently, when setting this register, do it in the DI status (interrupt flag = "0") and then read the interrupt factor flag in order to reset, or after setting the interrupt selection register (SIK00–SIK03, SIK10–SIK13) to the interrupt disabled status.

(3) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

4.5 Output Ports (R00–R03)

4.5.1 Configuration of output ports

The S1C621C0 has 4 bits general output ports.
Output specifications of the output ports can be selected individually with the mask option. Two kinds of output specifications are available: complementary output and Nch open drain output.
Further, the output port R00–R03 to be used as special output ports by the software setting.
Figure 4.5.1.1 shows the configuration of the output port.

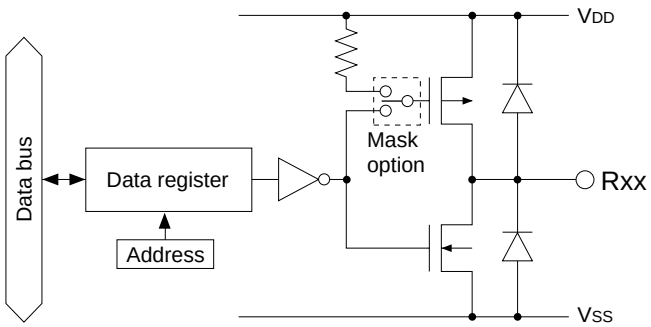


Fig. 4.5.1.1 Configuration of output port

4.5.2 Mask option

Output specifications of the output ports can be selected with the mask option.
Output specifications for the output ports (R00–R03) enable selection of either complementary output or Nch open drain output for each of the 4 bits.
The Nch open drain output is suitable for the common output for key matrix and the other outputs. However, even when Nch open drain output is selected, voltage exceeding source voltage must not be applied to the output port.
Select complementary output set in default for unused output port.

4.5.3 Special output

In addition to the regular DC output, special output can be selected for the output ports R00–R03 as shown in Table 4.5.3.1 with the software. Figure 4.5.3.1 shows the configuration of the special output.

Table 4.5.3.1 Special output

Terminal	Special output	Output enable register
R03	BZ	BZE
R02	FOUT	FOUTE
R01	REMDC	REMDC
R00	REMCR	REMCR

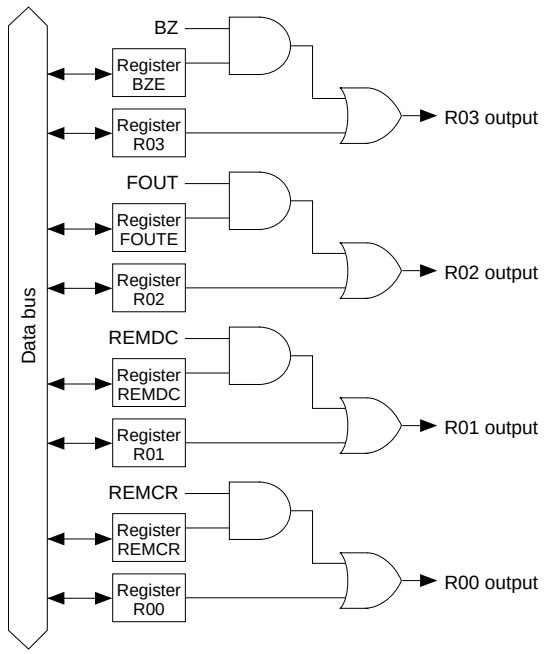


Fig. 4.5.3.1 Configuration of special output

At initial reset, the output terminals are set to low (V_{SS}).
When an R0x is used as the special output port, fix the output port register R0x at "0" and turn the signal ON or OFF using the special output enable register.

Note: Be sure that the output terminal is fixed at a high (V_{DD}) level the same with the DC output if "1" is written to the R0x register when the special output has been selected.

• REMCR (R00) and REMDC (R01) outputs

REMCR (remote control carrier) signal generated by the built-in remote controller can be output from the R00 terminal.
This output signal is used to drive the LED for an infrared remote controller so that the remote control signal is transmitted.
Similarly, REMDC (DC) signal that has not yet done pulse modulation can be output from the R01 terminal.
When R00 is used for REMCR output, keep R00 register set to "0". The signal output can be controlled using the REMCR register. When the REMCR register is set to "1", the REM (remote controller) circuit goes on and shifts to the status in which the REMCR signal can be output from the R00 terminal. When "0" is set, the R00 terminal goes low level (V_{SS}).
When R01 is used for REMDC output, keep the R01 register set to "0". The signal output can be controlled using the REMDC register. When the REMDC register is set to "1", the REM (remote controller) circuit goes on and shifts to the status in which the REMDC signal can be output from the R01 terminal. When "0" is set, the R01 terminal goes low level (V_{SS}).
See Section 4.9, "Remote Controller (REM)" for the output waveform and output timing.

• FOUT (R02)

In order for the S1C621C0 to provide clock signal to an external device, FOUT signal can be output from the R02 terminal.
When R02 is used for FOUT output, keep R02 register set to "0". ON / OFF of the signal output can be controlled using the FOUT output enable register FOUTE.
When the FOUTE register is set to "1", FOUT signal is output from the R02 terminal. When "0" is set, the R02 terminal goes low level (V_{SS}).
The frequency of clock output signal may be selected from among 4 types as Table 4.5.3.2 by setting of the FOFQ0 and FOFQ1 registers.

Table 4.5.3.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency (Hz)
0	0	512
0	1	4,096
1	0	f_{OSC1}
1	1	f_{OSC3}

f_{OSC1}: OSC1 oscillation frequency
f_{OSC3}: OSC3 oscillation frequency

Note: A hazard may occur when the FOUT signal is turned ON or OFF.

Figure 4.5.3.2 shows the output waveform of FOUT.

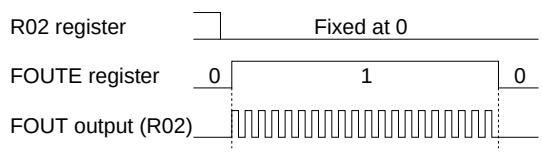


Fig. 4.5.3.2 Output waveform of FOUT

• BZ (R03)

BZ is the buzzer signal output for driving the piezo-electric buzzer, and it can be output from the R03 terminal.
When R03 is used for BZ output, keep R03 register set to "0". ON / OFF of the signal output can be controlled by the BZE register.
When the BZE register is set to "1", BZ signal is output from the R03 terminal. When "0" is set, the R03 terminal goes low level (VSS).
The buzzer frequency can be selected as 2,048 Hz or 4,096 Hz by setting of the BZFQ register. When the BZFQ register is set to "0", the frequency is set to 2,048 Hz, and to 4,096 Hz when "1" is set.

Note: A hazard may occur when the BZ signal is turned ON or OFF.

Figure 4.5.3.3 shows the output waveform of BZ.

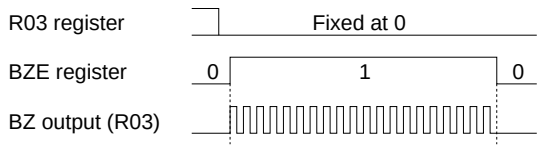


Fig. 4.5.3.3 Output waveform of BZ

4.5.4 Control of output ports

Table 4.5.4.1 lists the output ports' control bits and their addresses.

Table 4.5.4.1 Control bits of output ports

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
A0H	R03 (BZ)	R02 (FOUT)	R01 (REMDC)	R00 (REMCR)	R03	0	High	Low	Output port R03
					R02	0	High	Low	Output port R02
					R01	0	High	Low	Output port R01
	R/W				R00	0	High	Low	Output port R00
C4H	BZE	0	0	BZFQ	BZE	0	Enable	Disable	Buzzer output enable
					0 *5	– *2			Unused
	R/W	R		R/W	0 *5	– *2			Unused
					BZFQ	0	4,096Hz	2,048Hz	Buzzer frequency selection
C5H	FOUTE	0	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					0 *5	– *2			Unused
	R/W	R	R/W		FOFQ1	0			FOUT frequency selection
					FOFQ0	0			0: 512 Hz, 1: 4,096 Hz, 2: fOSC1, 3: fOSC3
E0H	0	REMSO	REMDC	REMCR	0 *5	– *2			Unused
					REMSO	0	On	Off	REM soft-timer output control
	R	R/W			REMDC	0	On	Off	REM DC output control
					REMCR	0	On	Off	REM carrier output control

Fix at "0" during BZ, FOUT, REMDC and REMCR output

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

R00–R03: Output port data (A0H)

Sets the output data for the output ports.

When "1" is written: High output
When "0" is written: Low output
Reading: Valid

The output port terminals output the data written in the corresponding registers (R00–R03) without changing it. When "1" is written in the register, the output port terminal goes high (VDD), and when "0" is written, the output port terminal goes low (VSS).
The registers R00–R03 that are used as special output should be fixed at "0".
At initial reset, these registers are set to "0".

REMCR: REM carrier output control register (E0H•D0)

Controls the REMCR (remote control carrier) output.

When "1" is written: REMCR output enable
When "0" is written: REMCR output disable
Reading: Valid

By writing "1" to REMCR when "0" has been set to the R00 register, the REMCR signal is output from the R00 terminal. When "0" is written, the R00 terminal goes low level (VSS).
When R00 is used for DC output, keep REMCR register set to "0".
At initial reset, this register is set to "0".
See Section 4.9, "Remote Controller (REM)" for the REMCR signal.

REMDC: REM DC output control register (E0H•D1)

Controls the REMDC (remote control DC) output.

When "1" is written: REMDC output enable
When "0" is written: REMDC output disable
Reading: Valid

By writing "1" to REMDC when "0" has been set to the R01 register, the REMDC signal is output from the R01 terminal. When "0" is written, the R01 terminal goes low level (VSS).
When R01 is used for DC output, keep REMDC register set to "0".
At initial reset, this register is set to "0".
See Section 4.9, "Remote Controller (REM)" for the REMDC signal.

FOUTE: FOUT output enable register (C5H•D3)

Controls the FOUT output.

When "1" is written: FOUT output enable
When "0" is written: FOUT output disable
Reading: Valid

By writing "1" to FOUTE when "0" has been set to the R02 register, the FOUT signal is output from the R02 terminal. When "0" is written, the R02 terminal goes low level (VSS) .
When R02 is used for DC output, keep FOUTE register set to "0".
At initial reset, this register is set to "0".

FOFQ0, FOFQ1: FOUT frequency selection register (C5H•D0, D1)

Selects the FOUT frequency.

Table 4.5.4.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency (Hz)
0	0	512
0	1	4,096
1	0	fOSC1
1	1	fOSC3

fOSC1: OSC1 oscillation frequency
fOSC3: OSC3 oscillation frequency

At initial reset, these registers are set to "0".

BZE: BZ output enable register (C4H•D3)

Controls the BZ output.

When "1" is written: BZ output enable
When "0" is written: BZ output disable
Reading: Valid

By writing "1" to BZE when "0" has been set to the R03 register, the BZ signal is output from the R03 terminal. When "0" is written, the R03 terminal goes low level (VSS).
When R03 is used for DC output, keep BZE register set to "0".
At initial reset, this register is set to "0".

BZFQ: BZ frequency selection register (C4H•D0)

Selects the frequency of the BZ signal.

When "1" is written:	4,096 Hz
When "0" is written:	2,048 Hz
Reading:	Valid

Select the frequency of the BZ signal when the R03 port is set to BZ output. By writing "1" to BZFQ, the frequency of the BZ signal is set to 4,096 Hz. When "0" is written, it is set to 2,048 Hz.
At initial reset, this register is set to "0".

4.5.5 Programming notes

(1) When R00–R03 are used as DC output, the special output enable registers REMCR (R00), REMDC (R01), FOUTE (R02) and BZE (R03) should be fixed at "0".

(2) When the special output is selected, the corresponding output port register (R00–R03) should be fixed at "0". Be aware that the output terminal is fixed at a high (V_{DD}) level the same with the DC output if "1" is written to the R00–R03 register when the special output has been selected.

(3) When BZ and FOUT are selected, a hazard may be observed in the output waveform when the data of the output register changes.

(4) When selecting f_{OSC3} as the FOUT clock frequency, it is necessary to control the OSC3 oscillation circuit. See Section 4.3, "Oscillation Circuit" for details of the control.

4.6 I/O Ports (P00–P03)

4.6.1 Configuration of I/O ports

The S1C621C0 has 4 bits general-purpose I/O ports. Figure 4.6.1.1 shows the configuration of the I/O port. The 4 bits of the I/O ports P00–P03 can be set to either input mode or output mode. Modes can be set by writing data to the I/O control register.
Moreover, pull up resistor which is turned ON during input mode can be controlled by the software.

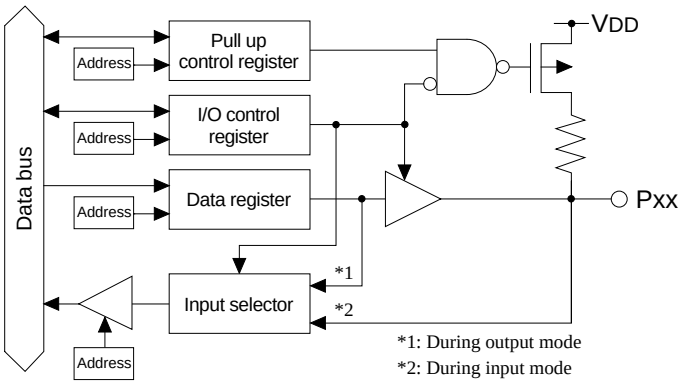


Fig. 4.6.1.1 Configuration of I/O port

4.6.2 I/O control registers and input/output mode

Input or output mode can be set for the 4 bits of I/O ports P00–P03 by writing data into the corresponding I/O control registers IOC00–IOC03.

To set the input mode, write "0" to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.
However, when the pull up explained in the following section has been set by software, the input line is pulled up only during this input mode.

The output mode is set when "1" is written to the I/O control register. When an I/O port set to output mode works as an output port, it outputs a high level (V_{DD}) when the port output data is "1", and a low level (V_{SS}) when the port output data is "0".

If perform the read out in each mode; when output mode, the register value is read out, and when input mode, the port value is read out.

At initial reset, the I/O control registers are set to "0", and the I/O port enters the input mode.

4.6.3 Pull up during input mode

A pull up resistor that operates during the input mode is built into the I/O ports of the S1C621C0. Software can set the use or non-use of this pull up. The pull up resistor becomes effective by writing "1" into the pull up control registers PUL00–PUL03 that correspond to each of P00–P03, and the input line is pulled up during the input mode. When "0" has been written, no pull up is done.
At initial reset, the pull up control registers are set to "1".

4.6.4 Control of I/O ports

Table 4.6.4.1 lists the I/O ports' control bits and their addresses.

Table 4.6.4.1 Control bits of I/O ports

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
B0H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	I/O control register (P00–P03)
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
B1H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	Pull up control register (P00–P03)
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
B2H	P03	P02	P01	P00	P03	1	High	Low	I/O port P00–P03
					P02	1	High	Low	
	R/W				P01	1	High	Low	
					P00	1	High	Low	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

P00–P03: I/O port data (B2H)

I/O port data can be read and output data can be set through these ports.

• ***When writing data***

When "1" is written: High level
When "0" is written: Low level

When an I/O port is set to the output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (V_{DD}), and when "0" is written, the level goes low (V_{SS}).
Port data can be written also in the input mode.

• ***When reading data out***

When "1" is read: High level
When "0" is read: Low level

When the I/O port is in the input mode the voltage level being input to the port terminal can be read out; in the output mode the register value can be read. When the terminal voltage in the input mode is high (V_{DD}) the port data that can be read is "1", and when the terminal voltage is low (V_{SS}) the data is "0".
When PUL register is set to "1", the built-in pull up resister goes ON during input mode, so that the I/O port terminal is pulled up. The gate floating has not occur by the input control signal even if the PUL register is set to "0" and no pull up register is set.

When input terminals are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching data during input mode, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN}$ + load capacitance on board) $\times$ 1.6 [sec]

R_{IN}: pull up resistance (Max. value)
C_{IN}: terminal capacitance (Max. value)

IOC00–IOC03: I/O control registers (B0H)

The input and output modes of the I/O ports can be set with these registers.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

The input and output modes of the I/O ports are set in units of one bit. IOC00–IOC03 set the mode for P00–P03, respectively.
Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.
At initial reset, these registers are set to "0", so the I/O ports are in the input mode.

PUL00–PUL03: Pull up control registers (B1H)

The pull up during the input mode can be set with these registers.

When "1" is written: Pull up ON
When "0" is written: Pull up OFF
Reading: Valid

The built-in pull up resistor which is turned ON during input mode is set to enable in units of one bit.
PUL00–PUL03 set the pull up for P00–P03, respectively.
By writing "1" to the pull up control register, the corresponding I/O ports are pulled up (during input mode), while writing "0" turns the pull up function OFF.
At initial reset, these registers are set to "1", so the pull up function is set to ON.

4.6.5 Programming note

When input terminals are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching data during input mode, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN}$ + load capacitance on board) $\times 1.6$ [sec]

R_{IN}: pull up resistance (Max. value)
C_{IN}: terminal capacitance (Max. value)

4.7 LCD Driver (COM0–COM3, SEG0–SEG33)

4.7.1 Configuration of LCD driver

The S1C621C0 has 4 common terminals (COM0–COM3) and 34 segment terminals (SEG0–SEG33), so that it can drive an LCD with a maximum of 136 (34 × 4) segments.
The power for driving the LCD is generated by the internal circuit so that there is no need to apply power especially from outside.
The driving method is 1/2 duty dynamic drive depending on the four types of potential, V_{SS}, V_{C1}, V_{C2} and V_{C3}. In addition to the 1/2 duty, 1/3 and 1/4 drive duty can be selected by the software. The frame frequency is 32 Hz for 1/4 and 1/2 duty, and 42.7 Hz for 1/3 duty (f_{OSC1} = 32.768 kHz).
LCD display ON/OFF may be controlled by the software.

Note: "f_{OSC1}" indicates the oscillation frequency of the OSC1 oscillation circuit.

4.7.2 LCD drive voltage

The LCD drive voltage V_{C1} is generated by the LCD system regulated voltage circuit, and V_{C2} and V_{C3} are generated by boosting the V_{C1} voltage with the LCD system voltage booster circuit.
The V_{C1} voltage can be adjusted to match the LCD panel characteristics using the V_{ADJ} terminal. See Section 2.1.2, "Voltage <V_{C1}, V_{C2} and V_{C3}> for LCD driving" for the V_{C1} adjustment method.
The LCD system power circuit that generates V_{C1}–V_{C3} is turned ON and OFF by the LCD power control register LPWR.
By setting LPWR to "1", the LCD system power circuit generates V_{C1}–V_{C3}. When LPWR is set to "0", V_{C1}–V_{C3} become V_{SS} level. In this case, all outputs from the COM terminals and SEG terminals go to V_{SS} level.
To display the LCD, the LCD drive power must be ON by previously setting LPWR to "1".
SEG output ports that are set for DC output by the mask option operate same as the output (R) port regardless of the power ON/OFF control.

4.7.3 LCD display ON/OFF control and duty switching

(1) Display ON/OFF control

In the S1C621C0, ON/OFF of the LCD display can be controlled by the LOFF register.
At initial reset, LOFF is set to "0", and the LCD display is set to the ON status.
The LCD power is OFF at initial reset, so the display is actually performed when the LCD power is turned ON (LPWR = "1").
To set all of the LCD display OFF, write "1" to LOFF. With this, the SEG terminals output an OFF waveform.

(2) Switching of drive duty

By setting the registers LDTY0 and LDTY1, the LCD drive duty can be selected from among 3 types, 1/4, 1/3 and 1/2 duty. Table 4.7.3.1 shows the LCD drive duty setting.

Table 4.7.3.1 LCD drive duty setting

LDTY1	LDTY0	Duty	Terminals used in common	Maximum number of segments	Frame frequency *
0	0	1/2	COM0, COM1	68 (34 × 2)	f_{OSC1}/1,024 (32 Hz)
0	1	1/3	COM0–COM2	102 (34 × 3)	f_{OSC1}/768 (42.7 Hz)
1	X	1/4	COM0–COM3	136 (34 × 4)	f_{OSC1}/1,024 (32 Hz)

* In case of f_{OSC1} = 32.768 kHz

Basically you should select the drive duty with the smallest drive segment number (for example, 1/3 duty for 100 segments and 1/2 duty for 60 segments) from among the drive duties permitting driving of the segment number of the LCD panel.
Figures 4.7.3.1–4.7.3.3 show the dynamic drive waveform for 1/4 duty, 1/3 duty and 1/2 duty.

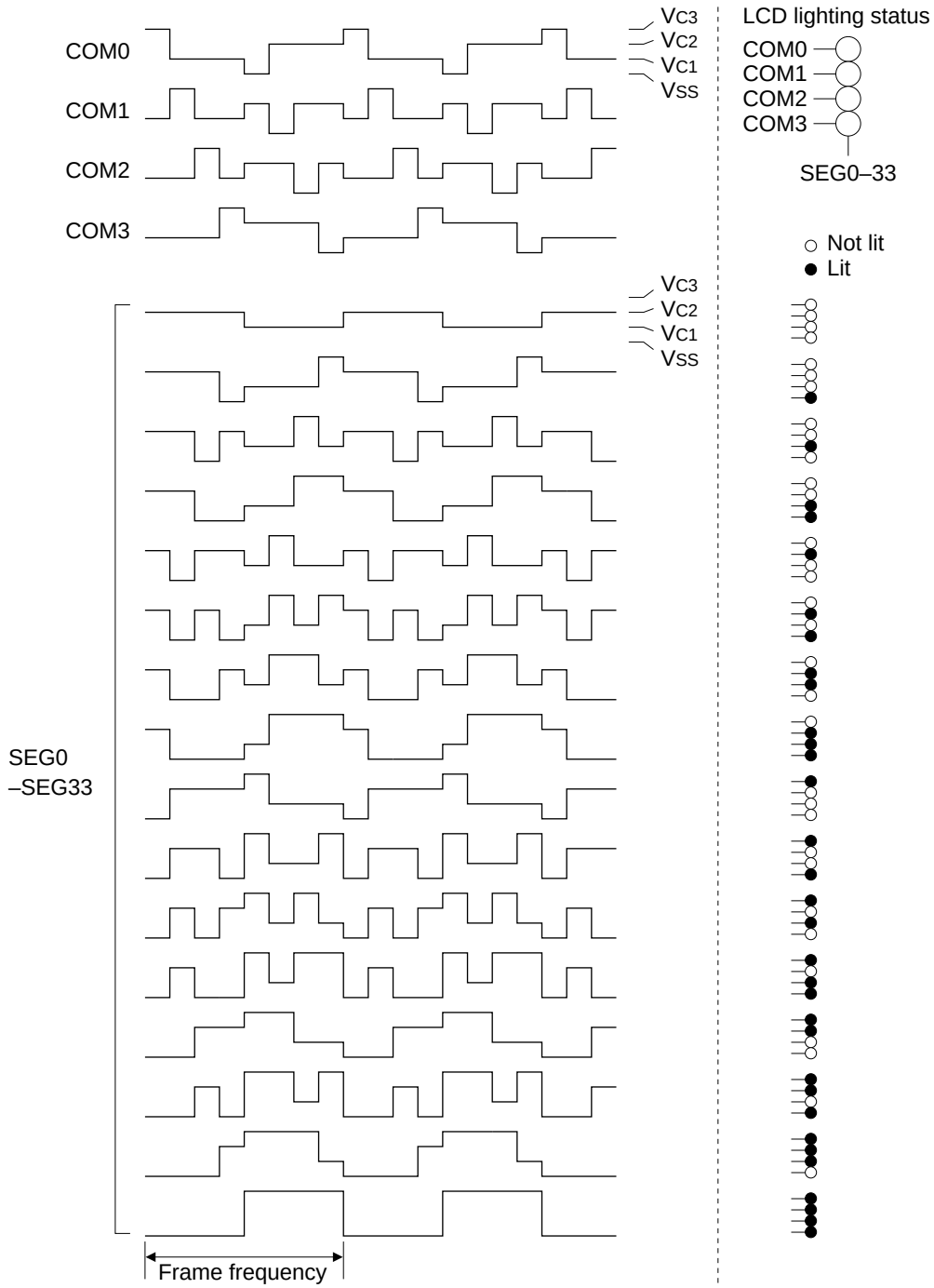


Fig. 4.7.3.1 Drive waveform for 1/4 duty

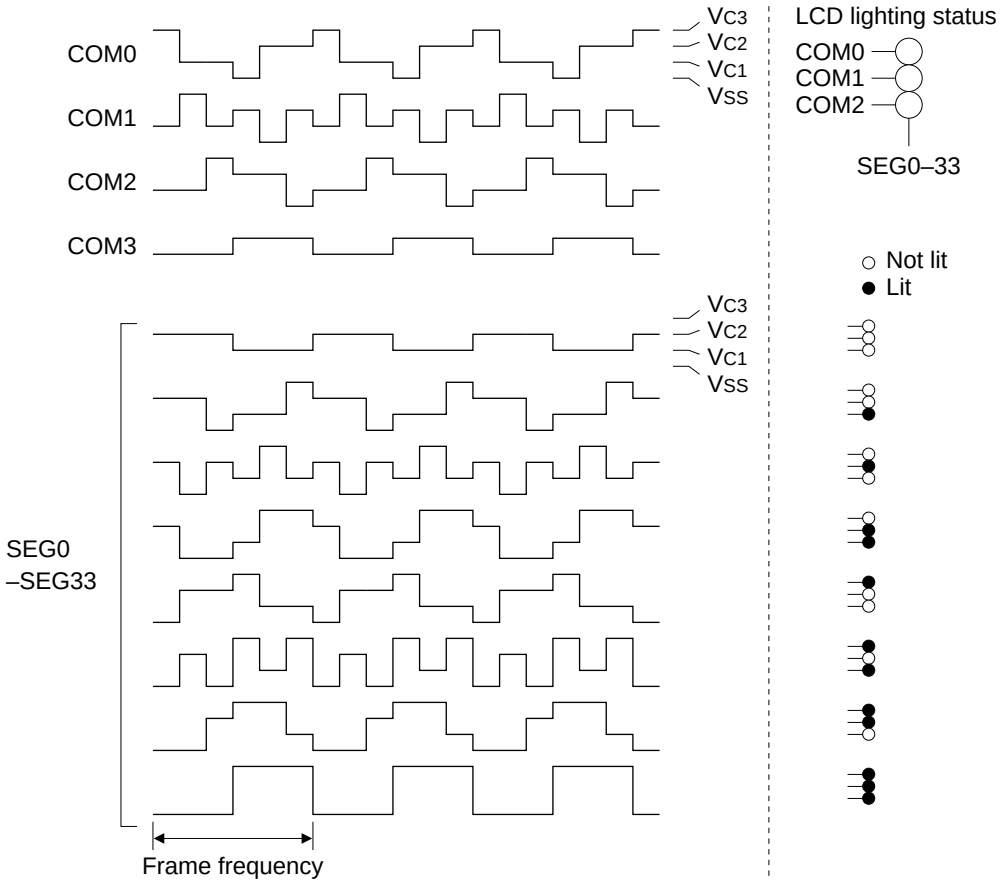


Fig. 4.7.3.2 Drive waveform for 1/3 duty

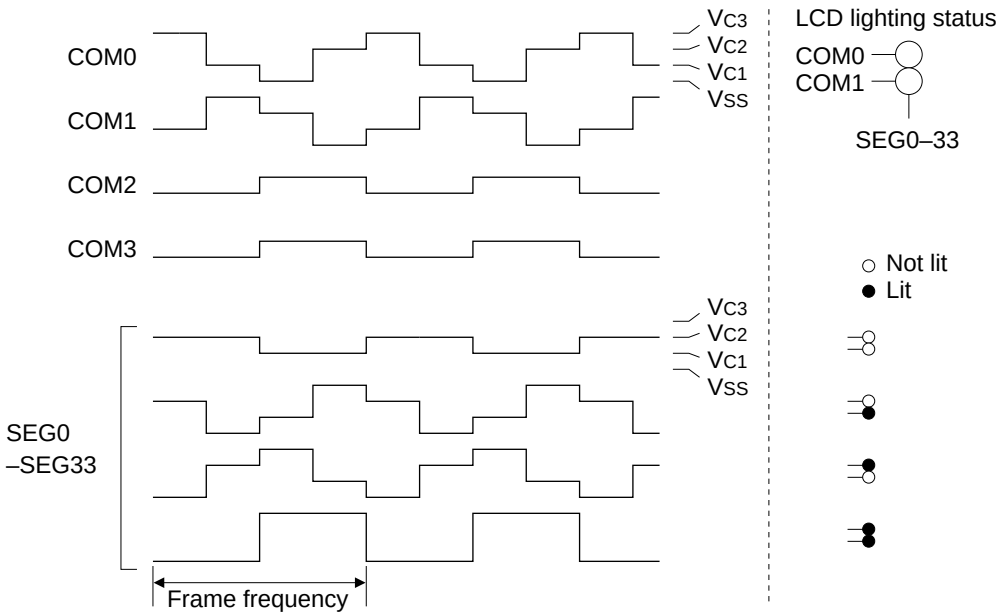


Fig. 4.7.3.3 Drive waveform for 1/2 duty

4.7.4 Switching between dynamic and static drive

The S1C621C0 provides software setting of the LCD static drive.
The frame frequency during static driving is fixed at 32 Hz (when f_{OSC1} = 32.768 kHz) regardless of the drive duty selection.
This function enables easy adjustment (cadence adjustment) of the oscillation frequency of the OSC1 oscillation circuit (crystal oscillation circuit).

The procedure for executing static drive of the LCD is as follows:

① Write "1" to register STCD at address C0H • D2.

② Write the same value to all registers corresponding to COM0–COM3 of the display memory.

Note: • When setting the static drive, all the COM outputs become effective regardless of the drive duty selection. Hence, for static drive, set the same value to all display memory corresponding to COM0–COM3 even when a drive duty other than 1/4 duty has been selected.

• For cadence adjustment, set the display data corresponding to COM0–COM3, so that all the LCDs light.

Figure 4.7.4.1 shows the drive waveform for static drive.

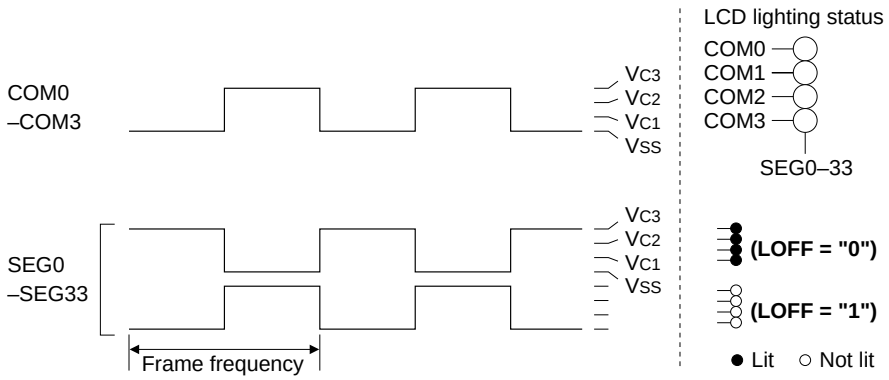


Fig. 4.7.4.1 LCD static drive waveform

4.7.5 Display memory area

The display memory is allocated in the data memory area, addresses 50H–7FH in page 0 or page 4. Either of the areas used can be selected using the software (LDMS register).
By setting LDMS to "1", page 0 is selected and addresses 050H–07FH become the display memory. Since a RAM has been allocated in this area, it can be used as the display memory for reading / writing. For this reason, control in a bit unit can simply be done using an arithmetic instruction. However, this area should not be used for general purpose RAM. Unused addresses for the display memory within the area (48 words × 4 bits) can be used as a general purpose RAM.
At initial reset, LDMS is set to "0" and page 4 (450H–47FH) becomes the display memory. When this area is selected, all the internal RAM can be used as general purpose RAM. However, since the display memory is write only, data modification by arithmetic instructions cannot be done.
Correspondence between segment outputs and bits within the display memory can be optionally set by the mask option explained in the next section.

4.7.6 Mask option (segment allocation)

(1) Segment allocation

The LCD driver has a segment decoder built-in, and the data bit (D0–D3) of the optional address in the display memory area (50H–7FH) can be allocated to the optional segment. This makes design easy by increasing the degree of freedom with which the liquid crystal panel can be designed.
The allocated segment displays when the bit for the display memory is set to "1", and goes out when bit is set to "0".

Figure 4.7.6.1 shows an example of the relationship between the LCD segments (on the panel) and the display memory for the case of 1/3 duty.

Address	Data			
	D3	D2	D1	D0
7AH	d	c	b	a
7BH	p	g	f	e
7CH	d'	c'	b'	a'
7DH	p'	g'	f'	e'

Display memory allocation

	Common 0	Common 1	Common 2
SEG10	7A, D0 (a)	7B, D1 (f)	7B, D0 (e)
SEG11	7A, D1 (b)	7B, D2 (g)	7A, D3 (d)
SEG12	7D, D1 (f')	7A, D2 (c)	7B, D3 (p)

Pin address allocation

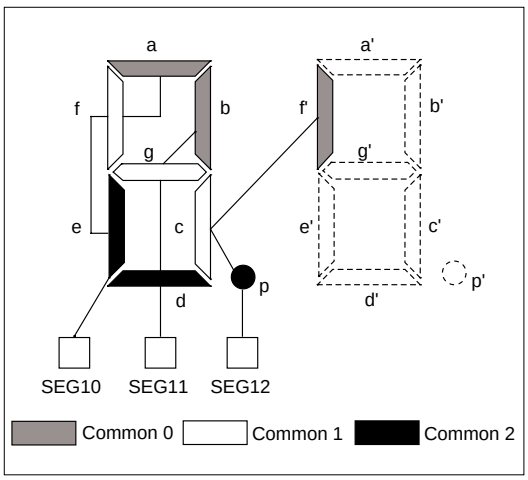


Fig. 4.7.6.1 Segment allocation

(2) Output specification

① The segment terminals (SEG0–SEG33) can be selected with the mask option in each pair for either segment signal output or DC output (V_{DD} and V_{SS} binary output).
When DC output is selected, the data corresponding to COM0 of each segment terminal is output.

② When DC output is selected, either complementary output or Nch open drain output can be selected for each terminal with the mask option.

Note: The terminal pairs are the combination of SEG2 × n and SEG2 × n + 1 (where n is an integer from 0 to 16).

4.7.7 Control of LCD driver

Table 4.7.7.1 shows the LCD driver's control bits and their addresses. Figure 4.7.7.1 shows the display memory map.

Table 4.7.7.1 LCD driver control bits

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C0H	LDMS	STCD	LDTY1	LDTY0	LDMS	0	0p(R/W)	4p(W)	LCD display memory area selection
					STCD	0	Static	Dynamic	LCD drive switch
	R/W				LDTY1	0			LCD drive duty selection
					LDTY0	0			0: 1/2, 1: 1/3, 2&3: 1/4
C1H	0	0	LOFF	LPWR	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		LOFF	0	All off	Normal	LCD display control
					LPWR	0	On	Off	LCD power supply On/Off

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 or 4	5	Display memory (48 words x 4 bits) Page 0: R/W Page 4: W															
	6																
	7																

Fig. 4.7.7.1 Display memory map

LPWR: LCD power supply ON/OFF (C1H•D0)

Controls the LCD power ON and OFF

When "1" is written: Power ON
When "0" is written: Power OFF
Reading: Valid

By writing "1" to LPWR, the LCD power goes ON.
When "0" is written, the LCD power goes OFF and all terminals of the COM output and SEG output become VSS level.
This control does not affect to SEG terminals that have been set for DC output.
At initial reset, this register is set to "0".

LOFF: LCD display control (C1H•D1)

Controls the LCD display

When "1" is written: Display all OFF
When "0" is written: Display ON
Reading: Valid

When "1" is written to LOFF, all LCD dots will fade out; writing "0" will set it back to normal.
All fading out of LCD at LOFF = "1" is due to light out signals and does not affect the content of the segment data memory.
Flashing on the entire LCD panel is performed by this function.
At initial reset, this register is set to "0".

STCD: LCD drive switch (C0H•D2)

Switches the LCD driving method.

When "1" is written: Static drive
When "0" is written: Dynamic drive
Reading: Valid

By writing "1" to STCD, static drive is selected, and dynamic drive is selected when "0" is written.
At initial reset, this register is set to "0".

LDTY1, LDTY0: LCD drive duty selection (C0H•D1, D0)
Sets the LCD drive duty as shown in Table 4.7.7.2.

Table 4.7.7.2 LCD drive duty setting

LDTY1	LDTY0	Duty	Terminals used in common	Maximum number of segments	Frame frequency *
0	0	1/2	COM0, COM1	68 (34 × 2)	f_{OSC1}/1,024 (32 Hz)
0	1	1/3	COM0–COM2	102 (34 × 3)	f_{OSC1}/768 (42.7 Hz)
1	X	1/4	COM0–COM3	136 (34 × 4)	f_{OSC1}/1,024 (32 Hz)

* In case of f_{OSC1} = 32.768 kHz

At initial reset, these registers are set to "0".

LDMS: LCD display memory area selection (C0H•D3)
Selects the display memory area.

When "1" is written: Page 0 (R / W)
When "0" is written: Page 4 (W)
Reading: Valid

By writing "1" to LDMS, page 0 is selected and addresses 050H–07FH become the display memory. Since a RAM has been allocated in this area, it can be used as the display memory for reading / writing.
When LDMS is set to "0", page 4 (450H–47FH) becomes the display memory. This area is write only.
At initial reset, this register is set to "0".

Display memory (50H–7FH)
The LCD segments are lit or turned off depending on this data.

When "1" is written: Lit
When "0" is written: Not lit
Reading: Invalid

By writing data into the display memory allocated to the LCD segment (on the panel), the segment can be lit or put out.
At initial reset, the contents of the display memory are undefined.

4.7.8 Programming notes

(1) The contents of the display memory are undefined until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) When page 4 is selected for the display memory area, since the display memory area is write-only, display data cannot be rewritten by arithmetic operations (such as AND, OR, ADD, SUB).

(3) 100 msec or more time is necessary for stabilizing the LCD drive voltages V_{C1}, V_{C2} and V_{C3} after setting the LCD power control register LPWR to "1". Be careful of the segment-on right after the power is turned on.

4.8 Clock Timer

4.8.1 Configuration of clock timer

The S1C621C0 has a built-in clock timer with OSC1 divided clock (256 Hz) as clock source. The clock timer is configured of a 8-bit binary counter and the timer data (128–16 Hz and 8–1 Hz) can be read out by the software.
Figure 4.8.1.1 is the block diagram for the clock timer.

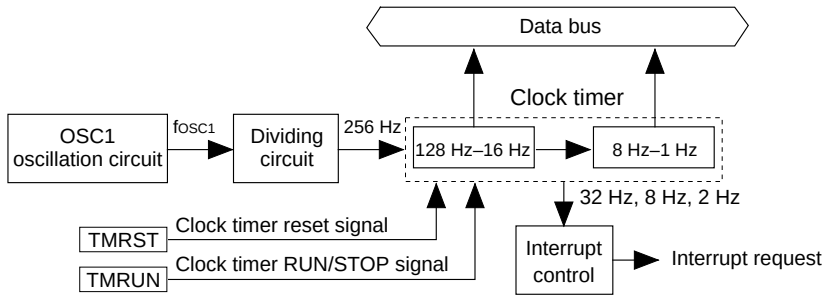


Fig. 4.8.1.1 Block diagram for the clock timer

Ordinarily, this clock timer is used for all types of timing functions such as clocks.

4.8.2 Data reading and hold function

The 8 bits timer data are allocated to the address C9H and CAH.

C9H	D0: TM0 (128 Hz)	D1: TM1 (64 Hz)	D2: TM2 (32 Hz)	D3: TM3 (16 Hz)
CAH	D0: TM4 (8 Hz)	D1: TM5 (4 Hz)	D2: TM6 (2 Hz)	D3: TM7 (1 Hz)

Since the clock timer data has been allocated to two addresses, a carry is generated from the low-order data within the count (TM0–TM3: 128–16 Hz) to the high-order data (TM4–TM7: 8–1 Hz). When this carry is generated between the reading of the low-order data and the high-order data, a content combining the two does not become the correct value (the low-order data is read as 0FH and the high-order data becomes the value that is counted up 1 from that point).
The high-order data hold function in the S1C621C0 is designed to operate to avoid this. This function temporarily stops the counting up of the high-order data (by carry from the low-order data) at the point where the low-order data has been read and consequently the time during which the high-order data is held is the shorter of the two indicated here following.

1. Period until it reads the high-order data.
2. 0.48–1.5 msec (varies due to the timing of the reading)

Note: When the high-order data has previously been read, since the low-order data is not held, you should be sure to first read from the low-order data.

4.8.3 Interrupt function

The clock timer can cause interrupts at the falling edge of 32 Hz, 8 Hz and 2 Hz signals. Software can set whether to mask any of these frequencies.
Figure 4.8.3.1 is the timing chart of the clock timer.

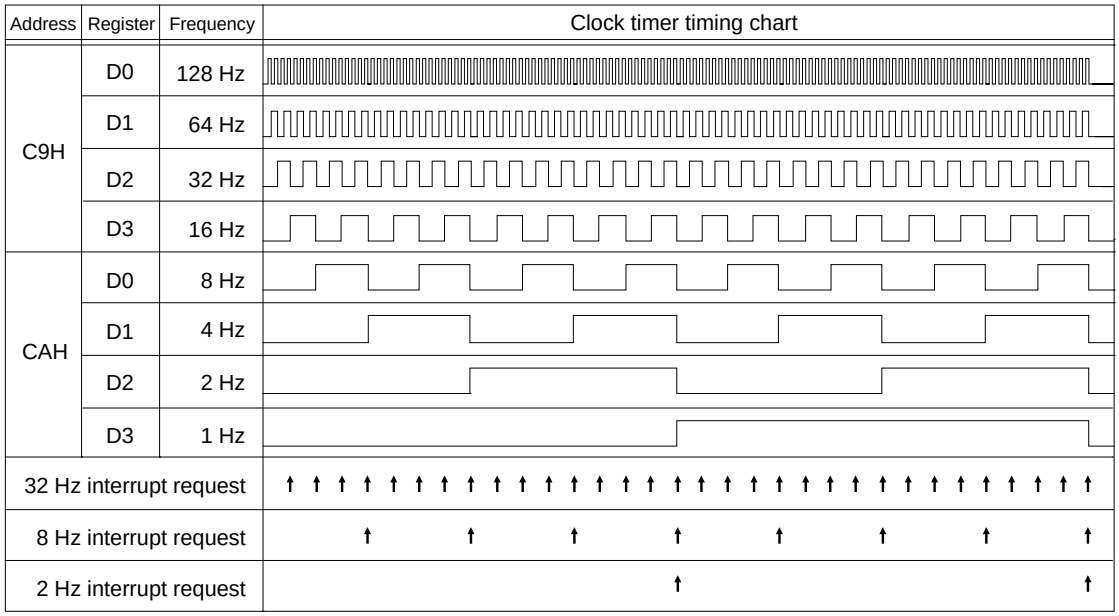


Fig. 4.8.3.1 Timing chart of clock timer

As shown in Figure 4.8.3.1, interrupt is generated at the falling edge of the frequencies (32 Hz, 8 Hz, 2 Hz). At this time, the corresponding interrupt factor flag (IT0, IT1, IT2) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT0, EIT1, EIT2). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

4.8.4 Control of clock timer

Table 4.8.4.1 shows the clock timer control bits and their addresses.

Table 4.8.4.1 Control bits of clock timer

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C8H	0	0	TMRUN	TMRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W	W	TMRUN	0	Run	Stop	Clock timer Run/Stop
					TMRST *5	Reset	Reset	–	Clock timer reset
C9H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
CAH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
F4H	0	EIT2	EIT1	EIT0	0 *5	– *2			Unused
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R	R/W			EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FCH	0	IT2	IT1	IT0	0 *5	– *2			Unused
					IT2 *4	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R				IT1 *4	0	Yes	No	Interrupt factor flag (Clock timer 8 Hz)
					IT0 *4	0	Yes	No	Interrupt factor flag (Clock timer 32 Hz)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

TM0–TM7: Timer data (C9H, CAH)

The 128 Hz–1 Hz timer data of the clock timer can be read out with these registers. These eight bits are read only, and writing operations are invalid.
By reading the low-order data (C9H), the high-order data (CAH) is held while the shorter of the two indicated here following.

1. Period until it reads the high-order data.
2. 0.48–1.5 msec (varies due to the timing of the reading)

At initial reset, the timer data is initialized to "00H".

TMRST: Clock timer reset (C8H•D0)

This bit resets the clock timer.

When "1" is written:	Clock timer reset
When "0" is written:	No operation
Reading:	Always "0"

The clock timer is reset by writing "1" to TMRST. When the clock timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained. No operation results when "0" is written to TMRST.
This bit is write-only, and so is always "0" at reading.

TMRUN: Clock timer RUN/STOP (C8H•D1)

This bit controls RUN / STOP of the clock timer.

When "1" is written:	RUN
When "0" is written:	STOP
Reading:	Valid

The clock timer enters the RUN status when "1" is written to TMRUN, and the STOP status when "0" is written.
In the STOP status, the timer data is maintained until the next RUN status or resets timer. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
At initial reset, this register is set to "0".

EIT0, EIT1, EIT2: Interrupt mask registers (F4H•D0, D1, D2)

These registers are used to select whether to mask the clock timer interrupt.

When "1" is written:	Enabled
When "0" is written:	Masked
Reading:	Valid

The interrupt mask registers (EIT0, EIT1, EIT2) are used to select whether to mask the interrupt to the separate frequencies (32 Hz, 8 Hz, 2 Hz).
At initial reset, these registers are all set to "0".

IT0, IT1, IT2: Interrupt factor flags (FCH•D0, D1, D2)

These flags indicate the status of the clock timer interrupt.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

The interrupt factor flags (IT0, IT1, IT2) correspond to the clock timer interrupts of the respective frequencies (32 Hz, 8 Hz, 2 Hz). The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.
These flags can be reset through being read out by the software.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.
At initial reset, these flags are set to "0".

4.8.5 Programming notes

(1) Be sure to data reading in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag reading (reset the flag) as necessary at reset.

(3) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

4.9 Remote Controller (REM)

4.9.1 Configuration of remote controller

The S1C621C0 has a remote controller (REM circuit) built-in. It can easily adapt to various remote controllers by connecting an infrared remote LED and a transistor as shown in Figure 4.9.1.1.

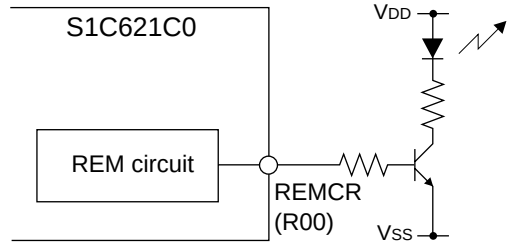


Fig. 4.9.1.1 Remote LED control circuit

Figure 4.9.1.2 shows the configuration of the REM circuit.

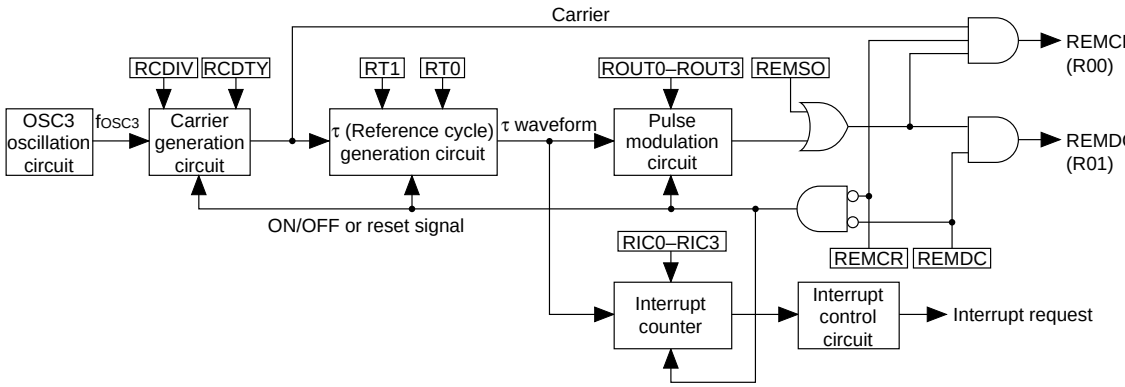


Fig. 4.9.1.2 Configuration of REM circuit

The generally used infrared remote controllers employ a method that generates transmission waveforms in pulse modulation as shown in Figure 4.9.1.3 and transmits the signal.
First the transmission code is modulated in a pulse phase modulation (PPM) method to generate the modulation signal, and the carrier that has constant frequency is amplitude-modulated (AM) using the modulation signal. As a result, transmission waveforms are generated. Transmission is done by driving the infrared LED using the transmission waveform.

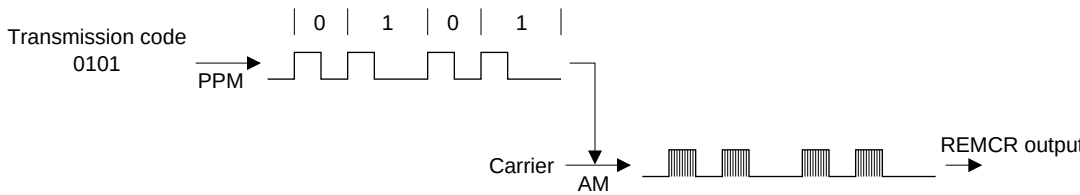


Fig. 4.9.1.3 Remote transmission method

In this remote controller, the carrier generated from the carrier generation circuit is controlled to turn the output ON and OFF and the transmission waveform is generated. This transmission waveform can be output from the REMCR (R00) terminal. Furthermore, the DC signal (above mentioned PPM modulation signal) that decides the ON / OFF timing for the carrier can be output from the REMDC (R01) terminal.
The carrier frequency and duty ratio can be selected by the software from among 4 types. (details are explained later)

This remote controller supports the following two modes for controlling the modulation signal (carrier ON / OFF).

- Soft-timer mode (Software timer control mode)
- Hard-timer mode (Hardware timer control mode)

In the soft-timer mode, the carrier ON / OFF timing and the time are controlled by the software. The optional ON / OFF time can be set within the range that is controlled by the software.
In the hard-timer mode, the carrier ON / OFF timing and the time are controlled by the pulse modulation circuit based on the reference cycle (τ) that is generated by the τ (reference cycle) generation circuit dividing the carrier. For the reference cycle (τ), the carrier dividing ratio can be selected by the software from 4 types. The carrier ON time can be selected by the software from 16 types, 0 to 15 times as long as the reference cycle (τ). The ON / OFF time is limited to some extent in comparison with the soft-timer mode, but the software's share is decreased because the interrupt can be used.
Features of the soft-timer mode and hard-timer mode are shown in Table 4.9.1.1.

Table 4.9.1.1 Features of soft-timer mode and hard-timer mode

Item	Soft-timer mode	Hard-timer mode
Processing of other routines during REM output	Difficult	Possible
Reference cycle (τ) sway during REM transmission	Source oscillation sway and errors caused by instruction cycles	Source oscillation sway only
Setting of REM output width	Variable to any width	Fixed to widths over ten
Relation between REM reference cycle and modulation frequency cycle	Variable	Fixed to widths over ten
Carrier waveform	Duty slightly disturbed before and after ON time	Stabilized at setting

4.9.2 Remote controller ON/OFF and output control

The remote controller has two output terminals: the REMCR terminal that outputs the pulse-modulated transmission waveform and the REMDC terminal that outputs the DC signal (PPM modulation signal) for controlling the carrier ON / OFF. (The following sections explain these outputs as REMCR output and REMDC output.) The REMCR and REMDC terminals are shared with the R00 and R01 output port terminals, respectively. The output circuit is configured as shown in Figure 4.9.2.1. When using the remote control outputs, fix the R00 and R01 registers at "0" and do not change them. (If the REMDC output is not used, the R01 register and terminal can be used as an output port.)
At initial reset and while remote output stops, the REMCR and REMDC terminals is set to low level (V_{SS}).

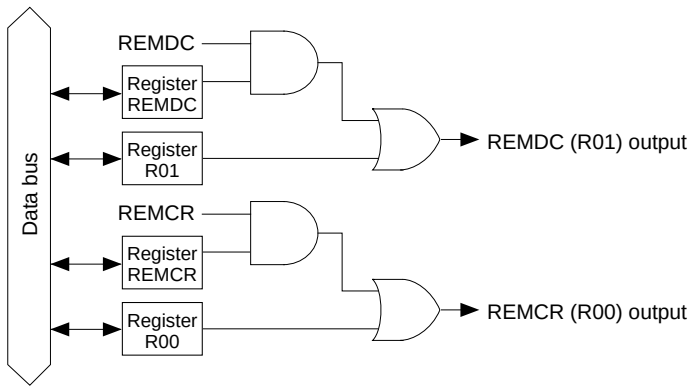


Fig. 4.9.2.1 Configuration of REMCR/R00 and REMDC/R01 output circuits

As shown in Figure 4.9.2.1, the REMCR output is enabled and shifts into outputable status by writing "1" to the REMCR register (E0H • D0). The REMDC output is enabled by writing "1" to the REMDC register (E0H • D1).

In addition, the REMCR and REMDC registers are designed to control the REM circuit ON / OFF. When "1" is written to either one or both registers, the REM circuit goes ON and the signal output corresponding to the register is started. When writing is done so that both registers are set to "0", the REM circuit goes OFF and the REMCR and REMDC terminals go to low level (V_{SS}). (when the R00 and R01 registers are fixed at "0".)

When the REMDC output is not used, control the REM circuit ON / OFF using the REMCR register only and fix the REMDC register at "0".
The timings of the REM circuit control such as the ON / OFF timing are explained in the following section.

Note: Except when outputting the remote control waveform, both REMCR and REMDC registers should be fixed at "0" to prevent outputting unnecessary waveforms and to reduce current consumption.

4.9.3 Carrier

The carrier is generated by the carrier generation circuit using the OSC3 clock as the source clock. The carrier cycle and duty ratio selections and the carrier generation circuit ON / OFF control can be done by the software.
The control for the carrier is same procedure for both the soft-timer mode and the hard-timer mode. Perform the carrier settings before starting the transmission in each mode.

The carrier cycle (selection as the dividing ratio of the OSC3 clock) and the duty ratio can be set using the RCDIV register (E1H • D3) and RCDTY register (E1H • D2) as shown in Table 4.9.3.1.

Table 4.9.3.1 Carrier dividing ratio and duty ratio

RCDIV	RCDTY	Carrier dividing ratio	Carrier duty ratio
0	0	f_{OSC3} / 8	1/4
0	1	f_{OSC3} / 8	3/8
1	0	f_{OSC3} / 12	1/3
1	1	f_{OSC3} / 12	1/4

f_{OSC3}: OSC3 oscillation frequency

Carrier settings can be done even when the OSC3 oscillation circuit is in OFF status. Furthermore, when these are set once, the set contents are maintained until an initial reset is performed.

Note: The setting of the RCDIV register and the RCDTY register should be done when the REM circuit is OFF (REMCR = REMDC = "0") before starting remote transmission. If changing the contents when the REM circuit is ON, it may cause a malfunction.

The carrier generation circuit is switched to ON / OFF by the above mentioned REMCR and REMDC registers. By writing "1" to either one or both registers, the carrier generation circuit goes ON and generates the carrier. When both registers are set to "0" by writing, the carrier generation circuit goes OFF and the carrier generation stops.
The OSC3 clock is divided to generate the carrier. Therefore, the OSC3 oscillation circuit must be ON before starting remote output. Remote output should be done when the OSC3 oscillation has stabilized.

Note: It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when starting a remote output, secure 5 msec or more waiting time for oscillation stabilization after turning the OSC3 oscillation ON.

Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the waiting time.

Figure 4.9.3.1 shows the carrier waveform.

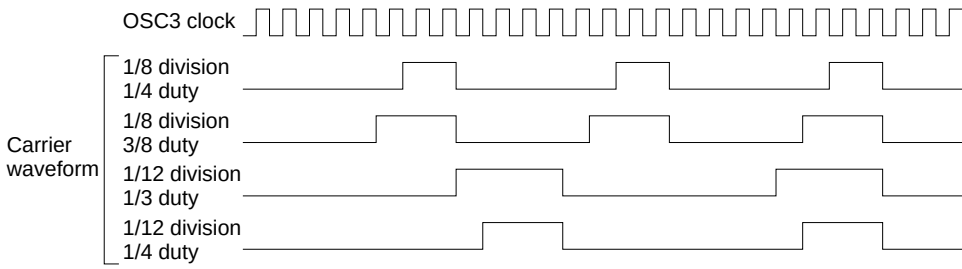


Fig. 4.9.3.1 Carrier waveform.

The carrier generation circuit starts carrier output internally in synchronization with the falling edge of the OSC3 clock immediately after writing "1" to the REMCR register or the REMDC register.
When both REMCR and REMDC registers is set to "0", the carrier output stops without synchronization with the OSC3 clock.

4.9.4 Soft-timer mode

In the soft-timer mode, software controls the ON / OFF time and timing of the carrier output. This mode does not use the τ (reference cycle) generation circuit, pulse modulation circuit and interrupt control circuit that are used in the hard-timer mode, and operates with the configuration as shown in Figure 4.9.4.1.

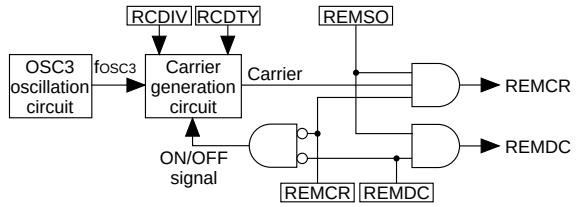


Fig. 4.9.4.1 REM circuit configuration in soft-timer mode

The ON / OFF control of the carrier output is done using the REMSO register (E0H • D2). By writing "1" to the REMSO register, the carrier is output to the REMCR terminal and when "0" is written, the REMCR terminal goes low level (VSS). However, the carrier must be generated by writing "1" to the REMCR register before writing "1" to the REMSO register.
Moreover, when the REMDC register has been set to "1" (the R01 register is fixed at "0"), the content of the REMSO register is output from the REMDC terminal as the REMDC signal.
Figure 4.9.4.2 shows the timing chart in the soft-timer mode.

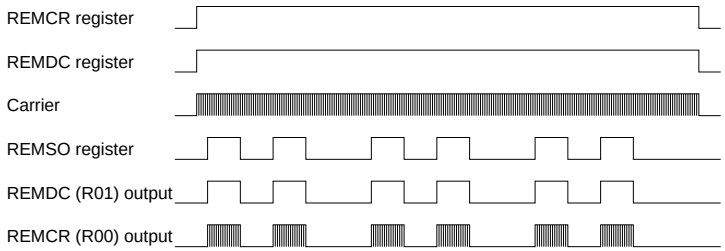


Fig. 4.9.4.2 Timing chart (soft-timer mode)

Note: • Writing to the REMSO register without synchronization with the carrier generation circuit, therefore when turning the carrier output ON/OFF using the REMSO register, the duty ratio of the carrier will not be the value set by the software. (Figure 4.9.4.3)

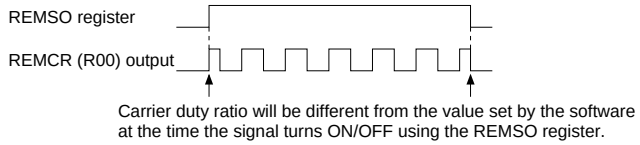


Fig. 4.9.4.3 Carrier ON/OFF by REMSO register

• Be sure to control the carrier output using the REMSO register. Do not control the carrier output using the REMCR register by setting the REMSO register to "1". Similarly, in the case of REMDC output, do not control the output using the REMDC register.

4.9.5 Hard-timer mode and REM interrupt

In the soft-timer mode, the CPU is occupied for the remote output processing so that it has no flexibility for execution of other routines. To alleviate this problem, the S1C621C0 supports the hard-timer mode explained below.

In the hard-timer mode, the carrier ON / OFF, that is controlled using the REMSO register in the soft-timer mode, is done in the hardware by using the τ (reference cycle) generation circuit and the pulse modulation circuit. τ (reference cycle) is generated from the carrier by dividing, and is used for reference of the carrier ON / OFF time in the hard-timer mode. The dividing ratio of τ (reference cycle) is selected from 4 types by the software. The carrier ON / OFF time can be set for each transmission data bit by the software using τ (reference cycle) as reference. Furthermore, the interrupt function is provided so that the setting can be done without synchronizing with the timing of the carrier output.
The interrupt timing can also be set by the software using τ (reference cycle) as the reference same as the ON / OFF time.

The circuit in the hard-timer mode is configured as shown in Figure 4.9.1.2, and all the REM circuit is used. However, the REMSO register that is used to control the carrier output in the soft-timer mode should be fixed at "0". If "1" is written to the REMSO register, REMCR output and / or REMDC output are forcibly done regardless of the control of the hard-timer mode.

(1) τ (reference cycle)

τ (reference cycle) is used as reference for the carrier output ON time and interrupt timing specified by the software, and is generated by the τ (reference cycle) generation circuit by dividing carrier. This dividing ratio can be selected using the RT1 and RT0 registers (E1H • D1, D0) from 4 types as shown in Table 4.9.5.1.

Table 4.9.5.1 τ (reference cycle) setting

RT1	RT0	τ dividing ratio
0	0	fcarrier / 12
0	1	fcarrier / 16
1	0	fcarrier / 20
1	1	fcarrier / 32

* fcarrier indicates carrier frequency. It is selected with the RCDIV register (E1H•D3).

The actual time of τ (reference cycle) can be found using the following expression according to the OSC3 oscillation frequency, carrier cycle selection and the above selection.

τ (reference cycle) [sec] = 1 / (f_{OSC3} × DIV1 × DIV2)

f_{OSC3}: OSC3 oscillation frequency
DIV1: Content of carrier dividing ratio set with the RCDIV register (1 / 8 or 1 / 12)
DIV2: Content of τ dividing ratio set with the RT1 and RT0 registers (1 / 12, 1 / 16, 1 / 20 or 1 / 32)

Table 4.9.5.2 shows the examples of τ (reference cycle) according to the OSC3 oscillation frequency.

Table 4.9.5.2 τ (reference cycle) examples

Register settings			OSC3 oscillation frequency	
RCDIV	RT1	RT0	455 kHz	1 MHz
0	0	0	0.211 msec (4739.6 Hz)	0.096 msec (10416.7 Hz)
0	0	1	0.281 msec (3554.7 Hz)	0.128 msec (7812.5 Hz)
0	1	0	0.352 msec (2843.8 Hz)	0.160 msec (6250.0 Hz)
0	1	1	0.563 msec (1777.3 Hz)	0.256 msec (3906.2 Hz)
1	0	0	0.316 msec (3159.7 Hz)	0.144 msec (6944.4 Hz)
1	0	1	0.422 msec (2369.8 Hz)	0.192 msec (5208.3 Hz)
1	1	0	0.527 msec (1895.8 Hz)	0.240 msec (4166.7 Hz)
1	1	1	0.844 msec (1184.9 Hz)	0.384 msec (2604.2 Hz)

The carrier output ON time can be set to 16 types (0τ to 15τ) based on the τ (reference cycle) set, so set the τ (reference cycle) after due consideration.

Figure 4.9.5.1 shows the τ waveform when fcarrier / 12 has been selected.
τ waveform is kept on outputting from the τ (reference cycle) generation circuit according to the set dividing ratio while the REMCR register or REMDC register is "1".

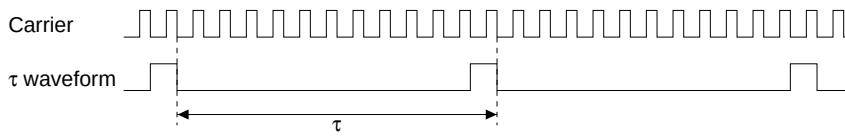


Fig. 4.9.5.1 τ waveform (when fcarrier /12 is selected)

It is possible to set τ (reference cycle) even if the OSC3 oscillation circuit is in OFF status. Furthermore, when it is set once, the set contents are maintained until an initial reset is performed.

Note: The setting of the RT1 and RT0 registers should be done when the REM circuit is OFF (REMCR = REMDC = "0") before starting remote transmission. Changing the contents when the REM circuit is ON may cause a malfunction.

(2) Setting of carrier output width

In the soft-timer mode, the carrier output width (carrier output ON time) is controlled by writing to the REMSO register, but in the hard-timer mode, it can be specified with values 0 to 15, which mean the number of τ cycles described above, in each transmission data bit. Since the carrier output ON / OFF is controlled by the hardware in synchronizing with τ waveform, it is unnecessary to watch the ON time and to specify the OFF timing by the software.
The carrier output width can be selected by writing data to the ROUT3–ROUT0 register (E3H) from among 16 types as shown in Table 4.9.5.3.

Table 4.9.5.3 Setting of carrier output width

ROUT3	ROUT2	ROUT1	ROUT0	Carrier output width
0	0	0	0	0τ
0	0	0	1	1τ
0	0	1	0	2τ
0	0	1	1	3τ
0	1	0	0	4τ
0	1	0	1	5τ
0	1	1	0	6τ
0	1	1	1	7τ
1	0	0	0	8τ
1	0	0	1	9τ
1	0	1	0	10τ
1	0	1	1	11τ
1	1	0	0	12τ
1	1	0	1	13τ
1	1	1	0	14τ
1	1	1	1	15τ

The carrier is output in synchronizing with the falling edge of the τ waveform after writing data to ROUT3–ROUT0 register. Data written to the ROUT3–ROUT0 register is maintained while the REM circuit is ON until the next data is written. The carrier output starts using the write signal for this register and the carrier output will be ON from the falling edge of the τ waveform immediately after that until the period set in the register has passed. In other words, the register data is valid only one time after writing. Consequently, data must be written (possible with a logical arithmetic instruction) every time even when outputting the same data successively.
The ROUT3–ROUT0 register is set to "0H" at initial reset and when both REMCR and REMDC registers are set to "0". Consequently, after turning the REM circuit ON ("1" is written to the REMCR or REMDC register), REMCR / REMDC output becomes low level (V_{SS}) until a value other than "0H" is written to the ROUT3–ROUT0 register.
Figure 4.9.5.2 shows the timing of data writing to the ROUT3–ROUT0 register and the carrier output.

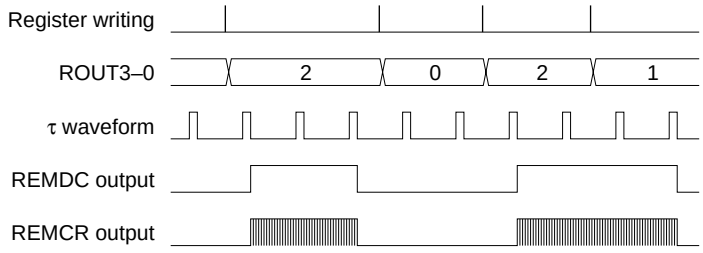


Fig. 4.9.5.2 Carrier output timing

Note: To prevent malfunction, do not write data to the ROUT3–ROUT0 register while τ waveform is high. Furthermore, the next transmission data writing should be done after the current carrier output is completed unless done intentionally. If this register is written during carrier output, it stops output at the point of the falling edge of the τ waveform after the writing and starts new carrier output.

Those timings to be processed using interrupt are explained in the following section.

(3) Remote controller (REM) interrupt

The carrier output ON time for one transmission data bit is controlled by writing data to the above mentioned ROUT3–ROUT0 register. The OFF time is from when the output is turned OFF to when the next carrier output starts by writing to the same register. Since the carrier output is turned ON at the falling edge of the τ waveform after writing data, the next data must be written during the last τ cycle in the carrier OFF period of the current transmission data. To decide its timing, an interrupt is used in the hard-timer mode.
By using the interrupt, the CPU is released from the processing such as a timing watch, and can execute other processing.

The timing to generate interrupt can be set by the software using τ cycle as reference the same as the carrier output width. Set the interrupt timing so that it will be generated after 1 to 16 τ cycles, and perform the next carrier output using the interrupt.
The interrupt timing can be selected by writing data to the RIC3–RIC0 register (E2H) from among 16 types as shown in Table 4.9.5.4.

Table 4.9.5.4 Setting of interrupt timing

RIC3	RIC2	RIC1	RIC0	Interrupt τ cycle
0	0	0	0	1τ
0	0	0	1	2τ
0	0	1	0	3τ
0	0	1	1	4τ
0	1	0	0	5τ
0	1	0	1	6τ
0	1	1	0	7τ
0	1	1	1	8τ
1	0	0	0	9τ
1	0	0	1	10τ
1	0	1	0	11τ
1	0	1	1	12τ
1	1	0	0	13τ
1	1	0	1	14τ
1	1	1	0	15τ
1	1	1	1	16τ

* Interrupt cycle nτ: (n=1 to 16) The interrupt is generated at the falling edge of the selected τ pulse after writing the RIC register.

When the REM circuit has been turned ON (REMCR / REMDC = "1"), the REM interrupt control circuit starts counting for τ waveform at the point that data is written to the RIC3–RIC0 register. The τ waveform is counted at every falling edge. When the count becomes the number set in the RIC3–RIC0 register, the interrupt factor flag IREM (F8H • D0) is set to "1" and an interrupt occurs in synchronization with that falling edge.
Set the next carrier output width and the interrupt timing using this interrupt.
The REM interrupt can be masked through the interrupt mask register EIREM (F1H • D0). However, regardless of the setting of the interrupt mask register, the interrupt factor flag IREM is set to "1" when the counting of the interrupt τ cycles are completed.
The interrupt factor flag is reset to "0" by the reading.

Data written to the RIC3–RIC0 register is maintained while the REM circuit is ON until the next data is written. However, the counting of τ waveform starts using the write signal for the RIC3–RIC0 register the same as the ROUT3–ROUT0 register, so this register data is valid only one time after writing. Consequently, data must be written (possible with a logical arithmetic instruction) every time even when generating the next interrupt in the same cycle.
The RIC3–RIC0 register is set to "0FH" (16τ) at initial reset and when both REMCR and REMDC registers are set to "0". However, the counting of τ cycles is not performed until the RIC3–RIC0 register is written after that.
Figure 4.9.5.3 shows the timing of data writing to the RIC3–RIC0 register and the interrupt generation.

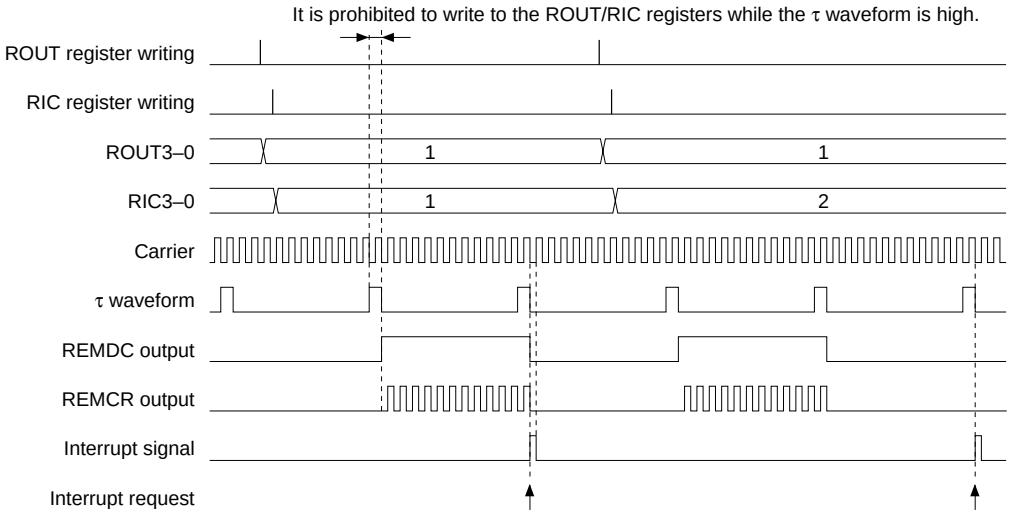


Fig. 4.9.5.3 Interrupt timing

Note: • To prevent malfunction, do not write data to the RIC3–RIC0 register while τ waveform is high. If this register is re-written before generating the interrupt corresponding the previous written data, the interrupt counter is renewed and the previous set interrupt becomes invalid.

• Reading of the interrupt factor flag is available at EI, but be careful in the following cases. If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

4.9.6 Control of remote controller

Table 4.9.6.1 lists the remote controller control bits and their addresses.

Table 4.9.6.1 Control bits of remote controller

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E0H	0	REMSO	REMDC	REMCR	0 *5	– *2			Unused
					REMSO	0	On	Off	REM soft-timer output control
	R	R/W			REMDC	0	On	Off	REM DC output control
					REMCR	0	On	Off	REM carrier output control
E1H	RCDIV	RCDTY	RT1	RT0	RCDIV	0	fosc3/12	fosc3/8	REM carrier cycle selection
					RCDTY	0			REM carrier duty selection *6
	R/W				RT1	0			REM τ cycle selection
					RT0	0			0: 1/12, 1: 1/16, 2:1/20, 3: 1/32 (x fcarrier)
E2H	RIC3	RIC2	RIC1	RIC0	RIC3	1			REM interrupt τ cycle selection
					RIC2	1			0H = 1τ ... FH = 16τ
	R/W				RIC1	1			
					RIC0	1			
E3H	ROUT3	ROUT2	ROUT1	ROUT0	ROUT3	0			REM carrier output width selection
					ROUT2	0			0H = 0τ ... FH = 15τ
	R/W				ROUT1	0			
					ROUT0	0			
F0H	0	0	0	EIREM	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIREM	0	Enable	Mask	Interrupt mask register (Remote controller)
F8H	0	0	0	IREM	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IREM *4	0	Yes	No	Interrupt factor flag (Remote controller)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

REMCR: REMCR output control (E0H•D0)

Controls the REMCR (carrier) output.

When "1" is written: REMCR output is enabled
When "0" is written: REMCR output is disabled
Reading: Valid

REMCR is the register to turn the carrier generation circuit ON / OFF and to enable / disable the REMCR (carrier) output.
When "1" is written to REMCR, the carrier generation circuit turns ON and the REMCR output from the REMCR (R00) terminal is enabled. The REMCR output timing is controlled according to the soft-timer mode or the hard-timer mode.
When performing the REMCR output, the data register of the R00 output port should be fixed at "0".
When "0" is written to REMCR, it disables the REMCR output. It also turns the carrier generation circuit OFF if REMDC has been set to "0".
At initial reset, this register is set to "0".

REMDC: REMDC output control (E0H•D1)

Controls the REMDC (DC) output.

When "1" is written: REMDC output is enabled
When "0" is written: REMDC output is disabled
Reading: Valid

REMDC is the register to turn the carrier generation circuit ON / OFF and to enable / disable the REMDC (DC signal before pulse modulation) output.
When "1" is written to REMDC, the carrier generation circuit turns ON and the REMDC output from the REMDC (R01) terminal is enabled. The REMDC output timing is controlled according to the soft-timer mode or the hard-timer mode.
When performing the REMDC output, the data register of the R01 output port should be fixed at "0".
When "0" is written to REMDC, it disables the REMDC output. It also turns the carrier generation circuit OFF if REMCR has been set to "0".
At initial reset, this register is set to "0".

REMSO: Soft-timer output control (E0H•D2)

Controls the carrier output in the soft-timer mode.

When "1" is written: Carrier output ON
When "0" is written: Carrier output OFF
Reading: Valid

REMSO is the register for the soft-timer mode to control the ON / OFF of the REMCR and REMDC outputs. By writing "1" to REMSO when REMCR has been set to "1", Carrier is output from the REMCR (R00) terminal. When "0" is written, the REMCR (R00) terminal goes to low level (V_{SS}).
When REMDC has been set to "1", the content of REMSO is output from the REMDC (R01) terminal as a DC signal. The REMDC output becomes high level (V_{DD}) when REMSO is "1", and becomes low level (V_{SS}) when it is "0".
At initial reset, this register is set to "0".

Note: REMSO is for the exclusive use of the soft-timer mode. When controlling with the hard-timer mode, REMSO should be fixed at "0".

RCDIV: Carrier cycle selection (E1H•D3)

Selects the carrier cycle.

When "1" is written: f_{OSC3} / 12
When "0" is written: f_{OSC3} / 8
Reading: Valid

RCDIV is the register to select the carrier cycle in the dividing ratio of the OSC3 oscillation frequency (f_{OSC3}).
When "1" is written to RCDIV, the carrier frequency is set to f_{OSC3} / 12. When "0" is written, it is set to f_{OSC3} / 8. This setting must be done when the remote controller is OFF (REMCR = REMDC = "0") status.
At initial reset, this register is set to "0".

RCDTY: Carrier duty ratio selection (E1H•D2)

Selects the duty ratio of the carrier.
Duty ratio set by RCDTY varies according to the carrier cycle set by RCDIV as the follows:

Table 4.9.6.2 Selection of carrier duty ratio

RCDIV	RCDTY	Carrier dividing ratio	Carrier duty ratio
0	0	fOSC3 / 8	1/4
0	1	fOSC3 / 8	3/8
1	0	fOSC3 / 12	1/3
1	1	fOSC3 / 12	1/4

fOSC3: OSC3 oscillation frequency

This setting must be done when the remote controller is OFF (REMCR = REMDC = "0") status.
At initial reset, this register is set to "0".

RT1, RT0: τ cycle selection (E1H•D1, D0)

Selects the τ (reference cycle).
When controlling in the hard-timer mode, select the τ (reference cycle) that is used as a reference for the timing from the following table.

Table 4.9.6.3 τ (reference cycle) setting

RT1	RT0	τ dividing ratio
0	0	fcarrier / 12
0	1	fcarrier / 16
1	0	fcarrier / 20
1	1	fcarrier / 32

* fcarrier indicates carrier frequency. It is selected by RCDIV (E1H•D3).

This setting must be done when the remote controller is in OFF (REMCR = REMDC = "0") status.
At initial reset, these registers are set to "0".

ROUT3–ROUT0: Carrier output width selection (E3H)

When controlling in the hard-timer mode, select the carrier output width.

Table 4.9.6.4 Setting of carrier output width

ROUT3	ROUT2	ROUT1	ROUT0	Carrier output width
0	0	0	0	0τ
0	0	0	1	1τ
0	0	1	0	2τ
:	:	:	:	:
1	1	1	0	14τ
1	1	1	1	15τ

By writing data to this register when the REMCR output has been enabled (REMCR = "1"), the carrier for set τ cycles is output from the REMCR (R00) terminal in synchronization with the falling edge of the τ waveform immediately after that. If the REMDC output has been enabled, the REMDC output goes high level (VDD) at the same timing, and is maintained for the set output width.
The setting (writing) of carrier output width must be done at every bit of the transmission data.
At initial reset and when both REMCR and REMDC registers are set to "0", this register is set to "0H (0000B)".

Note: The ROUT3–ROUT0 register is for the exclusive use of the hard-timer mode. When controlling with the soft-timer mode, be sure not to write data to this register to prevent malfunction.

RIC3–RIC0: Interrupt τ cycle selection (E2H)

When controlling in the hard-timer mode, select the interrupt generation timing.

Table 4.9.6.5 Setting of interrupt timing

RIC3	RIC2	RIC1	RIC0	Interrupt τ cycle
0	0	0	0	1τ
0	0	0	1	2τ
0	0	1	0	3τ
:	:	:	:	:
1	1	1	0	15τ
1	1	1	1	16τ

By writing data to this register when the REM circuit has been ON (REMCR / REMDC = "1"), the counting of τ waveform is started by synchronizing with the falling edge of the τ waveform immediately after that. When the count becomes the number set in this register, an interrupt occurs. Set the next transmission data and interrupt timing using this interrupt.
The setting (writing) of interrupt τ cycle must be done at every bit of the transmission data.
At initial reset and when both REMCR and REMDC registers are set to "0", this register is set to "0FH (1111B)".

Note: The RIC3–RICO register is for the exclusive use of the hard-timer mode. When controlling with the soft-timer mode, be sure not to write data to this register to prevent malfunction.

EIREM: Interrupt mask register (F0H•D0)

This register is used to select whether to mask the remote controller interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

When "1" is written to EIREM, the remote controller interrupt is enabled. When "0" is written, it is masked.
At initial reset, this register is set to "0".

IREM: Interrupt factor flag (F8H•D0)

This is the interrupt factor flag of the remote controller.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

This flag is set to "1" when the interrupt τ cycle set with RIC3–RIC0 has passed (counting of the τ waveform has completed).
From the status of this flag, the software can decide the remote controller interrupt. Note, however, that even if the interrupt is masked, this flag will be set to "1" when the counting of the interrupt τ cycle is completed.
This flag is reset when read out by the software.
Reading of the interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.
At initial reset, this flag is set to "0".

4.9.7 Programming notes

(1) When using the remote control outputs, fix the R00 and R01 registers at "0" and do not change them. (If the REMDC output is not used, the R01 register and terminal can be used as an output port.)

(2) Except when outputting the remote control waveform, both REMCR and REMDC registers should be fixed at "0" to prevent outputting unnecessary waveform and to reduce current consumption.

(3) When performing remote output, it is necessary that the OSC3 oscillation circuit has already been ON. Remote output should be started when the OSC3 oscillation is stabilized.
It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when starting a remote output, secure 5 msec or more waiting time for oscillation stabilization after turning the OSC3 oscillation ON.
Further, the oscillation stabilization time varies depending ON the external oscillator characteristics and conditions of use, so allow ample margin when setting the waiting time.

(4) The setting of the RCDIV register (carrier cycle), RCDTY register (carrier duty ratio) and RT1/RT0 registers (τ reference cycle) should be done when the REM circuit is OFF (REMCR = REMDC = "0") before starting remote transmission. Changing the contents when the REM circuit is ON may cause a malfunction.

(5) When performing remote output in the soft-timer mode, be sure to control the carrier output using the REMSO register. Do not control the carrier output using the REMCR register by setting the REMSO register to "1". Similarly, in the case of REMDC output, do not control the output using the REMDC register.

(6) REMSO is for the exclusive use of the soft-timer mode. When controlling with the hard-timer mode, REMSO should be fixed at "0".

(7) When performing remote output in the hard-timer mode, do not write data to the ROUT3–ROUT0 register while the τ waveform is high to prevent malfunction. Furthermore, next transmission data writing should be done after the current carrier output is completed unless done intentionally. If this register is written during carrier output, it stops output at that point of the falling edge of the τ waveform after the writing and starts new carrier output.
Furthermore, the ROUT3–ROUT0 register is for the exclusive use of the hard-timer mode. When controlling with the soft-timer mode, be sure not to write data to this register to prevent malfunction.

(8) When performing remote output in the hard-timer mode, do not write data to the RIC3–RIC0 register while τ waveform is high to prevent malfunction. If this register is re-written before generating the interrupt corresponding the previous written data, the interrupt counter is renewed and the previous set interrupt becomes invalid.
Furthermore, the RIC3–RIC0 register is for the exclusive use of the hard-timer mode. When controlling with the soft-timer mode, be sure not to write data to this register to prevent malfunction.

(9) The soft-timer mode and the hard-timer mode can not be used at the same time. To use them in combination, set both REMCR and REMDC registers to "0" to stop the REM circuit before switching the mode.

(10) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

4.10 R/F Converter

4.10.1 Configuration of R/F converter

The S1C621C0 has CR oscillation type R/F converter.
Two systems (two sensor connection terminals: SEN0, SEN1) of CR oscillation circuit are built into this R/F converter, so it is possible to compose two types of R/F conversion circuits by connecting different resistive sensors to each CR oscillation circuit.
Each of the R/F conversion circuits uses the same CR oscillation circuit and the same external reference resistance. The R/F conversion circuit to be used is selected by the software.
Resistance value (relative value to external reference resistance) of the resistive sensor that has been connected to the sensor input terminal is converted into frequency by the CR oscillation circuit and the number of clocks is counted in the built-in measurement counter. By reading the value of the measurement counter, it can obtain the data after digitally-converting the value detected by the sensor.
Various sensor circuits such as temperature measurement circuits using a thermistor can be easily realized using this R/F converter.
The configuration of the R/F converter is shown in Figure 4.10.1.1.

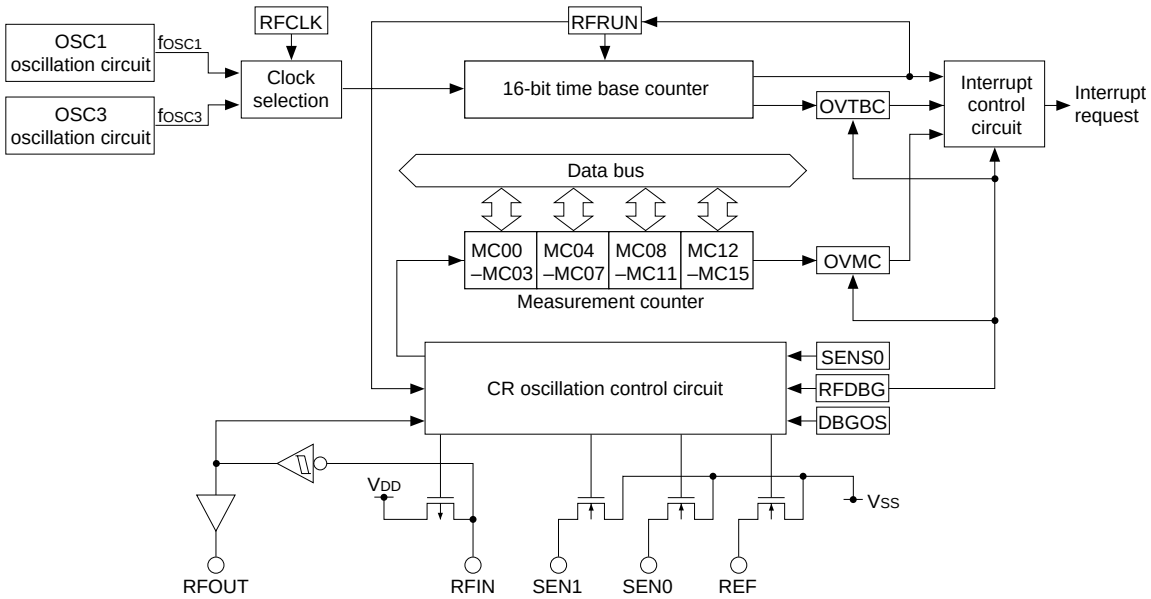


Fig. 4.10.1.1 Configuration of R/F converter

4.10.2 Connection terminals and CR oscillation circuit

The S1C621C0 has the connecting terminals for one reference resistance and two sensors so that two R/F converters can be configured.
Figure 4.10.2.1 shows the connection diagram of external elements.

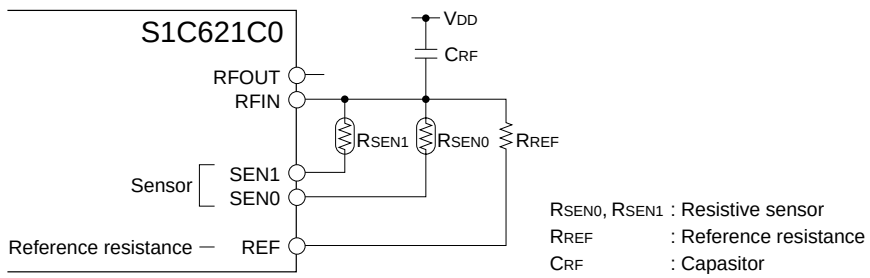


Fig. 4.10.2.1 R/F converter external connection diagram

The capacitor for the CR oscillation circuit is commonly used for the reference resistance and both sensors. The CR oscillation circuit is configured with the reference resistance, each of the sensors and this capacitor and can R/F-convert using the reference resistance and the sensor selected by the software.
The R/F converter performs CR oscillation using each of the two resistances (sensor and reference resistance) in the same period, and counts the CR oscillation clock. Difference in counted oscillation frequency can be evaluated in terms of the difference between the respective resistance values. Measurement results can be obtained from the changes in resistance values after correcting the difference according to the program. Consequently, a resistance that has a resistance value equivalent to the middle of the measurement range of the sensor to be used for measurement should be used as a reference resistance. An element that does not change due to temperature or other environmental conditions must be used as the reference resistance.

Sensor to be R/F-converted can be selected as below using the SENS0 register.

SENS0 register = "1" ... SEN1 is selected
SENS0 register = "0" ... SEN0 is selected

The following explains the operation of the CR oscillation circuit that is configured with the above connection.

The operation of the CR oscillation circuit is similar for both reference resistance and sensors, so the following explanation is in the case of the CR oscillation circuit with the sensor connected to the SEN0 terminal.
Figure 4.10.2.2 shows the CR oscillation circuit configured with the SEN0 terminal.

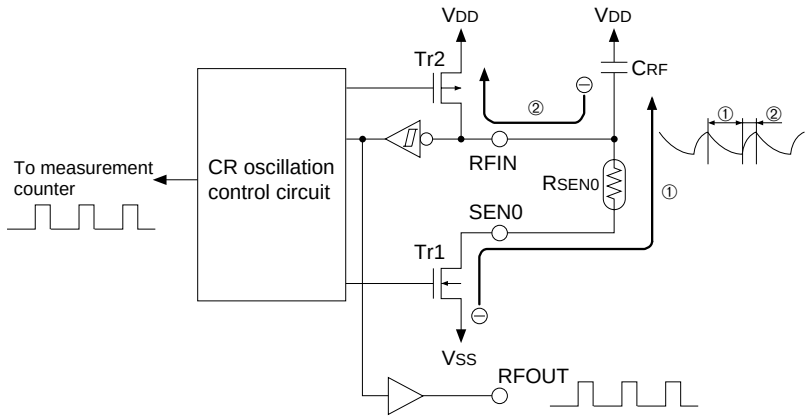


Fig. 4.10.2.2 CR oscillation circuit

The Tr1 turns on first, and the capacitor (C_{RF}) connected between the V_{DD} and RFIN terminals is charged through the sensor (R_{SEN0}). If the voltage level of the RFIN terminal decreases, the Tr1 turns off and the Tr2 turns on. As a result, the capacitor becomes discharged, and oscillation is performed according to CR time constant. The time constant changes as the sensor resistance value fluctuates, producing a difference from the oscillation frequency of the reference resistance.

The above example is in the case of a SEN0 terminal. Controlling whether the reference resistance or the sensor selected by the software to be CR-oscillated (controlling a transistor of terminal) is done by the CR oscillation circuit.

Oscillation waveforms are shaped by the schmitt trigger and transmitted to the measurement counter. The clock transmitted to the counter is also output from the RFOUT terminal. As a result, oscillation frequency can be identified by the oscilloscope. Since this monitor has no effect on oscillation frequency, it can be used to adjust CR oscillation frequency.
Oscillation waveforms and waveforms output from the RFOUT terminal are shown in Figure 4.10.2.3.

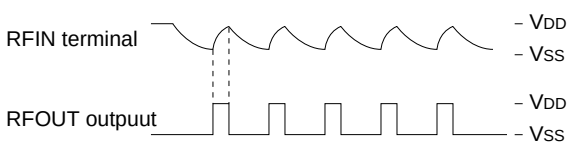


Fig. 4.10.2.3 Oscillation waveform

4.10.3 Operation of R/F conversion

(1) Counter

The R/F converter incorporates two types of counters. One is the measurement counter MCxx that counts the aforementioned oscillation clock, and the other is the time base counter that counts the internal clock for reference counting.

The measurement counter is used to count (count up) the CR oscillation clock by the reference resistance and sensor, and the results of R/F conversion can be obtained by reading this counter. The measurement counter is 16 bits (MC00–MC15) and can be read in 4-bit units.
This counter is designed so that it counts serially in order of the reference resistance and the sensor. Also it switches the CR oscillation from reference resistance to sensor at the point an overflow occurs (counter = 0000H) during counting of the reference resistance oscillation. Furthermore, both of the oscillation times of the reference resistance and sensor are designed to be the same by the time base counter described later. Therefore, by converting a proper initial value for counting of the oscillation of the reference resistance into a complement (value subtracted from 0000H) and setting it into the counter before starting to count, the number of counts for the sensor oscillation is obtained by reading this counter after the R/F conversion. In other words, the difference between the reference resistance and sensor oscillation frequencies can be found easily. For instance, if resistance values of the reference resistance and the sensor are equivalent, the same value as the initial value before converting into a complement will be obtained as the result.

The time base counter is a 16-bit up/down counter to equal both oscillation times for the reference resistance and the sensor. For the input clock, either OSC1 clock (Typ. 32.768 kHz) or OSC3 clock (Typ. 455 kHz) can be selected using the software. This selection can be done using the register RFCLK (D0H • D1). When "1" is set to the register, OSC3 clock is selected and when "0" is set, OSC1 clock is selected.
When R/F conversion is started, the time base counter starts counting-down from "0000H" at the same time the measurement counter starts counting for oscillation by reference resistance. After that, when the oscillation switches to the sensor side, this counter also switches to counting-up and counts up oppositely from the value that is counted during oscillation of the reference resistance. The counting-up continues until the counter value is "0000H". When the counter becomes "0000H", the counter stops and the sensor oscillation also stops. In other words, the oscillation times of reference resistance and sensor can be made the same.

(2) R/F conversion sequence

R/F conversion starts by writing "1" to the register RFRUN (D2H • D1).
Further the following settings must be done before starting the R/F conversion.

1. Sensor selection (SENS0)
2. Selecting the time base counter input clock (RFCLK)
3. Initial value setting to the measurement counter
4. Turning the OSC3 oscillation ON (OSCC) ...when the OSC3 clock is selected at 2.

Note: It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when starting a remote output, secure 5 msec or more waiting time for oscillation stabilization after turning the OSC3 oscillation ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the waiting time.

When R/F conversion is initiated by the RFRUN register, oscillation by the reference resistance begins first, and the measurement counter starts counting up from the initial value by the oscillation clock. The time base counter also starts counting down by the internal clock.
Timing in starting oscillation and starting counting are shown in Figure 4.10.3.1.
CR oscillation starts in synchronizing with the falling edge of the OSC1 or OSC3 clock (one of these that is selected as the time base counter input clock) immediately after writing "1" to the RFRUN register.
The measurement counter starts counting up at the falling edge of the first clock after CR oscillation is initiated.
The time base counter becomes enable at the falling edge of the first internal clock (OSC1 or OSC3). Then, it counts down by the falling edge of the internal clock.

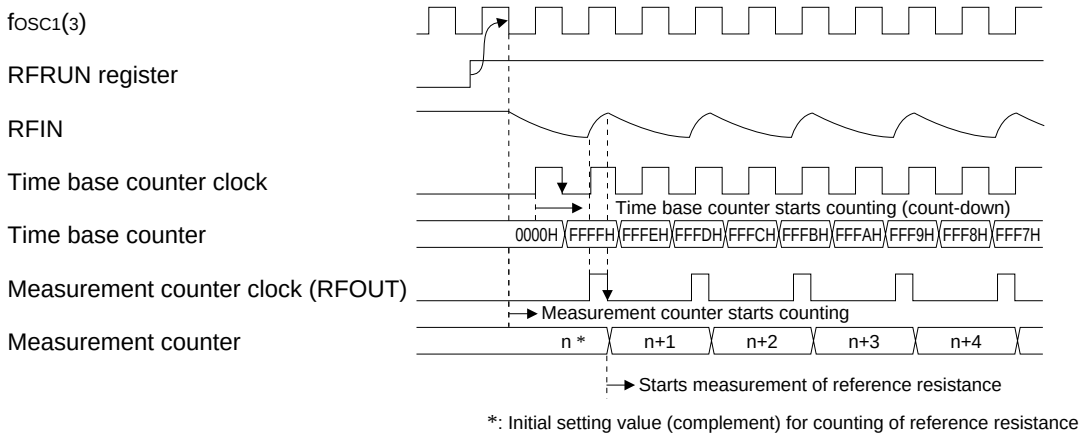


Fig. 4.10.3.1 Counting up start timing

If the measurement counter becomes "0000H" due to overflow, the oscillation is switched from the reference resistance side to the sensor side, and the measurement counter starts counting up according to the oscillation clock on the sensor side.
The time base counter shifts to the counting-up mode at this point and starts counting up from the value that has been counted while the reference resistance was oscillating.
Timing in switching oscillation is shown in Figure 4.10.3.2.
The sensor oscillation starts in synchronization with the counting of the time base counter after a measurement of the reference resistance has completed.

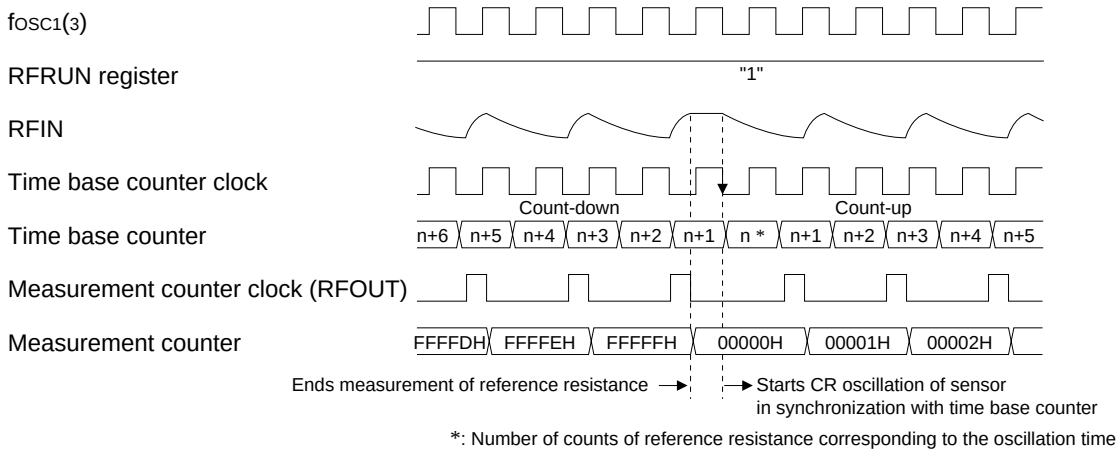


Fig. 4.10.3.2 Oscillation switch timing

When the time base counter has counted up to "0000H", the counting operation of both counters and CR oscillation stop, and an interrupt occurs. At the same time, the RFRUN register is set to "0", and the R/F converter circuit stops operation completely.
Figure 4.10.3.3 shows the R/F conversion end timing.
To prevent malfunction of the measurement counter, a CR oscillation clock is also counted in the measurement counter when the time base counter becomes "0000H". An interrupt occurs in synchronizing with the rising edge of OSC1 or OSC3 (one of these selected as the time base counter input clock) immediately after the measurement counter stops.
Further, the timing of the RFRUN register when it is set to "0" is the falling edge of the interrupt request signal.

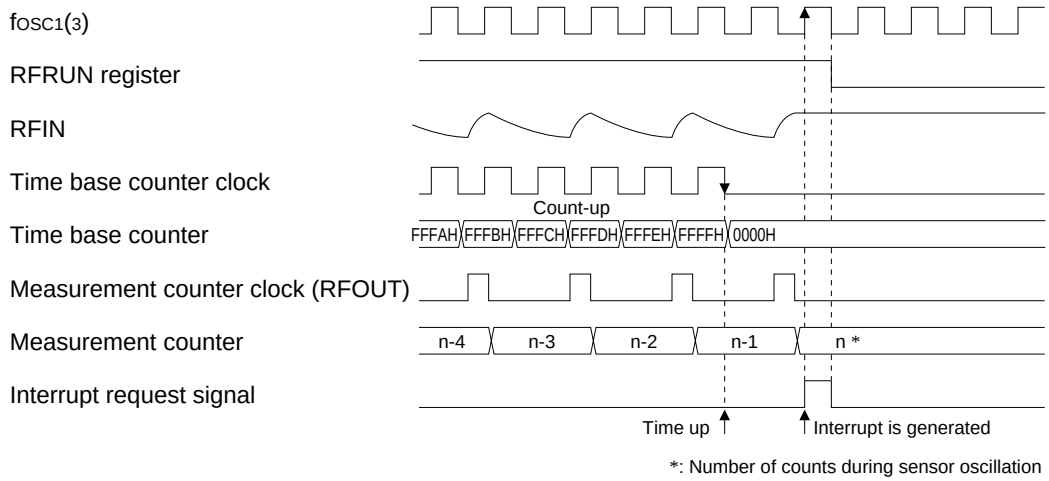


Fig. 4.10.3.3 R/F conversion end timing

By the above operation, the sensor is oscillated for the same period of time as the reference resistance is oscillated. Therefore, the difference in oscillation frequency can be measured from the values counted by the measurement counter.

Since the reference resistance is oscillated until the measurement counter overflows, an appropriate initial value needs to be set before R/F conversion is started. If a smaller initial value is set, a longer counting period is possible, thereby ensuring more accurate detection. However, the time base counter may overflow while counting the oscillation frequency of the reference resistance.
If an overflow occurs, CR oscillation and R/F conversion is terminated immediately. Also in such cases, interrupt occurs. Moreover, the measurement counter may overflow while counting the sensor oscillation depending on initial value setting. If the measurement counter overflows, CR oscillation and R/F conversion is terminated at that point and an interrupt occurs.
When these overflows occur, the correct value cannot be read. Therefore, the overflow flags are provided to judge whether the read data is correct or an overflow occurs. There are two overflow flags; OVMC (D2H • D2) that indicates an measurement counter overflow and OVTBC (D2H • D3) that indicates an time base counter overflow. These flags are set to "1" if respective counter overflows. These flags are reset to "0" when R/F conversion is started or when "1" is written to the flag. When the interrupt occurs, be sure to read the overflow flags and check overflow.
The initial value to be set depends on the measurable range by the sensor or where to set the reference resistance value within that range.
The initial value must be set taking the above into consideration.

Convert the initial value into a complement (value subtracted from 0000H) before setting it on the measurement counter. Since the data output from the measurement counter after R/F conversion matches data detected by the sensor, process the difference between that value and the initial value before it is converted into a complement according to the program and calculate the target value.

The above operations are shown in Figure 4.10.3.4.

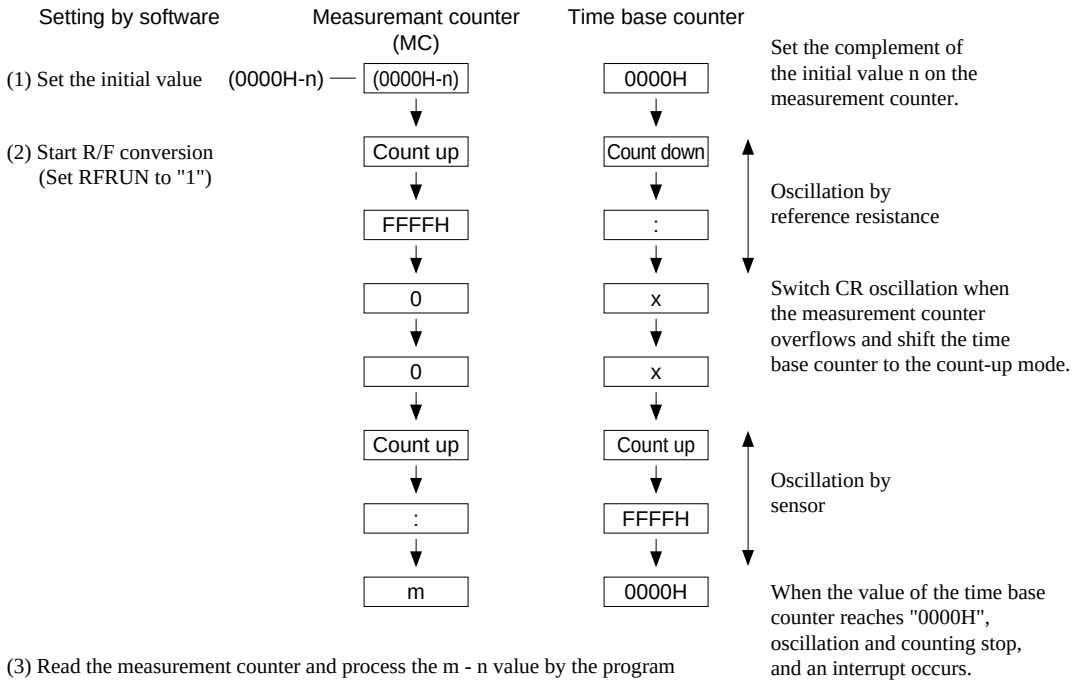


Fig. 4.10.3.4 Sequence of R/F conversion

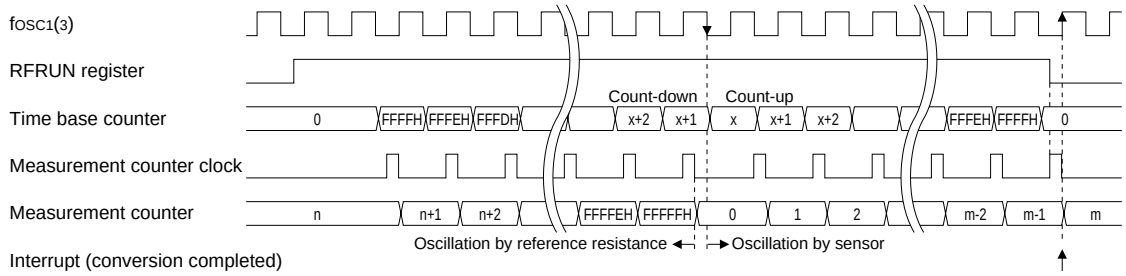
Note: Set the initial value of the measurement counter taking into account the measurable range and the overflow of counters.

(3) Operation mode

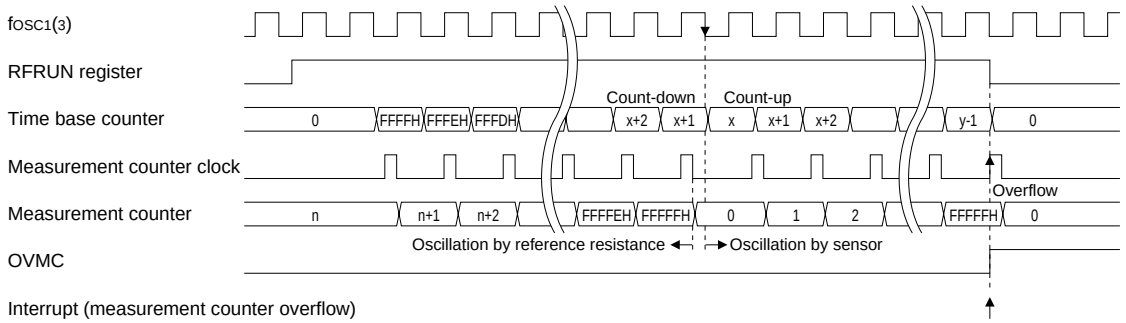
Thus far we explained the R/F converter to be operated in the normal mode.
The debug mode is set as an operating mode for the R/F converter in addition to the normal mode, and can be set by writing "1" to the register RFDBG (D0H•D2). To return to the normal mode, write "0" to the RFDBG.
The debug mode is provided for hardware/software debugging. It functions to continuously oscillate only the reference resistance side or sensor side. This function can measure the oscillation frequency by the resisters connected to each terminal. (Overflow of each counter and interrupt do not occur.) Sensor selection function is valid even in the debug mode. The oscillating operation starts by writing "1" to the RFRUN and is continued until "0" is written to the RFRUN.
Whether to oscillate the reference resistance or sensor is selected using the register DBGOS (D0H•D3). When "1" is written to the DBGOS register, the sensor side is selected. When "0" is written, the reference resister side is selected. This setting is valid only in the debug mode.

4.10.4 Interrupt function

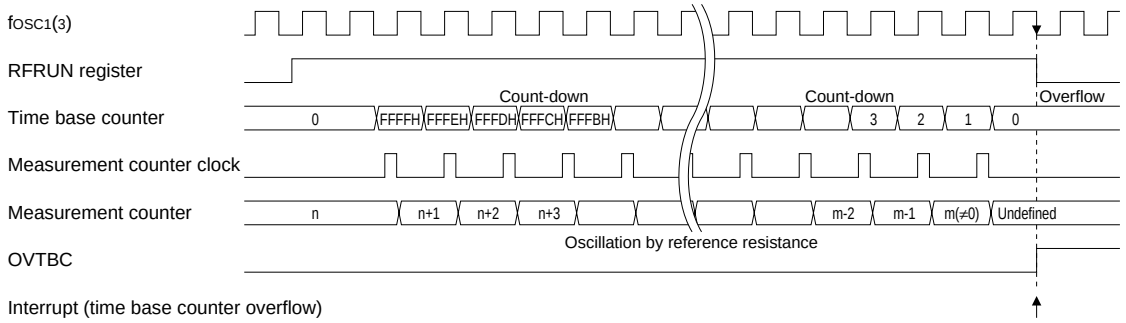
The R/F converter has a function which allows interrupt to occur after R/F conversion.
When the time base counter is counted up to "0000H", both counters stop counting. The interrupt factor flag IRF (F9H•D0) is set to "1" at the rising edge of the next clock (OSC1 or OSC3 clock that has been selected as the time base counter input clock).
If the time base counter overflows during counting of the reference resistance oscillation, or the measurement counter overflows during counting of the sensor oscillation, the interrupt factor flag IRF is also set to "1".
This interrupt factor allows masking by the interrupt mask register EIRF (F1H•D0). When the EIRF has been set at "1", an interrupt occurs in the CPU. When the EIRF is set at "0", no interrupt will occur in the CPU even if the interrupt factor flag is set to "1".
The interrupt factor flag is reset to "0" by reading.
Timing of interrupt by the R/F converter is shown in Figure 4.10.4.1.



(1) Completion interrupt



(2) Measurement counter overflow



(3) Time base counter overflow

Fig. 4.10.4.1 Timing of R/F converter interrupt

Note: • *When an interrupt occurs by the counter overflow, the same interrupt will occur if the overflow flag (OVMC or OVTBC) is not reset. Be sure to check and reset to "0" (writing "1") the overflow flag when the R/F converter interrupt occurs.*

• *Reading of interrupt factor flag is available at EI, but be careful in the following cases.*
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

4.10.5 Control of R/F converter

Table 4.10.5.1 lists the control bits and their addresses for the R/F converter.

Table 4.10.5.1 Control bits of R/F converter

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D0H	DBGOS	RFDBG	RFCLK	RFPWR	DBGOS	0	Sensor	Ref.-R	R/F converter debugging element selection
					RFDBG	0	Debug	Normal	R/F converter debug mode selection
	R/W				RFCLK	0	OSC3	OSC1	R/F converter clock source selection
					RFPWR	0	1	0	Reserved register
D1H	0	0	0	SENS0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					SENS0	0	SEN1	SEN0	Sensor selection
D2H	OVTBC	OVMC	RFRUN	0	OVTBC	0	Overflow	Non-ov	Time base counter overflow flag *6
					OVMC	0	Overflow	Non-ov	Measurement counter overflow flag *6
	R/W			R	RFRUN	0	Run	Stop	R/F converter Run/Stop
					0 *5	– *2			Unused
D3H	MC03	MC02	MC01	MC00	MC03	– *3			Measurement counter MC00–MC03
					MC02	– *3			
	R/W				MC01	– *3			
					MC00	– *3			
D4H	MC07	MC06	MC05	MC04	MC07	– *3			Measurement counter MC04–MC07
					MC06	– *3			
	R/W				MC05	– *3			
					MC04	– *3			
D5H	MC11	MC10	MC09	MC08	MC11	– *3			Measurement counter MC08–MC11
					MC10	– *3			
	R/W				MC09	– *3			
					MC08	– *3			
D6H	MC15	MC14	MC13	MC12	MC15	– *3			Measurement counter MC12–MC15
					MC14	– *3			
	R/W				MC13	– *3			
					MC12	– *3			
F1H	0	0	0	EIRF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIRF	0	Enable	Mask	Interrupt mask register (R/F converter)
F9H	0	0	0	IRF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IRF *4	0	Yes	No	Interrupt factor flag (R/F converter)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

DBGOS: Debugging element selection (D0H•D3)

Selects an element to be oscillated during the debug mode.

When "1" is written: Sensor
When "0" is written: Reference resistance
Reading: Valid

When "1" is written to DBGOS, sensor is continuously oscillated during the debug mode, and when "0" is written, reference resistance is continuously oscillated. This selection is valid only in the debug mode.
At initial reset, this register is set to "0".

RFDBG: Debug mode selection (D0H•D2)

Selects the debug mode of the R/F converter.

When "1" is written: Debug mode
When "0" is written: Normal mode
Reading: Valid

When "1" is written to RFDBG, the debug mode is selected, and when "0" is written, the normal mode is selected. When the debug mode is set, the oscillating operation of the element side selected by the DBGOS register can be done continuously.
At initial reset, this register is set to "0".

RFCLK: Input clock selection (D0H•D1)

Select an input clock of the time base counter.

When "1" is written: OSC3
When "0" is written: OSC1
Reading: Valid

When "1" is written to RFCLK, the OSC3 clock (Typ. 455 kHz) is selected. When "0" is written, the OSC1 clock (Typ. 32.768 kHz) is selected.
The initial value must be set on the measurement counter so that the time base counter will not overflow while CR oscillation is being counted.
At initial reset, these registers are set to "0".

SENS0: Sensor selection (D1H•D0)

Selects a sensor to be R/F-converted.

When "1" is written: SEN1
When "0" is written: SEN0
Reading: Valid

When "1" is written to SENS0, the sensor connected to the SEN1 terminal is selected. When "0" is written, the sensor connected to the SEN0 terminal is selected.
At initial reset, this register is set to "0".

MC0–MC15: Measurement counter (D3H–D6H)

This counter counts up according to the CR oscillation clock. It permits writing and reading on a 4-bit basis. The complement of the number of clocks to be counted by the oscillation of the reference resistance, must be entered in this counter prior to R/F conversion.
If R/F conversion is initiated, the counter counts up from the set initial value, first according to the oscillation clock of the reference resistance. When the counter reaches "0000H" due to overflow, the oscillation of the reference resistance stops, and the sensor starts oscillating. The counter continues counting according to the sensor oscillation clock. Counting time during the CR oscillation of the reference resistance is calculated by the time base counter. The measurement counter stops counting when the same period of time elapses. Number of clocks counted by the sensor oscillation can be evaluated from the value indicated by the counter when it stops. Calculate the target value by processing the above counted number according to the program.
Measurable range and the overflow of the counter must be taken into account when setting an initial value to be entered prior to R/F conversion.
After an initial reset, data in this counter become indefinite.

RFRUN: R/F conversion RUN/STOP (D2H•D1)

Starts R/F conversion and indicates the operating (RUN/STOP) status.

When "1" is written: R/F conversion starts
When "0" is written: R/F conversion stops

When "1" is read: RUN status
When "0" is read: STOP status

When "1" is written to RFRUN, R/F conversion starts. The register remains at "1" during R/F conversion and is set to "0" when R/F conversion is terminated.
When "0" is written to RFRUN during R/F conversion, R/F conversion is paused.
This register is set to "0" at initial reset, when the time base counter or measurement counter overflows, or when measurement is finished.

OVMC: Measurement counter overflow flag (D2H•D2)

Indicates whether the measurement counter has overflown.

When "1" is read: Overflow has occurred
When "0" is read: Overflow has not occurred

When "1" is written: Flag reset
When "0" is written: No operation

If an overflow occurs while counting the oscillation of the sensor, OVMC is set to "1" and the interrupt occurs at the same time.
This flag is reset by writing "1" or starting R/F conversion.
At initial reset, this flag is set to "0".

OVTBC: Time base counter overflow flag (D2H•D3)

Indicates whether the time base counter has overflown.

When "1" is read: Overflow has occurred
When "0" is read: Overflow has not occurred

When "1" is written: Flag reset
When "0" is written: No operation

If an overflow occurs while counting the oscillation of the reference resistance, OVTBC is set to "1" and the interrupt occurs at the same time.
This flag is reset by writing "1" or starting R/F conversion.
At initial reset, this flag is set to "0".

EIRF: Interrupt mask register (F1H•D0)

Select whether to mask interrupt with the R/F converter.

When "1" is written: Enable
When "0" is written: Mask
Reading: Valid

The R/F converter interrupt is permitted when "1" is written to EIRF. When "0" is written, interrupt is masked.
At initial reset, this register is set to "0".

IRF: Interrupt factor flag (F9H•D0)

This flag indicates the status of the R/F converter interrupt.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

IRF is set to "1" when R/F conversion is terminated, when the time base counter overflows while counting the oscillation of the reference resistance, or the measurement counter overflows while counting the oscillation of the sensor.
From the status of this flag, the software can decide whether an R/F converter interrupt has occurred.
Further this flag is set in the above timing regardless of the interrupt mask register setting.
This flag is reset when the software has read it.
Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.
After an initial reset, this flag is set to "0".

4.10.6 Programming notes

(1) Depending on the initial value of the measurement counter (MC), the measurement counter (MC) or the time base counter may overflow while the CR oscillation clock is being counted. When setting the initial value, pay attention to CR oscillation frequency, its fluctuation range and the input clock frequency of the time base counter. If an overflow occurs, R/F conversion is terminated immediately. When the R/F conversion result (measurement counter value) is read, check the overflow flags (OVMC and OVTBC).

(2) When an interrupt occurs by the counter overflow, the same interrupt will occur if the overflow flag (OVMC or OVTBC) is not reset. Be sure to check and reset to "0" (writing "1") the overflow flag when the R/F converter interrupt occurs.

(3) When using the OSC3 clock as the time base counter input clock, the OSC3 oscillation circuit must be ON (OSCC = "1") before starting R/F conversion.
It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when starting a remote output, secure 5 msec or more waiting time for oscillation stabilization after turning the OSC3 oscillation ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the waiting time.

(4) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

4.11 SVD (Supply Voltage Detection) Circuit

4.11.1 Configuration of SVD circuit

The S1C621C0 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers. Turning the SVD circuit ON / OFF can be controlled by the software.
The criteria voltage for evaluating the supply voltage is set to 2.3 V ± 0.15 V and whether the supply voltage is more or less it can be read as data by the software.
Figure 4.11.1.1 shows the configuration of the SVD circuit.

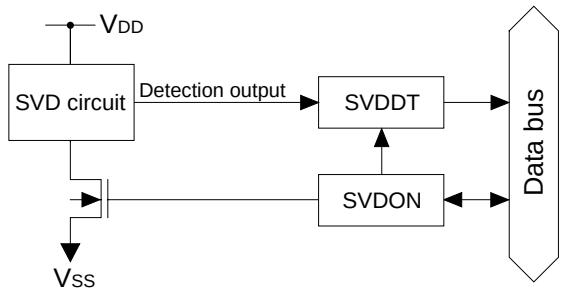


Fig. 4.11.1.1 Configuration of SVD circuit

4.11.2 SVD operation

When SVDON is set to "1", source voltage detection by the SVD circuit is executed. The SVD circuit compares the criteria voltage (2.3 V ± 0.15 V) and the supply voltage (V_{DD}–V_{SS}). As soon as SVDON is reset to "0", the result is loaded to in the SVDDT latch and SVD circuit goes OFF. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.

To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

① Set SVDON to "1"
② Maintain for 100 µsec minimum
③ Set SVDON to "0"
④ Read SVDDT

However, when f_{OSC1} is selected for CPU system clock, the instruction cycles are long enough, so there is no need to worry about maintaining 100 µsec for SVDON = "1" in the software.
The detected data latched in SVDDT is maintained until the SVD circuit is operated again and a new detection result is latched.
When SVD is on, the IC draws a large current, so keep SVD off unless it is.

4.11.3 Control of SVD circuit

Table 4.11.3.1 shows the control bits and their addresses for the SVD circuit.

Table 4.11.3.1 Control bits for SVD circuit

Address *7	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
80H	0	0	SVDDT	SVDON	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	Supply voltage detection data
					SVDON	0	On	Off	SVD circuit On/Off

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

SVDON: SVD circuit ON/OFF (80H•D0)

Turns the SVD circuit ON and OFF.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

When SVDON is set to "1", source voltage detection by the SVD circuit is executed. As soon as SVDON is reset to "0", the result is loaded to in the SVDDT latch. To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec.
At initial reset, this register is set to "0".

SVDDT: SVD data (80H•D1)

This is the result of supply voltage detection.

When "0" is read: Supply voltage (V_{DD}–V_{SS}) ≥ Criteria voltage
When "1" is read: Supply voltage (V_{DD}–V_{SS}) < Criteria voltage
Writing: Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this latch.
At initial reset, SVDDT is set to "0".

4.11.4 Programming notes

(1) To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

① Set SVDON to "1"
② Maintain for 100 µsec minimum
③ Set SVDON to "0"
④ Read SVDDT

However, when f_{OSC1} is selected for CPU system clock, the instruction cycles are long enough, so there is no need to worry about maintaining 100 µsec for SVDON = "1" in the software.

(2) The SVD circuit should normally be turned OFF as the consumption current of the IC becomes large when it is ON.

4.12 Interrupt and HALT

<Interrupt types>

The S1C621C0 provides the following interrupt settings, each of which is maskable.

External interrupt:	• Input port interrupt	(2 systems)
Internal interrupt:	• Clock timer interrupt	(3 systems)
	• Remote controller interrupt	(1 system)
	• R/F converter interrupt	(1 system)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).
When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.
Figure 4.12.1 shows the configuration of the interrupt circuit.

<HALT>

The S1C621C0 has HALT function that considerably reduce the current consumption when it is not necessary.

The CPU enters the HALT status when the HALT instruction is executed.
In the HALT status, the operation of the CPU is stopped. However, the oscillation circuit operates. Reactivating the CPU from the HALT status is done by generating an interrupt request. When it does not reactivate upon an interrupt request, the watchdog timer will cause it to restart from the initial reset status.

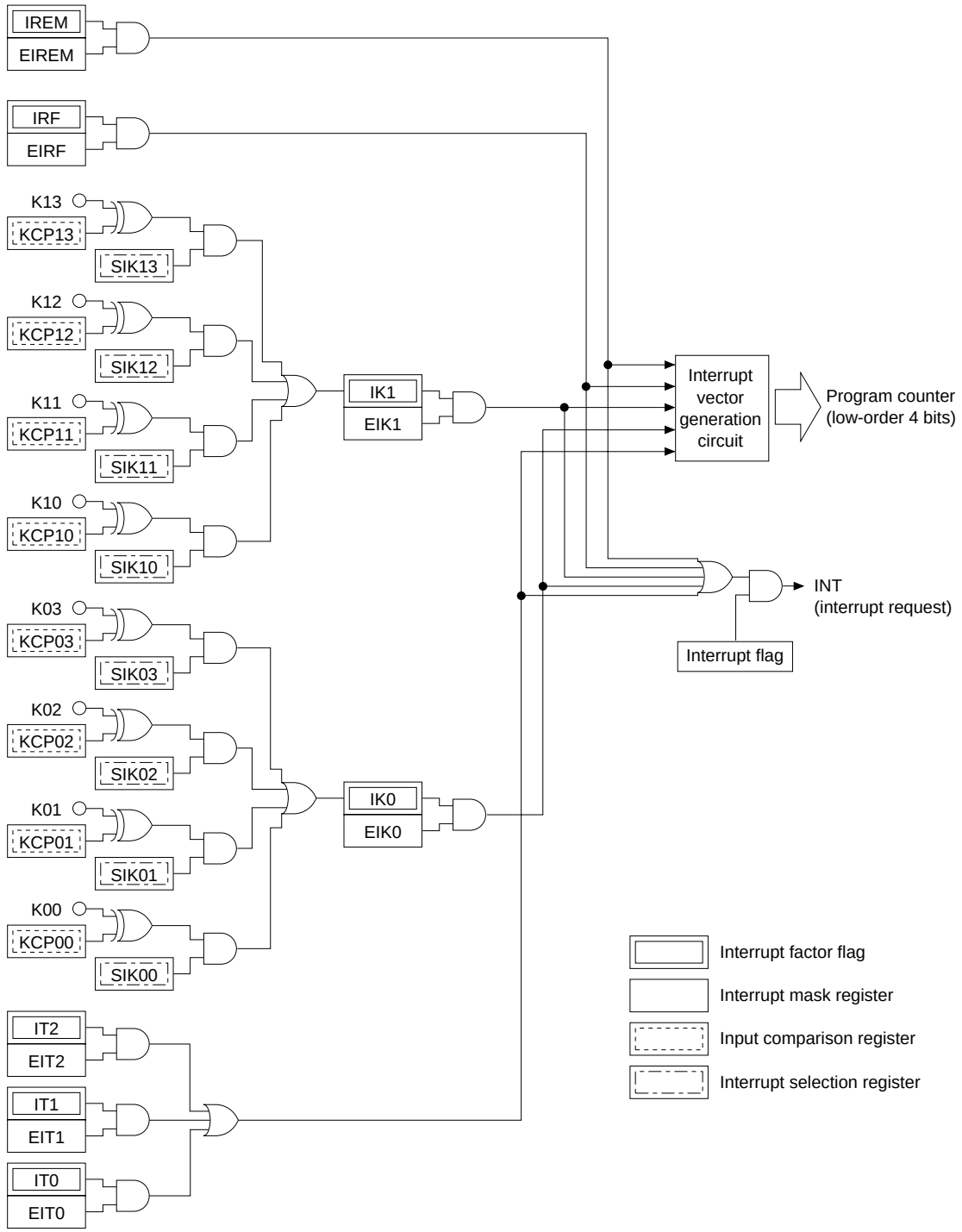


Fig. 4.12.1 Configuration of the interrupt circuit

4.12.1 Interrupt factor

Table 4.12.1.1 shows the factors for generating interrupt requests.

The interrupt flags are set to "1" depending on the corresponding interrupt factors.
The CPU operation is interrupted when any of the conditions below set an interrupt factor flag to "1".

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is a read-only register, but can be reset to "0" when the register data is read out.
At initial reset, the interrupt factor flags are reset to "0".

Table 4.12.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag
Remote controller (set τ cycle has passed)	IREM (F8H•D0)
R/F converter (R/F conversion has completed)	IRF (F9H•D0)
K10–K13 input (falling or rising edge)	IK1 (FAH•D0)
K00–K03 input (falling or rising edge)	IK0 (FBH•D0)
Clock timer 2 Hz (falling edge)	IT2 (FCH•D2)
Clock timer 8 Hz (falling edge)	IT1 (FCH•D1)
Clock timer 32 Hz (falling edge)	IT0 (FCH•D0)

Note: Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

4.12.2 Interrupt mask

The interrupt factor flags can be masked by the corresponding interrupt mask registers.
The interrupt mask registers are read / write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.
At initial reset, the interrupt mask register is set to "0".
Table 4.12.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.12.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register	Interrupt factor flag
EIREM (F0H•D0)	IREM (F8H•D0)
EIRF (F1H•D0)	IRF (F9H•D0)
EIK1 (F2H•D0)	IK1 (FAH•D0)
EIK0 (F3H•D0)	IK0 (FBH•D0)
EIT2 (F4H•D2)	IT2 (FCH•D2)
EIT1 (F4H•D1)	IT1 (FCH•D1)
EIT0 (F4H•D0)	IT0 (FCH•D0)

4.12.3 Interrupt vector

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

① The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).

② The interrupt request causes the value of the interrupt vector (page 1, 02H–0BH) to be set in the program counter.

③ The program at the specified address is executed (execution of interrupt processing routine by software).

Table 4.12.3.1 shows the correspondence of interrupt requests and interrupt vectors.

Note: The processing in ① and ② above take 12 cycles of the CPU system clock.

Table 4.12.3.1 Interrupt request and interrupt vectors

Interrupt vector	Interrupt request	Priority
102H	Remote controller	High
104H	R/F converter	↑
106H	K10–K13 input	
108H	K00–K03 input	↓
10AH	Clock timer	Low

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

4.12.4 Control of interrupt

Tables 4.12.4.1(a) and (b) show the interrupt control bits and their addresses.

Table 4.12.4.1(a) Control bits of interrupt (1)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
90H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	Interrupt selection register (K00–K03)
					SIK02	0	Enable	Disable	
					SIK01	0	Enable	Disable	
	R/W				SIK00	0	Enable	Disable	
92H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	Input comparison register (K00–K03)
					KCP02	1	↓	↑	
					KCP01	1	↓	↑	
	R/W				KCP00	1	↓	↑	
94H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	Interrupt selection register (K10–K13)
					SIK12	0	Enable	Disable	
					SIK11	0	Enable	Disable	
	R/W				SIK10	0	Enable	Disable	
96H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	Input comparison register (K10–K13)
					KCP12	1	↓	↑	
					KCP11	1	↓	↑	
	R/W				KCP10	1	↓	↑	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

Table 4.12.4.1(b) Control bits of interrupt (2)

Address *7	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F0H	0	0	0	EIREM	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIREM	0	Enable	Mask	Interrupt mask register (Remote controller)
F1H	0	0	0	EIRF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIRF	0	Enable	Mask	Interrupt mask register (R/F converter)
F2H	0	0	0	EIK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
F3H	0	0	0	EIK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	0 *5	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
F4H	0	EIT2	EIT1	EIT0	0 *5	– *2			Unused
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R	R/W			EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
F8H	0	0	0	IREM	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IREM *4	0	Yes	No	Interrupt factor flag (Remote controller)
F9H	0	0	0	IRF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IRF *4	0	Yes	No	Interrupt factor flag (R/F converter)
FAH	0	0	0	IK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
FBH	0	0	0	IK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
FCH	0	IT2	IT1	IT0	0 *5	– *2			Unused
					IT2 *4	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R				IT1 *4	0	Yes	No	Interrupt factor flag (Clock timer 8 Hz)
					IT0 *4	0	Yes	No	Interrupt factor flag (Clock timer 32 Hz)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Reset (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual
*7 Page switching in I/O memory is not necessary

EIREM: Interrupt mask register (F0H•D0)
IREM: Interrupt factor flag (F8H•D0)

..... See Section 4.9, "Remote Controller (REM)".

EIRF: Interrupt mask register (F1H•D0)
IRF: Interrupt factor flag (F9H•D0)

..... See Section 4.10, "R/F Converter".

KCP13–KCP10: Input comparison registers (96H)
SIK13–SIK10: Interrupt selection registers (94H)
EIK1: Interrupt mask register (F2H•D0)
IK1: Interrupt factor flag (FAH•D0)

..... See Section 4.4, "Input Ports".

KCP03–KCP00: Input comparison registers (92H)
SIK03–SIK00: Interrupt selection registers (90H)
EIK0: Interrupt mask register (F3H•D0)
IK0: Interrupt factor flag (FBH•D0)

..... See Section 4.4, "Input Ports".

EIT2, EIT1, EIT0: Interrupt mask registers (F4H•D2–D0)
IT2, IT1, IT0: Interrupt factor flags (FCH•D2–D0)

..... See Section 4.8, "Clock Timer".

4.12.5 Programming notes

(1) The interrupt factor flags are set when the timing condition is established, even if the interrupt mask registers are set to "0".

(2) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

CHAPTER 5 SUMMARY OF NOTES

5.1 Notes for Low Current Consumption

The S1C621C0 contains control registers for each of the circuits so that current consumption can be lowered. These control registers lower the current consumption through programs that operate the circuits at the minimum levels.
The following text explains the circuits that can control operation and their control registers. Refer to these when putting programs together.

Table 5.1.1 Circuits and control registers

Circuit (and Item)	Control register
CPU	HALT instruction
CPU operating frequency	CLKCHG, OSCC
LCD power supply circuit	LPWR
Remote controller	REMCR, REMDC
SVD circuit	SVDON

See Chapter 7, "ELECTRICAL CHARACTERISTICS", for order of current consumption.

Below are the circuit statuses at initial reset.

CPU: Operating status

CPU operating frequency: Low speed side (CLKCHG = "0"),
OSC3 oscillation circuit OFF status (OSCC = "0")

LCD power supply circuit: OFF status (LPWR = "0")

Remote controller: OFF status (REMCR = REMDC = "0")

SVD circuit: OFF status (SVDON = "0")

Also, be careful about panel selection because the current consumption can differ by the order of several µA on account of the LCD panel characteristics.

5.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory

Memory is not mounted in unused area within the memory map and in memory area not indicated in this manual. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Watchdog timer

When the watchdog timer is being used, the software must reset it within 3-second cycles.

Oscillation circuit

(1) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

OSC1 → OSC3
1. Set OSCC to "1" (OSC3 oscillation ON)
2. Maintain 5 msec or more
3. Set CLKCHG to "1" (OSC1 → OSC3)

OSC3 → OSC1
1. Set CLKCHG to "0" (OSC3 → OSC1)
2. Set OSCC to "0" (OSC3 oscillation OFF)

(2) When switching the clock form OSC3 to OSC1, use a separate instruction for turning the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(3) If it is not necessary to operate the CPU in high-speed and the OSC3 clock is not needed for some peripheral circuits, turn the OSC3 oscillation circuit off (CLKCHG = "0", OSCC = "0") to reduce current consumption.

Input ports

(1) When input ports are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN}$ + load capacitance on board) $\times$ 1.6 [sec]
R_{IN}: pull up resistance (Max. value)
C_{IN}: terminal capacitance (Max. value)

(2) When the input comparison register (KCP00–KCP03, KCP10–KCP13) is set, the interrupt factor flag (IK0, IK1) may be set to "1" depending on the status of the input port terminal. Consequently, when setting this register, do it in the DI status (interrupt flag = "0") and then read the interrupt factor flag in order to reset, or after setting the interrupt selection register (SIK00–SIK03, SIK10–SIK13) to the interrupt disabled status.

Output ports

(1) When R00–R03 are used as DC output, the special output enable registers REMCR (R00), REMDC (R01), FOUTE (R02) and BZE (R03) should be fixed at "0".

(2) When the special output is selected, the corresponding output port register (R00–R03) should be fixed at "0". Be aware that the output terminal is fixed at a high (V_{DD}) level the same with the DC output if "1" is written to the R00–R03 register when the special output has been selected.

(3) When BZ and FOUT are selected, a hazard may be observed in the output waveform when the data of the output register changes.

(4) When selecting f_{OSC3} as the FOUT clock frequency, it is necessary to control the OSC3 oscillation circuit. See Section 4.3, "Oscillation Circuit" for details of the control.

I/O ports

When input terminals are changed from low to high by pull up resistor, the rise of the waveform is delayed on account of the time constant of the pull up resistor and input gate capacitance. Hence, when fetching data during input mode, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

Waiting time = $R_{IN} \times (C_{IN}$ + load capacitance on board) $\times$ 1.6 [sec]
R_{IN}: pull up resistance (Max. value)
C_{IN}: terminal capacitance (Max. value)

LCD driver

(1) The contents of the display memory are undefined until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) When page 4 is selected for the display memory area, since the display memory area is write-only, display data cannot be rewritten by arithmetic operations (such as AND, OR, ADD, SUB).

(3) 100 msec or more time is necessary for stabilizing the LCD drive voltages V_{C1}, V_{C2} and V_{C3} after setting the LCD power control register LPWR to "1". Be careful of the segment-on right after the power is turned on.

Clock timer

(1) Be sure to data reading in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag reading (reset the flag) as necessary at reset.

Remote controller

(1) When using the remote control outputs, fix the R00 and R01 registers at "0" and do not change them. (If the REMDC output is not used, the R01 register and terminal can be used as an output port.)

(2) Except when outputting the remote control waveform, both REMCR and REMDC registers should be fixed at "0" to prevent outputting unnecessary waveform and to reduce current consumption.

(3) When performing remote output, it is necessary that the OSC3 oscillation circuit has already been ON. Remote output should be started when the OSC3 oscillation is stabilized.
It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when starting a remote output, secure 5 msec or more waiting time for oscillation stabilization after turning the OSC3 oscillation ON.
Further, the oscillation stabilization time varies depending ON the external oscillator characteristics and conditions of use, so allow ample margin when setting the waiting time.

(4) The setting of the RCDIV register (carrier cycle), RCDTY register (carrier duty ratio) and RT1/RT0 registers (τ reference cycle) should be done when the REM circuit is OFF (REMCR = REMDC = "0") before starting remote transmission. Changing the contents when the REM circuit is ON may cause a malfunction.

(5) When performing remote output in the soft-timer mode, be sure to control the carrier output using the REMSO register. Do not control the carrier output using the REMCR register by setting the REMSO register to "1". Similarly, in the case of REMDC output, do not control the output using the REMDC register.

(6) REMSO is for the exclusive use of the soft-timer mode. When controlling with the hard-timer mode, REMSO should be fixed at "0".

(7) When performing remote output in the hard-timer mode, do not write data to the ROUT3–ROUT0 register while the τ waveform is high to prevent malfunction. Furthermore, next transmission data writing should be done after the current carrier output is completed unless done intentionally. If this register is written during carrier output, it stops output at that point of the falling edge of the τ waveform after the writing and starts new carrier output.
Furthermore, the ROUT3–ROUT0 register is for the exclusive use of the hard-timer mode. When controlling with the soft-timer mode, be sure not to write data to this register to prevent malfunction.

(8) When performing remote output in the hard-timer mode, do not write data to the RIC3–RIC0 register while τ waveform is high to prevent malfunction. If this register is re-written before generating the interrupt corresponding the previous written data, the interrupt counter is renewed and the previous set interrupt becomes invalid.
Furthermore, the RIC3–RIC0 register is for the exclusive use of the hard-timer mode. When controlling with the soft-timer mode, be sure not to write data to this register to prevent malfunction.

(9) The soft-timer mode and the hard-timer mode can not be used at the same time. To use them in combination, set both REMCR and REMDC registers to "0" to stop the REM circuit before switching the mode.

R/F converter

(1) Depending on the initial value of the measurement counter (MC), the measurement counter (MC) or the time base counter may overflow while the CR oscillation clock is being counted. When setting the initial value, pay attention to CR oscillation frequency, its fluctuation range and the input clock frequency of the time base counter. If an overflow occurs, R/F conversion is terminated immediately. When the R/F conversion result (measurement counter value) is read, check the overflow flags (OVMC and OVTBC).

(2) When an interrupt occurs by the counter overflow, the same interrupt will occur if the overflow flag (OVMC or OVTBC) is not reset. Be sure to check and reset to "0" (writing "1") the overflow flag when the R/F converter interrupt occurs.

(3) When using the OSC3 clock as the time base counter input clock, the OSC3 oscillation circuit must be ON (OSCC = "1") before starting R/F conversion.
It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when starting a remote output, secure 5 msec or more waiting time for oscillation stabilization after turning the OSC3 oscillation ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the waiting time.

SVD circuit

(1) To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

① Set SVDON to "1"
② Maintain for 100 µsec minimum
③ Set SVDON to "0"
④ Read SVDDT

However, when f_{OSC1} is selected for CPU system clock, the instruction cycles are long enough, so there is no need to worry about maintaining 100 µsec for SVDON = "1" in the software.

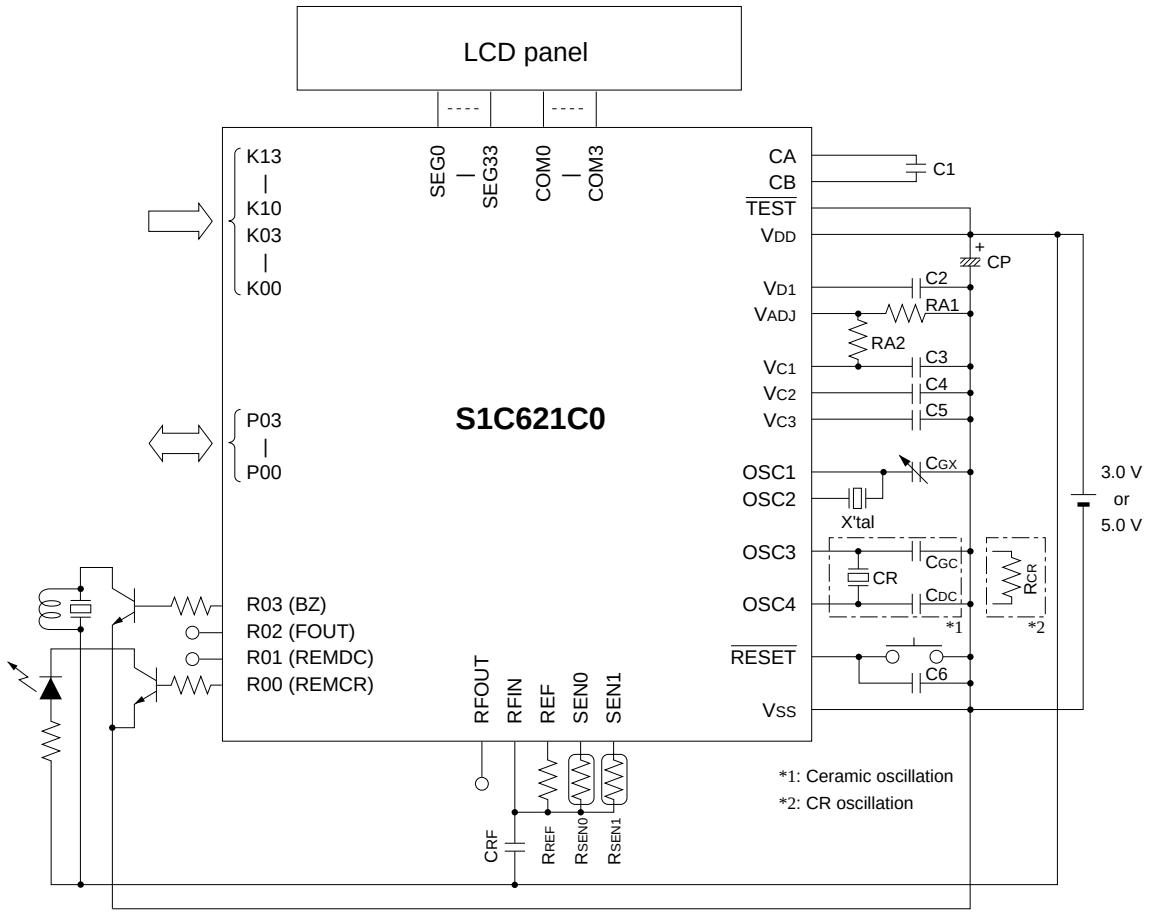
(2) The SVD circuit should normally be turned OFF as the consumption current of the IC becomes large when it is ON.

Interrupt and HALT

(1) The interrupt factor flags are set when the timing condition is established, even if the interrupt mask registers are set to "0".

(2) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

CHAPTER 6 DIAGRAM OF BASIC EXTERNAL CONNECTIONS



X'tal	Crystal oscillator	32.768 kHz, CI(Max.) = 35kΩ
CGX	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	455 kHz (Typ.)
CGC	Gate capacitor	100 pF
CDC	Drain capacitor	100 pF
RCR	CR oscillating resistor	33 kΩ (980 kHz, Typ.)
RREF	Reference resistance for R/F conversion	50 kΩ
RSEN0	Sensor 0 for R/F conversion (DC bias)	503AT-2 *3
RSEN1	Sensor 1 for R/F conversion (DC bias)	503AT-2 *3
CRF	Capacitor for R/F conversion	2,200 pF
RA1	Resistor for VC1 adjustment	Open (VC1 = 1.0 V), 2 MΩ (VC1 = 1.5 V)
RA2	Resistor for VC1 adjustment	Short (VC1 = 1.0 V), 1 MΩ (VC1 = 1.5 V)
C1–C6	Capacitor	0.1 µF
CP	Power capacitor	3.3 µF

*3: Made by Ishizuka Electronics Corporation

Note: The above table is simply an example, and is not guaranteed to work.

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

(V_{SS} = 0 V)

Item	Symbol	Rated value	Unit
Power voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-40 to 85	°C
Strage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible disspation *2	P_D	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is drawn in).

*2 In case of plastic package (QFP5-80pin).

7.2 Recommended Operating Conditions

(Ta = -40 to 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power voltage	V_{DD}	V_{SS} = 0 V	2.2	3.0	5.5	V
Oscillation frequency	f_{OSC1}		–	32.768	–	kHz
	f_{OSC3}	Duty 50±10%	300	500	1,300	kHz
LCD output voltage	V_{C1}			1.05	1.60	V

7.3 DC Characteristics

Unless otherwise specified:

V_{SS} = 0 V, V_{DD} = 3.0 V, f_{OSC1} = 32.768 kHz, Ta = 25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3} are internal voltage, C1–C6 = 0.1 µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–K03, K10–K13 P00–P03	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–K03, K10–K13 P00–P03	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH} = 3.0 V	K00–K03, K10–K13 P00–P03 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1} = V_{SS} Without pull up resistor	K00–K03, K10–K13 P00–P03	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2} = V_{SS} With pull up resistor	K00–K03, K10–K13 P00–P03 $\overline{RESET}$, $\overline{TEST}$	-15	-10	-5	µA
High level output current	I_{OH1}	V_{OH1} = 0.9·V_{DD}	R00–R03, P00–P03 RFOUT			-1	mA
Low level output current	I_{OL1}	V_{OL1} = 0.1·V_{DD}	R00–R03, P00–P03 RFOUT	3			mA
Common output current	I_{OH2}	V_{OH2} = V_{C3} - 0.05 V	COM0–COM3			-3	µA
	I_{OL2}	V_{OL2} = V_{SS} + 0.05 V		3			µA
Segment output current	I_{OH3}	V_{OH3} = V_{C3} - 0.05 V	SEG0–SEG33			-3	µA
(during LCD output)	I_{OL3}	V_{OL3} = V_{SS} + 0.05 V		3			µA
Segment output current	I_{OH4}	V_{OH4} = 0.9·V_{DD}	SEG0–SEG33			-200	µA
(during DC output)	I_{OL4}	V_{OL4} = 0.1·V_{DD}		200			µA

7.4 Analog Characteristics and Consumed Current

Unless otherwise specified:

V_{SS} = 0 V, V_{DD} = 3.0 V, f_{OSC1} = 32.768 kHz, C_G = 25 pF, R_{REF} = 50 kΩ, C_{RF} = 2,200 pF

Ta = 25°C, V_{D1}/V_{C1}/V_{C2}/V_{C3} are internal voltage, C1–C6 = 0.1 µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{C1}	V_{ADJ} = V_{C1}, I_{C1} = 5 µA		0.95	1.05	1.15	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2} (Without panel load)		2·V_{C1} × 0.9		2·V_{C1} + 0.1	V V
	V_{C3}	Connect 1MΩ load resistor between V_{SS} and V_{C3} (Without panel load)		3·V_{C1} × 0.9		3·V_{C1} + 0.1	V V
SVD voltage	V_{SVD}			2.15	2.30	2.45	V
SVD circuit responce time	t_{SVD}					100	µS
Power current consumption	I_{OP}	During HALT (32 kHz)	Without panel load		3	6	µA
		During execution (32 kHz) *1			7	15	nA
		During execution (455 kHz) *1			170	300	µA
		During execution (1 MHz) *1			250	500	µA
		During execution (32 kHz) *2			40	120	µA
		During execution (32 kHz) *3			10	30	µA

*1 The R/F converter and SVD circuit are in OFF status.

*2 The R/F converter is in ON status. The SVD circuit is in OFF status.

*3 The R/F converter is in OFF status. The SVD circuit is in ON status.

7.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

Unless otherwise specified:

V_{SS} = 0 V, V_{DD} = 3.0 V, Crystal: Q13MC146, CI = 35 kΩ, C_G = 25 pF, C_D = built-in, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta ≤ 3 sec (V_{DD})	2.2			V
Oscillation stop voltage	Vstp	tstp ≤ 10 sec (V_{DD})	2.2			V
Built-in capacitance (drain)	C_D	Including incidental capacitance inside IC		20		pF
Frequency/voltage deviation	∂f/∂V	V_{DD} = 2.2 to 5.5 V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G = 5 to 25 pF	35			ppm
Harmonic oscillation start voltage	V_{hho}	C_G = 5 pF (V_{DD})			7	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

OSC3 CR oscillation circuit

Unless otherwise specified:

V_{SS} = 0 V, V_{DD} = 3.0 V, R_{CR} = 33 kΩ, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	(1 MHz)	30	%
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD} = 2.2 to 5.5 V			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

OSC3 ceramic oscillation circuit

Unless otherwise specified:

V_{SS} = 0 V, V_{DD} = 3.0 V, Ceramic oscillator: 1 MHz, C_{GC} = C_{DC} = 100 pF, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD} = 2.2 to 5.5 V			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

7.6 CR Oscillation Characteristics

The following characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

(1) CR oscillation frequency characteristic

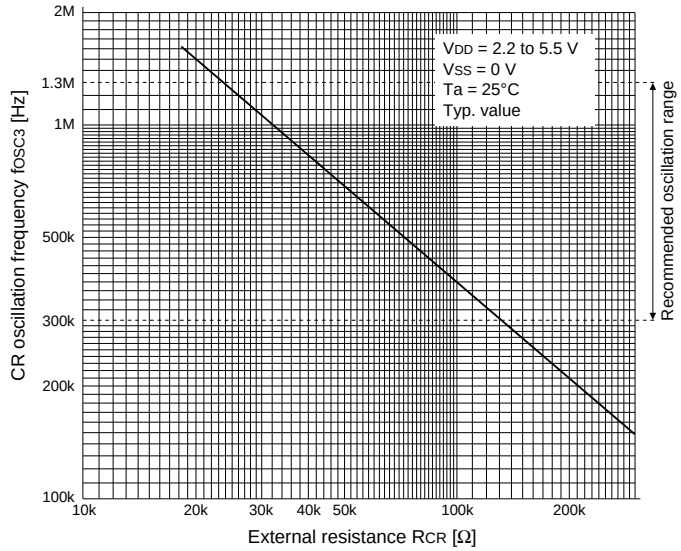


Fig. 7.6.1 CR oscillation characteristic

(2) Frequency-Current consumption characteristic

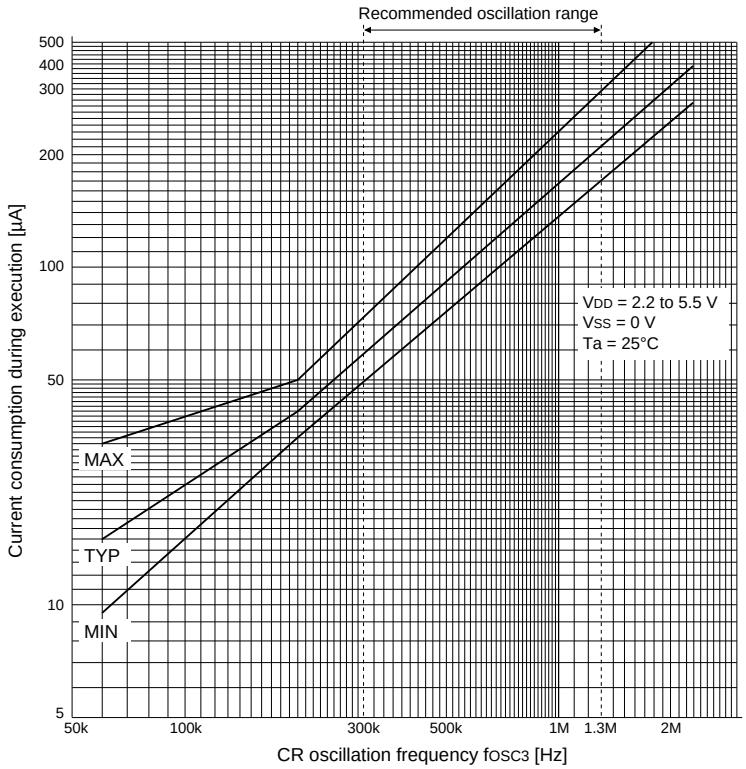


Fig. 7.6.2 Frequency-current consumption characteristic

7.7 R/F Converter Characteristics

The following characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

Unless otherwise specified:

V_{SS} = 0 V, V_{DD} = 3.0 V, f_{OSC1} = 32.768 kHz, C_{RF} = 2,200 pF, R_{REF} = 10 kΩ or 50 kΩ, Ta = -40°C to 85°C
The following values do not include errors caused by changing temperature of the external attached elements (R_{REF}, C_{RF})

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
R/F conversion counter value	C_{RS1}	1 kΩ ≤ R_{SEN} < 10 kΩ	MC×0.93		MC×1.07	count
	C_{RS2}	10 kΩ ≤ R_{SEN} ≤ 2 MΩ	MC×0.97 -15		MC×1.03 +15	count

$$* MC = \frac{R_{REF}\,[k\Omega] + 0.15}{R_{SEN}\,[k\Omega] + 0.15} \times \text{Measurement counter value}$$

(1) Sensor resistance-Oscillation frequency ratio

Figure 7.7.1 shows the oscillation frequency ratio (ratio of oscillation frequency by the reference resistance to oscillation frequency by the sensor resistance) when the following elements are connected. (Typ.)
If the R/F conversion uses SEN0 or SEN1, both characteristics will be the same.

Reference resistance (R_{REF}) ..... 10 kΩ
Sensor resistance (R_{SEN0}, R_{SEN1}) ..... 10 kΩ to 20 MΩ
Oscillating capacitor (C_{RF}) ..... 2,200 pF

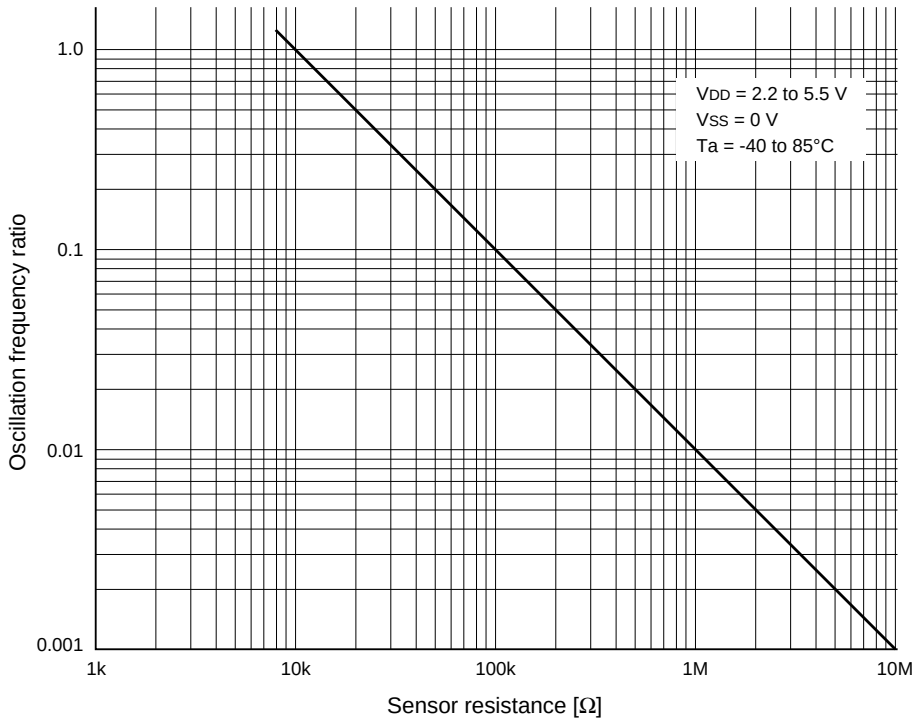


Fig. 7.7.1 Oscillation frequency ratio-resistance curve

(2) Resistance-Oscillation frequency

CR oscillation frequency of the R/F converter disperses in each sampling. Therefore, the initial setting value of the measurement counter should be decided after considering the fluctuation margin of the CR oscillation frequency by the reference resistance and sensor resistance to be used for the measurement. Figures 7.7.2 and 7.7.3 show the resistance-oscillation frequency curves.

Note: • The following curves are characteristic when the oscillating capacitor is 2,200 pF.

• Typical oscillation frequency is characteristic when V_{DD} = 3.0 V and Ta = 25°C.

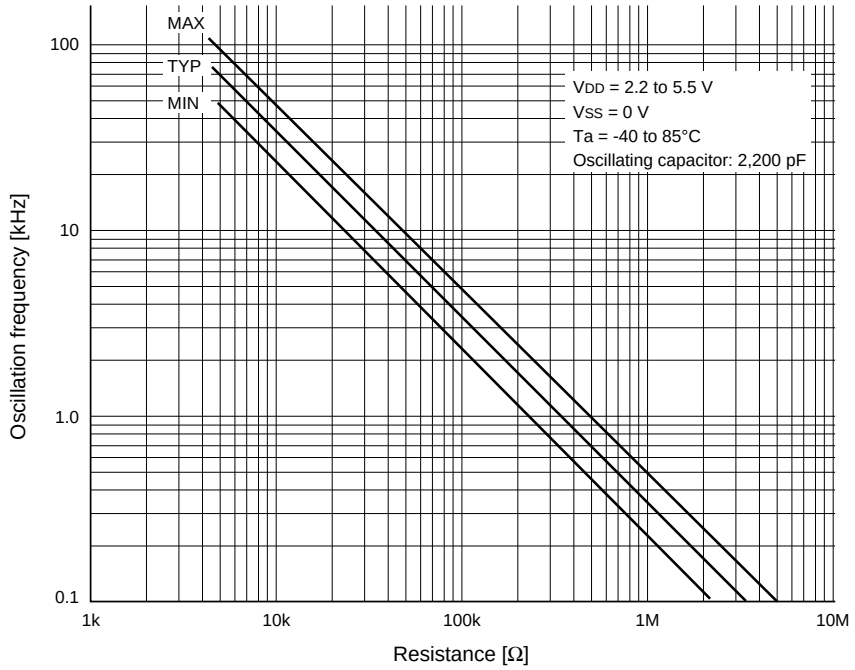


Fig. 7.7.2 Resistance-oscillation frequency curve (REF)

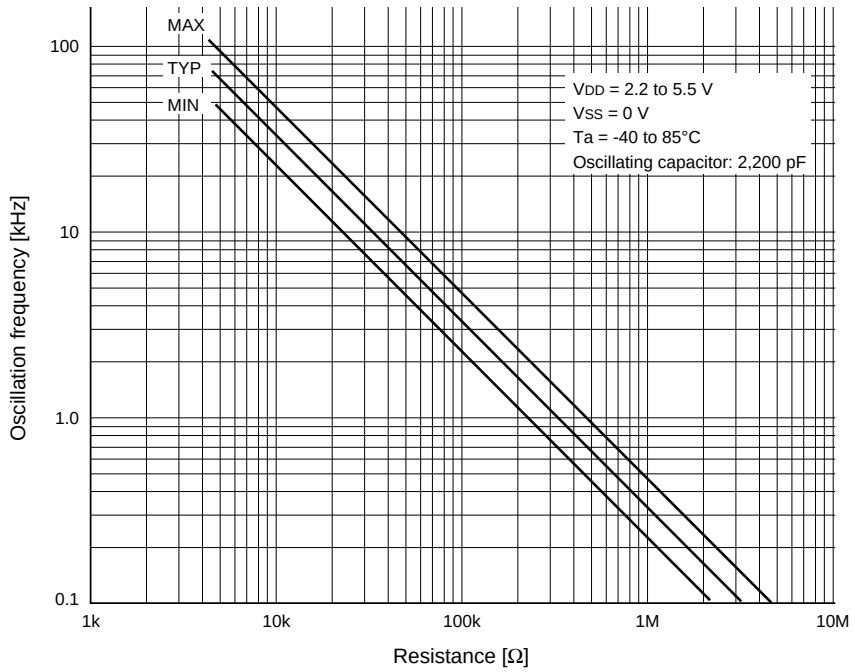


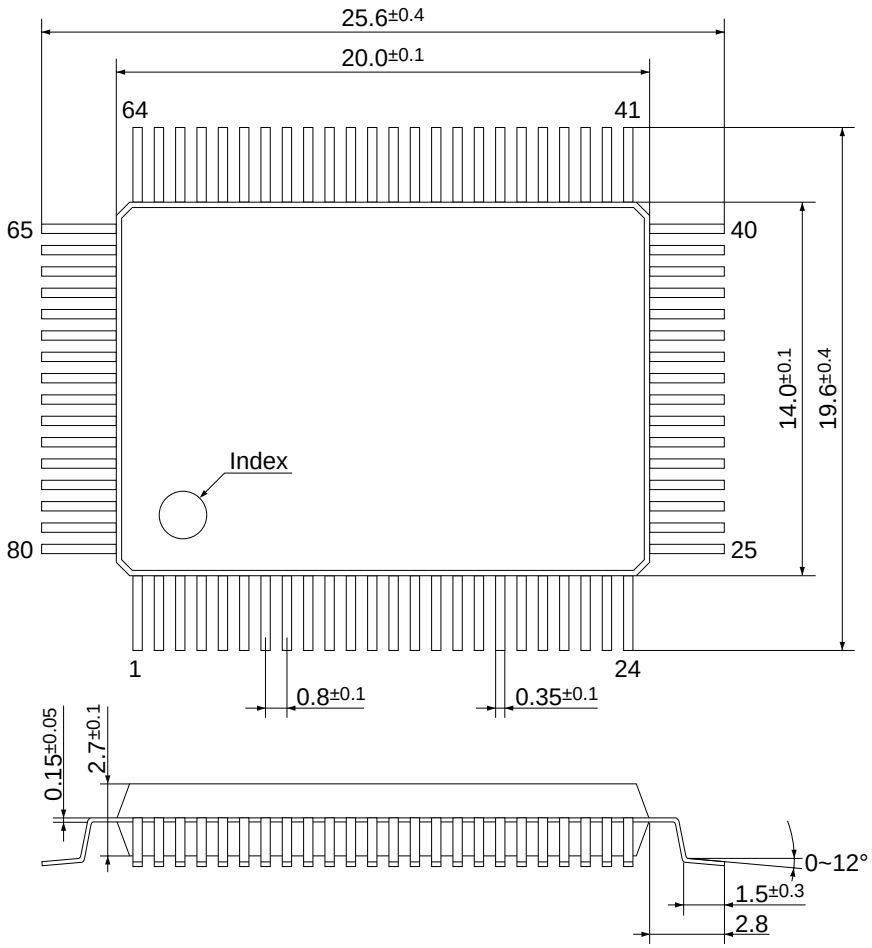
Fig. 7.7.3 Resistance-oscillation frequency curve (SEN0, SEN1)

CHAPTER 8 PACKAGE

8.1 Plastic Package

QFP5-80pin

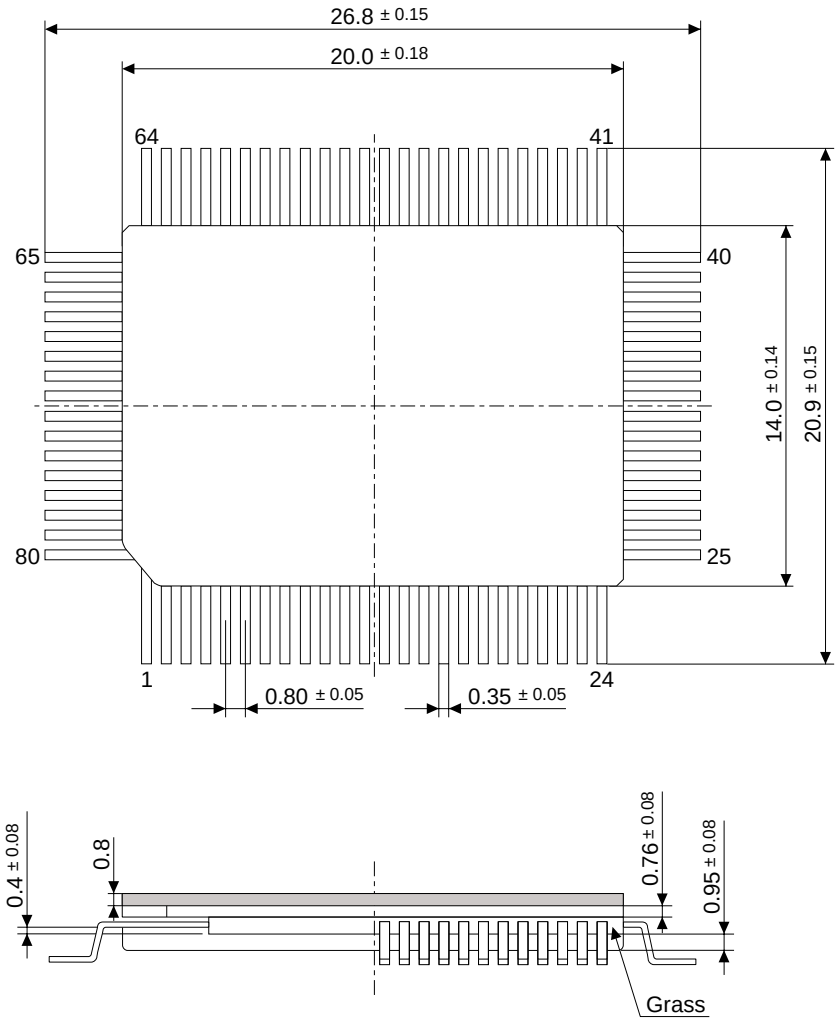
(Unit: mm)



8.2 Ceramic Package for Test Samples

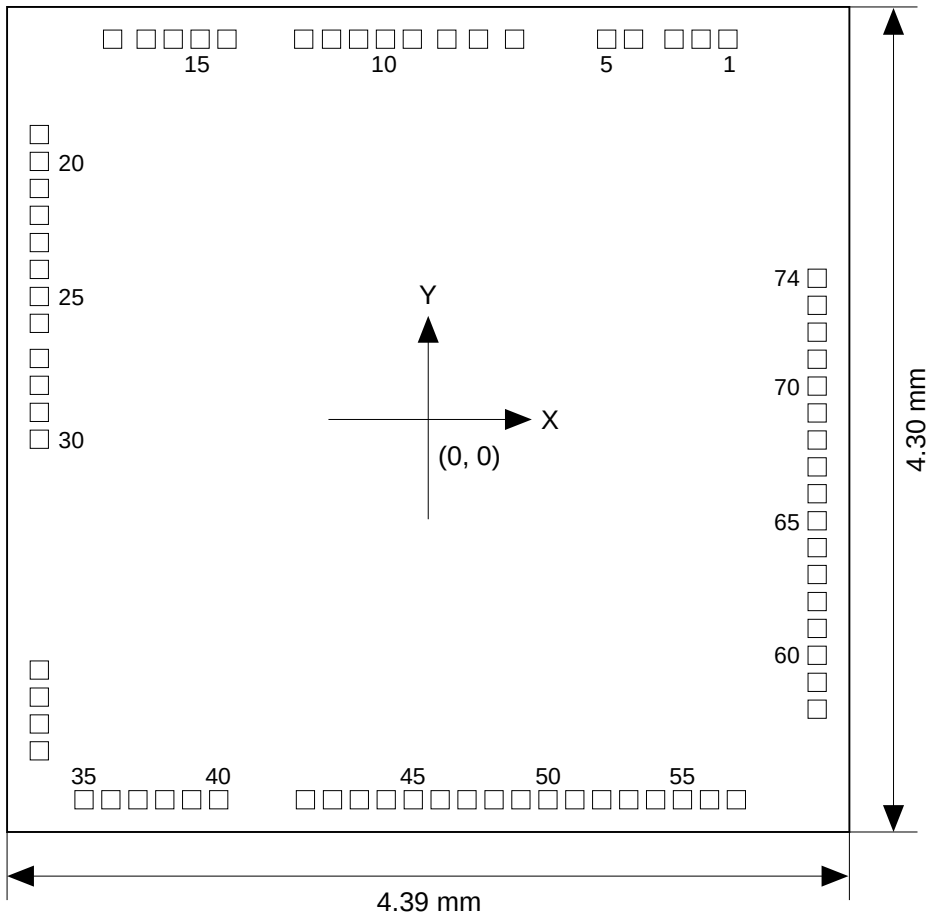
QFP5-80pin

(Unit: mm)



CHAPTER 9 PAD LAYOUT

9.1 Diagram of Pad Layout



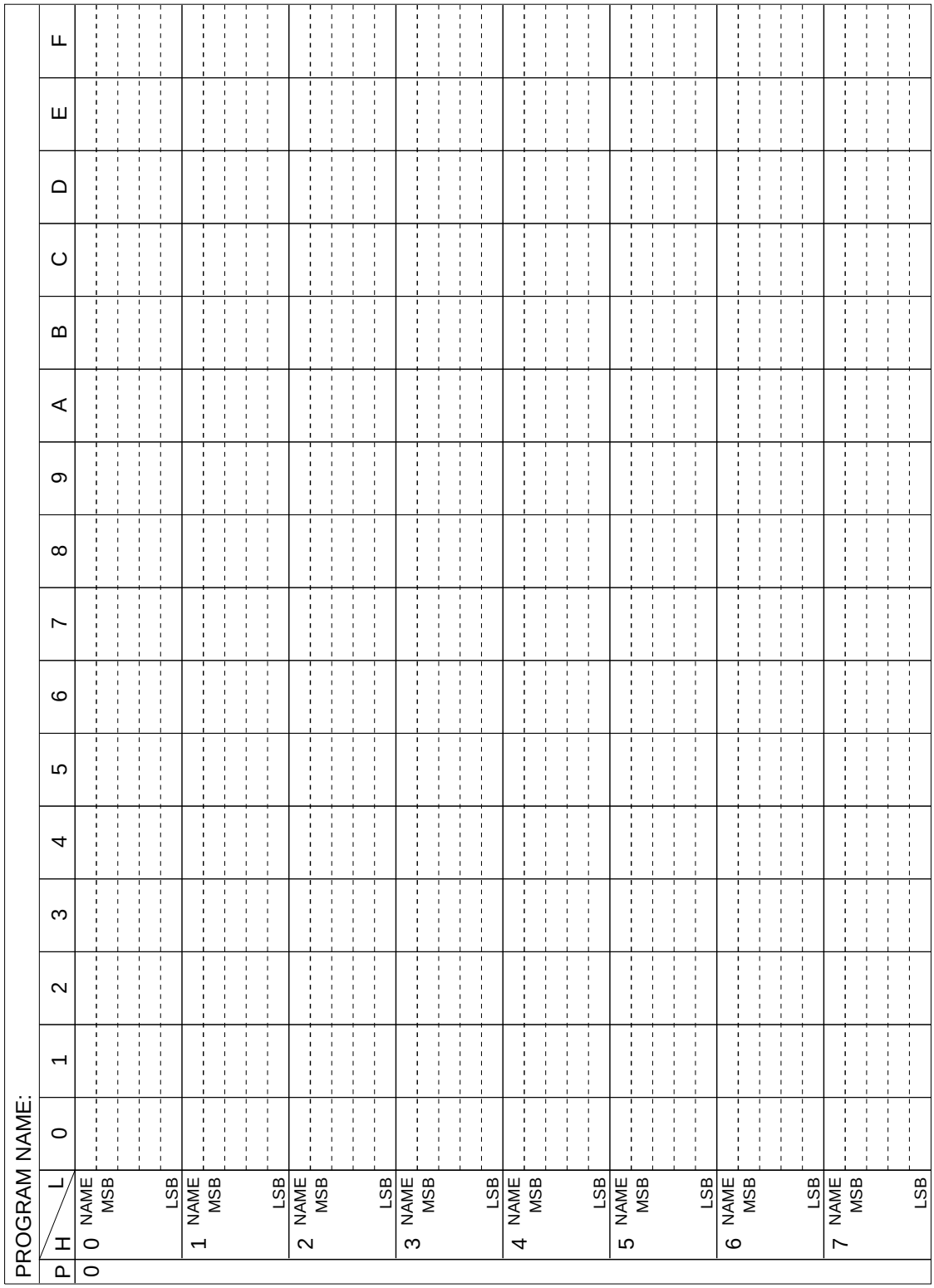
Chip thickness: 400 µm
Pad opening: 95 µm

9.2 Pad Coordinates

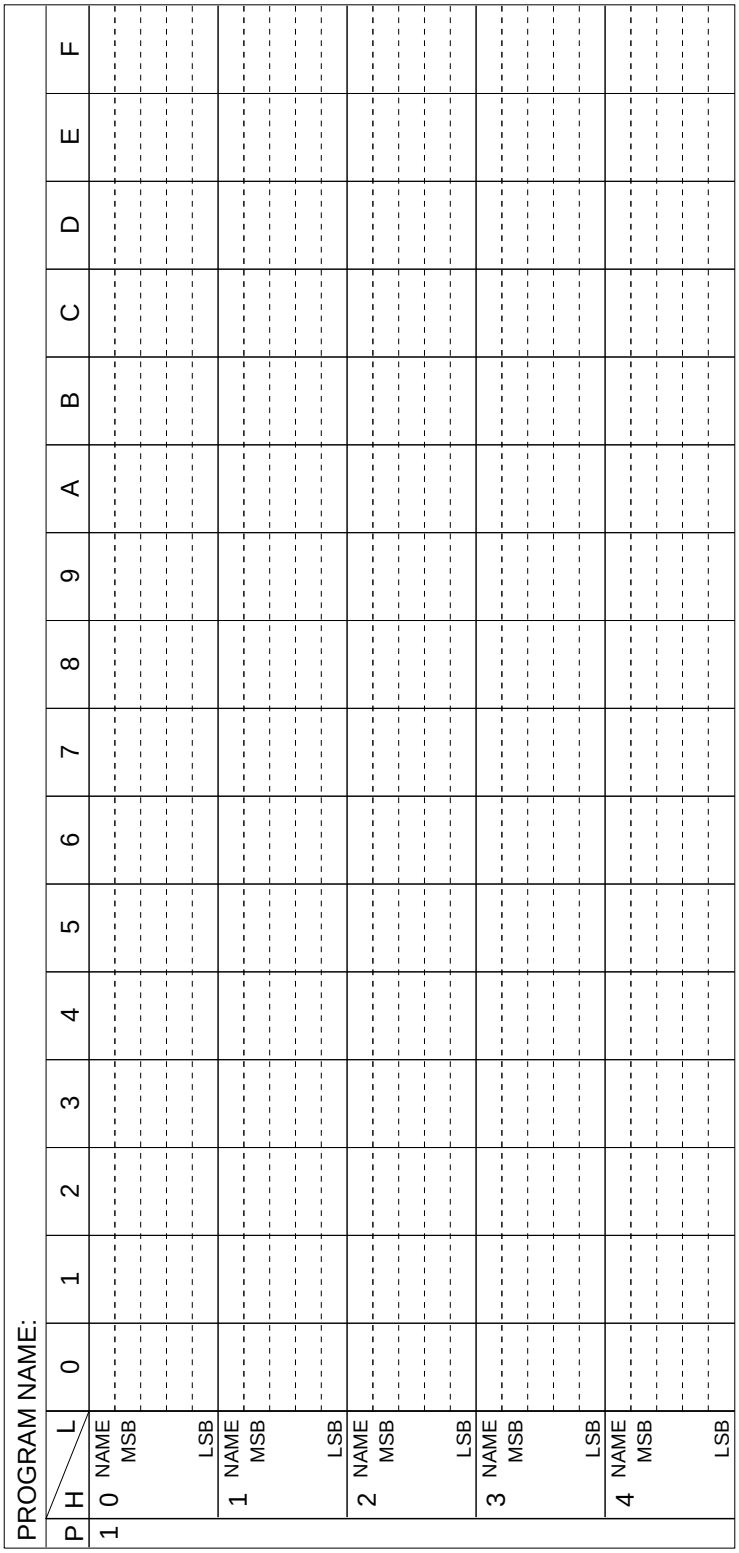
Pad		Coordinate		Pad		Coordinate	
No.	Name	X [mm]	Y [mm]	No.	Name	X [mm]	Y [mm]
1	REF	1.562	1.982	38	COM1	-1.373	-1.982
2	SEN0	1.422	1.982	39	COM2	-1.233	-1.982
3	SEN1	1.281	1.982	40	COM3	-1.092	-1.982
4	RFIN	1.070	1.982	41	SEG0	-0.640	-1.982
5	RFOUT	0.930	1.982	42	SEG1	-0.499	-1.982
6	V_{SS}	0.450	1.982	43	SEG2	-0.359	-1.982
7	OSC1	0.262	1.982	44	SEG3	-0.219	-1.982
8	OSC2	0.097	1.982	45	SEG4	-0.078	-1.982
9	V_{D1}	-0.083	1.982	46	SEG5	0.062	-1.982
10	OSC3	-0.223	1.982	47	SEG6	0.202	-1.982
11	OSC4	-0.363	1.982	48	SEG7	0.343	-1.982
12	V_{DD}	-0.504	1.982	49	SEG8	0.483	-1.982
13	$\overline{\text{RESET}}$	-0.649	1.982	50	SEG9	0.624	-1.982
14	R03	-1.049	1.982	51	SEG10	0.764	-1.982
15	R02	-1.189	1.982	52	SEG11	0.904	-1.982
16	R01	-1.329	1.982	53	SEG12	1.045	-1.982
17	R00	-1.470	1.982	54	SEG13	1.185	-1.982
18	$\overline{\text{TEST}}$	-1.645	1.982	55	SEG14	1.325	-1.982
19	K13	-2.027	1.485	56	SEG15	1.466	-1.982
20	K12	-2.027	1.345	57	SEG16	1.606	-1.982
21	K11	-2.027	1.204	58	SEG17	2.027	-1.510
22	K10	-2.027	1.064	59	SEG18	2.027	-1.370
23	K03	-2.027	0.922	60	SEG19	2.027	-1.229
24	K02	-2.027	0.782	61	SEG20	2.027	-1.089
25	K01	-2.027	0.641	62	SEG21	2.027	-0.949
26	K00	-2.027	0.501	63	SEG22	2.027	-0.808
27	P03	-2.027	0.318	64	SEG23	2.027	-0.668
28	P02	-2.027	0.178	65	SEG24	2.027	-0.528
29	P01	-2.027	0.037	66	SEG25	2.027	-0.387
30	P00	-2.027	-0.103	67	SEG26	2.027	-0.247
31	V_{ADJ}	-2.027	-1.306	68	SEG27	2.027	-0.107
32	V_{C1}	-2.027	-1.447	69	SEG28	2.027	0.034
33	V_{C2}	-2.027	-1.587	70	SEG29	2.027	0.174
34	V_{C3}	-2.027	-1.727	71	SEG30	2.027	0.314
35	CA	-1.794	-1.982	72	SEG31	2.027	0.455
36	CB	-1.654	-1.982	73	SEG32	2.027	0.595
37	COM0	-1.513	-1.982	74	SEG33	2.027	0.736

APPENDIX A. S1C621C0 RAM MAP

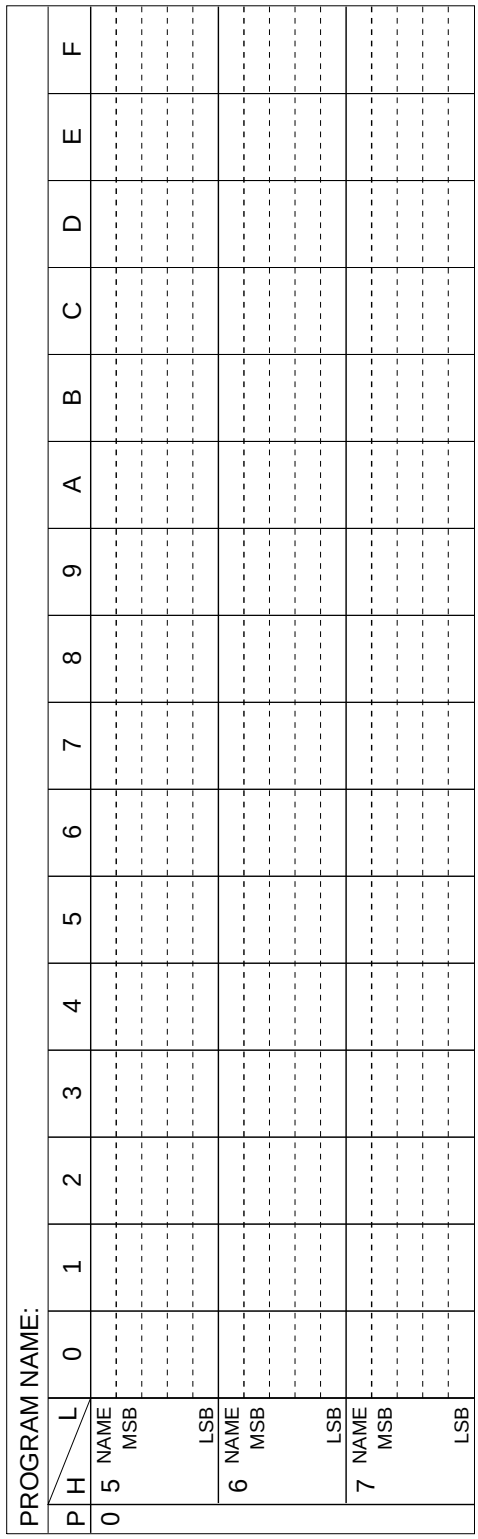
RAM map - 1 (000H–07FH)



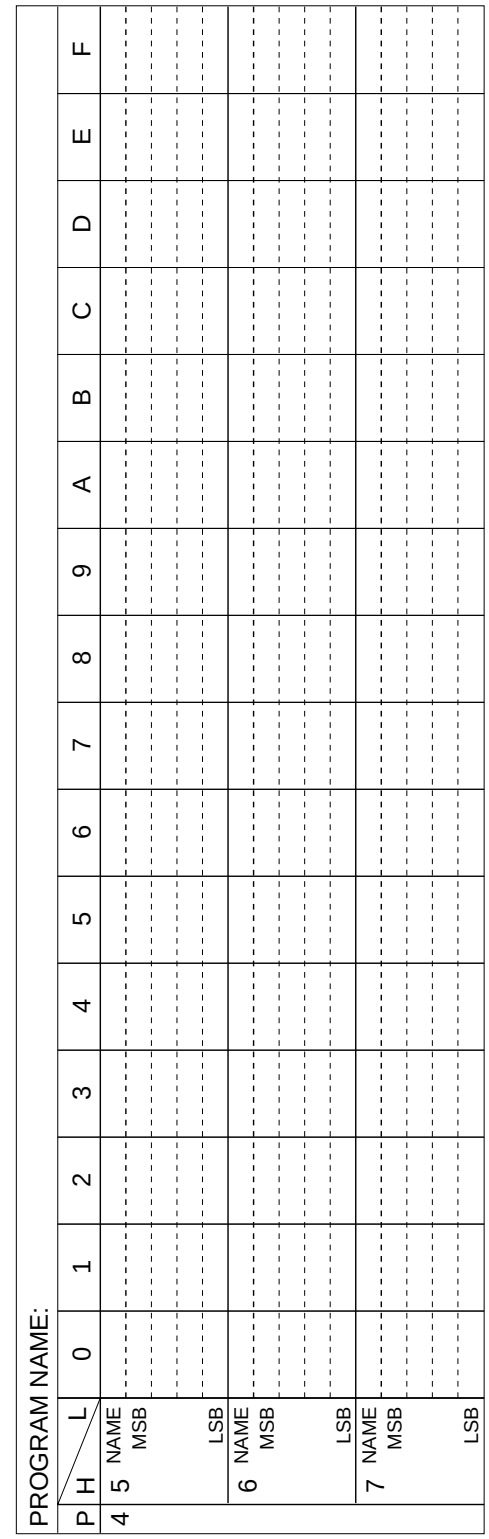
RAM map - 2 (100H–14FH)



Display memory map - 1 (050H–07FH, R/W)



Display memory map -2 (450H–47FH, W only)



I/O memory map (80H–FCH)

PROGRAM NAME:

P	H \ L		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	8	NAME																
		MSB	0	0														
1			0	0														
			SVDDT	CLKCHG														
2		LSB	SVDON	OSCC														
3	9	NAME																
		MSB	SIK03	K03	KCP03		SIK13	K13	KCP13									
4			SIK02	K02	KCP02		SIK12	K12	KCP12									
			SIK01	K01	KCP01		SIK11	K11	KCP11									
		LSB	SIK00	K00	KCP00		SIK10	K10	KCP10									
	A	NAME																
		MSB	R03															
			R02															
			R01															
		LSB	R00															
	B	NAME																
		MSB	IOC03	PUL03	P03													
			IOC02	PUL02	P02													
			IOC01	PUL01	P01													
		LSB	IOC00	PUL00	P00													
	C	NAME																
		MSB	LDMS	0			BZE	FOUTE	0		0	TM3	TM7					
			STCD	0			0	0	0		0	TM2	TM6					
			LDTY1	LOFF			0	FOFQ1	0		TMRUN	TM1	TM5					
		LSB	LDTY0	LPWR			BZFQ	FOFQ0	WDRST		TMRST	TM0	TM4					
	D	NAME																
		MSB	DBGOS	0	OVTBC	MC03	MC07	MC11	MC15									
			RFDBG	0	OVMC	MC02	MC06	MC10	MC14									
			RFCLK	0	RFRUN	MC01	MC05	MC09	MC13									
		LSB	RFPWR	SENS0	0	MC00	MC04	MC08	MC12									
	E	NAME																
		MSB	0	RCDIV	RIC3	ROUT3												
			REMSO	RCDTY	RIC2	ROUT2												
			REMDC	RT1	RIC1	ROUT1												
		LSB	REMCR	RT0	RIC0	ROUT0												
	F	NAME																
		MSB	0	0	0	0	0				0	0	0	0	0			
			0	0	0	0	EIT2				0	0	0	0	IT2			
			0	0	0	0	EIT1				0	0	0	0	IT1			
		LSB	EIREM	EIRF	EIK1	EIK0	EIT0				IREM	IRF	IK1	IK0	IT0			

Unused area

APPENDIX B. S1C621C0 INSTRUCTION SET

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Branch instructions	PSET	p	1	1	1	0	0	1	0	p4	p3	p2	p1	p0					5	NBP ← p4, NPP ← p3~p0
	JP	s	0	0	0	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0
		C, s	0	0	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=1
		NC, s	0	0	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=0
		Z, s	0	1	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=1
		NZ, s	0	1	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=0
	JPBA		1	1	1	1	1	1	1	0	1	0	0	0					5	PCB ← NBP, PCP ← NPP, PCSH ← B, PCSL ← A
	CALL	s	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← NPP, PCS ← s7~s0
	CALZ	s	0	1	0	1	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← 0, PCS ← s7~s0
	RET		1	1	1	1	1	1	0	1	1	1	1	1					7	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3
	RETS		1	1	1	1	1	1	0	1	1	1	1	0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, PC ← PC+1
	RETD	*I*	0	0	0	1	*I*7	*I*6	*I*5	*I*4	*I*3	*I*2	*I*1	*I*0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, M(X) ← *I*3~*I*0, M(X+1) ← *I*7~*I*4, X ← X+2
System control instructions	NOP5		1	1	1	1	1	1	1	1	1	0	1	1					5	No operation (5 clock cycles)
	NOP7		1	1	1	1	1	1	1	1	1	1	1	1					7	No operation (7 clock cycles)
	HALT		1	1	1	1	1	1	1	1	1	0	0	0					5	Halt (stop clock)
Index operation instructions	INC	X	1	1	1	0	1	1	1	0	0	0	0	0					5	X ← X+1
		Y	1	1	1	0	1	1	1	1	0	0	0	0					5	Y ← Y+1
	LD	X, x	1	0	1	1	x7	x6	x5	x4	x3	x2	x1	x0					5	XH ← x7~x4, XL ← x3~x0
		Y, y	1	0	0	0	y7	y6	y5	y4	y3	y2	y1	y0					5	YH ← y7~y4, YL ← y3~y0
		XP, r	1	1	1	0	1	0	0	0	0	0	r1	r0					5	XP ← r
		XH, r	1	1	1	0	1	0	0	0	0	1	r1	r0					5	XH ← r
		XL, r	1	1	1	0	1	0	0	0	1	0	r1	r0					5	XL ← r
		YP, r	1	1	1	0	1	0	0	1	0	0	r1	r0					5	YP ← r
		YH, r	1	1	1	0	1	0	0	1	0	1	r1	r0					5	YH ← r
		YL, r	1	1	1	0	1	0	0	1	1	0	r1	r0					5	YL ← r
		r, XP	1	1	1	0	1	0	1	0	0	0	r1	r0					5	r ← XP
		r, XH	1	1	1	0	1	0	1	0	0	1	r1	r0					5	r ← XH
		r, XL	1	1	1	0	1	0	1	0	1	0	r1	r0					5	r ← XL
		r, YP	1	1	1	0	1	0	1	1	0	0	r1	r0					5	r ← YP
		r, YH	1	1	1	0	1	0	1	1	0	1	r1	r0					5	r ← YH
		r, YL	1	1	1	0	1	0	1	1	1	0	r1	r0					5	r ← YL
	ADC	XH, i	1	0	1	0	0	0	0	0	i3	i2	i1	i0			↕	↕	7	XH ← XH+i3~i0+C
		XL, i	1	0	1	0	0	0	0	1	i3	i2	i1	i0			↕	↕	7	XL ← XL+i3~i0+C
		YH, i	1	0	1	0	0	0	1	0	i3	i2	i1	i0			↕	↕	7	YH ← YH+i3~i0+C
		YL, i	1	0	1	0	0	0	1	1	i3	i2	i1	i0			↕	↕	7	YL ← YL+i3~i0+C

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Index operation instructions	CP	XH, i	1	0	1	0	0	1	0	0	i3	i2	i1	i0			↕	↕	7	XH-i3~i0
		XL, i	1	0	1	0	0	1	0	1	i3	i2	i1	i0			↕	↕	7	XL-i3~i0
		YH, i	1	0	1	0	0	1	1	0	i3	i2	i1	i0			↕	↕	7	YH-i3~i0
		YL, i	1	0	1	0	0	1	1	1	i3	i2	i1	i0			↕	↕	7	YL-i3~i0
Data transfer instructions	LD	r, i	1	1	1	0	0	0	r1	r0	i3	i2	i1	i0					5	r ← i3~i0
		r, q	1	1	1	0	1	1	0	0	r1	r0	q1	q0					5	r ← q
		A, Mn	1	1	1	1	1	0	1	0	n3	n2	n1	n0					5	A ← M(n3~n0)
		B, Mn	1	1	1	1	1	0	1	1	n3	n2	n1	n0					5	B ← M(n3~n0)
		Mn, A	1	1	1	1	1	0	0	0	n3	n2	n1	n0					5	M(n3~n0) ← A
		Mn, B	1	1	1	1	1	0	0	1	n3	n2	n1	n0					5	M(n3~n0) ← B
	LDPX	MX, i	1	1	1	0	0	1	1	0	i3	i2	i1	i0					5	M(X) ← i3~i0, X ← X+1
		r, q	1	1	1	0	1	1	1	0	r1	r0	q1	q0					5	r ← q, X ← X+1
	LDPY	MY, i	1	1	1	0	0	1	1	1	i3	i2	i1	i0					5	M(Y) ← i3~i0, Y ← Y+1
		r, q	1	1	1	0	1	1	1	1	r1	r0	q1	q0					5	r ← q, Y ← Y+1
	LBPX	MX, *l*	1	0	0	1	*l*7	*l*6	*l*5	*l*4	*l*3	*l*2	*l*1	*l*0					5	M(X) ← *l*3~*l*0, M(X+1) ← *l*7~*l*4, X ← X+2
Flag operation instructions	SET	F, i	1	1	1	1	0	1	0	0	i3	i2	i1	i0	↑	↑	↑	↑	7	F ← F∨i3~i0
	RST	F, i	1	1	1	1	0	1	0	1	i3	i2	i1	i0	↓	↓	↓	↓	7	F ← F∧i3~i0
	SCF		1	1	1	1	0	1	0	0	0	0	0	1				↑	7	C ← 1
	RCF		1	1	1	1	0	1	0	1	1	1	1	0				↓	7	C ← 0
	SZF		1	1	1	1	0	1	0	0	0	0	1	0			↑		7	Z ← 1
	RZF		1	1	1	1	0	1	0	1	1	1	0	1			↓		7	Z ← 0
	SDF		1	1	1	1	0	1	0	0	0	1	0	0		↑			7	D ← 1 (Decimal Adjuster ON)
	RDF		1	1	1	1	0	1	0	1	1	0	1	1		↓			7	D ← 0 (Decimal Adjuster OFF)
	EI		1	1	1	1	0	1	0	0	1	0	0	0	↑				7	I ← 1 (Enables Interrupt)
	DI		1	1	1	1	0	1	0	1	0	1	1	1	↓				7	I ← 0 (Disables Interrupt)
Stack operation instructions	INC	SP	1	1	1	1	1	1	0	1	1	0	1	1					5	SP ← SP+1
	DEC	SP	1	1	1	1	1	1	0	0	1	0	1	1					5	SP ← SP-1
	PUSH	r	1	1	1	1	1	1	0	0	0	0	r1	r0					5	SP ← SP-1, M(SP) ← r
		XP	1	1	1	1	1	1	0	0	0	1	0	0					5	SP ← SP-1, M(SP) ← XP
		XH	1	1	1	1	1	1	0	0	0	1	0	1					5	SP ← SP-1, M(SP) ← XH
		XL	1	1	1	1	1	1	0	0	0	1	1	0					5	SP ← SP-1, M(SP) ← XL
		YP	1	1	1	1	1	1	0	0	0	1	1	1					5	SP ← SP-1, M(SP) ← YP
		YH	1	1	1	1	1	1	0	0	1	0	0	0					5	SP ← SP-1, M(SP) ← YH
		YL	1	1	1	1	1	1	0	0	1	0	0	1					5	SP ← SP-1, M(SP) ← YL
		F	1	1	1	1	1	1	0	0	1	0	1	0					5	SP ← SP-1, M(SP) ← F
	POP	r	1	1	1	1	1	1	0	1	0	0	r1	r0					5	r ← M(SP), SP ← SP+1
		XP	1	1	1	1	1	1	0	1	0	1	0	0					5	XP ← M(SP), SP ← SP+1
		XH	1	1	1	1	1	1	0	1	0	1	0	1					5	XH ← M(SP), SP ← SP+1
		XL	1	1	1	1	1	1	0	1	0	1	1	0					5	XL ← M(SP), SP ← SP+1
		YP	1	1	1	1	1	1	0	1	0	1	1	1					5	YP ← M(SP), SP ← SP+1

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Stack operation instructions	POP	YH	1	1	1	1	1	1	0	1	1	0	0	0					5	YH← M(SP), SP← SP+1
		YL	1	1	1	1	1	1	0	1	1	0	0	1					5	YL← M(SP), SP← SP+1
		F	1	1	1	1	1	1	0	1	1	0	1	0	↕	↕	↕	↕	5	F← M(SP), SP← SP+1
	LD	SPH, r	1	1	1	1	1	1	1	0	0	0	r1	r0					5	SPH← r
		SPL, r	1	1	1	1	1	1	1	1	0	0	r1	r0					5	SPL ← r
		r, SPH	1	1	1	1	1	1	1	0	0	1	r1	r0					5	r← SPH
		r, SPL	1	1	1	1	1	1	1	1	0	1	r1	r0					5	r← SPL
Arithmetic instructions	ADD	r, i	1	1	0	0	0	0	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r+i3~i0
		r, q	1	0	1	0	1	0	0	0	r1	r0	q1	q0	★	↕	↕		7	r← r+q
	ADC	r, i	1	1	0	0	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r+i3~i0+C
		r, q	1	0	1	0	1	0	0	1	r1	r0	q1	q0	★	↕	↕		7	r← r+q+C
	SUB	r, q	1	0	1	0	1	0	1	0	r1	r0	q1	q0	★	↕	↕		7	r← r-q
	SBC	r, i	1	1	0	1	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r-i3~i0-C
		r, q	1	0	1	0	1	0	1	1	r1	r0	q1	q0	★	↕	↕		7	r← r-q-C
	AND	r, i	1	1	0	0	1	0	r1	r0	i3	i2	i1	i0		↕			7	r← r∧ i3~i0
		r, q	1	0	1	0	1	1	0	0	r1	r0	q1	q0		↕			7	r← r∧ q
	OR	r, i	1	1	0	0	1	1	r1	r0	i3	i2	i1	i0		↕			7	r← r∨i3~i0
		r, q	1	0	1	0	1	1	0	1	r1	r0	q1	q0		↕			7	r← r∨q
	XOR	r, i	1	1	0	1	0	0	r1	r0	i3	i2	i1	i0		↕			7	r← r∀i3~i0
		r, q	1	0	1	0	1	1	1	0	r1	r0	q1	q0		↕			7	r← r∀q
	CP	r, i	1	1	0	1	1	1	r1	r0	i3	i2	i1	i0		↕	↕		7	r-i3~i0
		r, q	1	1	1	1	0	0	0	0	r1	r0	q1	q0		↕	↕		7	r-q
	FAN	r, i	1	1	0	1	1	0	r1	r0	i3	i2	i1	i0		↕			7	r∧i3~i0
		r, q	1	1	1	1	0	0	0	1	r1	r0	q1	q0		↕			7	r∧q
	RLC	r	1	0	1	0	1	1	1	1	r1	r0	r1	r0		↕	↕		7	d3←d2, d2←d1, d1←d0, d0←C, C← d3
	RRC	r	1	1	1	0	1	0	0	0	1	1	r1	r0		↕	↕		5	d3←C, d2←d3, d1←d2, d0←d1, C← d0
	INC	Mn	1	1	1	1	0	1	1	0	n3	n2	n1	n0		↕	↕		7	M(n3~n0)←M(n3~n0)+1
	DEC	Mn	1	1	1	1	0	1	1	1	n3	n2	n1	n0		↕	↕		7	M(n3~n0)←M(n3~n0)-1
	ACPX	MX, r	1	1	1	1	0	0	1	0	1	0	r1	r0	★	↕	↕		7	M(X)←M(X)+r+C, X←X+1
	ACPY	MY, r	1	1	1	1	0	0	1	0	1	1	r1	r0	★	↕	↕		7	M(Y)←M(Y)+r+C, Y←Y+1
	SCPX	MX, r	1	1	1	1	0	0	1	1	1	0	r1	r0	★	↕	↕		7	M(X)←M(X)-r-C, X←X+1
	SCPY	MY, r	1	1	1	1	0	0	1	1	1	1	r1	r0	★	↕	↕		7	M(Y)←M(Y)-r-C, Y←Y+1
	NOT	r	1	1	0	1	0	0	r1	r0	1	1	1	1		↕			7	r←$\overline{r}$

Abbreviations used in the explanations have the following meanings.

Symbols associated with registers and memory

A A register
B B register
X XHL register
(low order eight bits of index register IX)
Y YHL register
(low order eight bits of index register IY)
XH XH register
(high order four bits of XHL register)
XL XL register
(low order four bits of XHL register)
YH YH register
(high order four bits of YHL register)
YL YL register
(low order four bits of YHL register)
XP XP register
(high order four bits of index register IX)
YP YP register
(high order four bits of index register IY)
SP Stack pointer SP
SPH High-order four bits of stack pointer SP
SPL Low-order four bits of stack pointer SP
MX, M(X) Data memory whose address is specified with index register IX
MY, M(Y) Data memory whose address is specified with index register IY
Mn, M(n) Data memory address 000H–00FH (address specified with immediate data n of 00H–0FH)
M(SP) Data memory whose address is specified with stack pointer SP
r, q Two-bit register code
r, q is two-bit immediate data; according to the contents of these bits, they indicate registers A, B, and MX and MY (data memory whose addresses are specified with index registers IX and IY)

r		q		Register specified
r1	r0	q1	q0	
0	0	0	0	A
0	1	0	1	B
1	0	1	0	MX
1	1	1	1	MY

Symbols associated with program counter

NBP New bank pointer
NPP New page pointer
PCB Program counter bank
PCP Program counter page
PCS Program counter step
PCSH Four high order bits of PCS
PCSL Four low order bits of PCS

Symbols associated with flags

F Flag register (I, D, Z, C)
C Carry flag
Z Zero flag
D Decimal flag
I Interrupt flag
↓ Flag reset
↑ Flag set
↕ Flag set or reset

Associated with immediate data

p Five-bit immediate data or label 00H–1FH
s Eight-bit immediate data or label 00H–0FFH
l Eight-bit immediate data 00H–0FFH
i Four-bit immediate data 00H–0FH

Associated with arithmetic and other operations

+ Add
- Subtract
∧ Logical AND
∨ Logical OR
∀ Exclusive-OR
★ Add-subtract instruction for decimal operation when the D flag is set

APPENDIX C. PSEUDO-INSTRUCTION TABLE OF THE CROSS ASSEMBLER

Item No.	Pseudo-instruction	Meaning	Example of use
1	EQU (Equation)	To allocate data to label	`ABC EQU 9` `BCD EQU ABC+1`
2	ORG (Origin)	To define location counter	`ORG 100H` `ORG 256`
3	SET (Set)	To allocate data to label (data can be changed)	`ABC SET 0001H` `ABC SET 0002H`
4	DW (Define Word)	To define ROM data	`ABC DW 'AB'` `BCD DW 0FFBH`
5	PAGE (Page)	To define boundary of page	`PAGE 1H` `PAGE 4`
6	SECTION (Section)	To define boundary of section	`SECTION`
7	END (End)	To terminate assembly	`END`

8	MACRO
	(Macro)
		To define macro	`CHECK MACRO DATA`
			`LOCAL LOOP`
			`LOOP CP MX,DATA`
			`JP NZ,LOOP`
			`ENDM`
			
			`CHECK 1`

9	LOCAL (Local)	To make local specification of label during macro definition	
10	ENDM (End Macro)	To end macro definition	

APPENDIX D. COMMAND TABLE OF ICE

Item No.	Function	Command Format	Outline of Operation
1	Assemble	#A,a ↵	Assemble command mnemonic code and store at address "a"
2	Disassemble	#L,a1,a2 ↵	Contents of addresses a1 to a2 are disassembled and displayed
3	Dump	#DP,a1,a2 ↵	Contents of program area a1 to a2 are displayed
		#DD,a1,a2 ↵	Content of data area a1 to a2 are displayed
4	Fill	#FP,a1,a2,d ↵	Data d is set in addresses a1 to a2 (program area)
		#FD,a1,a2,d ↵	Data d is set in addresses a1 to a2 (data area)
5	Set Run Mode	#G,a ↵	Program is executed from the "a" address
		#TIM ↵	Execution time and step counter selection
		#OTF ↵	On-the-fly display selection
6	Trace	#T,a,n ↵	Executes program while displaying results of step instruction from "a" address
		#U,a,n ↵	Displays only the final step of #T,a,n
7	Break	#BA,a ↵	Sets Break at program address "a"
		#BAR,a ↵	Breakpoint is canceled
		#BD ↵	Break condition is set for data RAM
		#BDR ↵	Breakpoint is canceled
		#BR ↵	Break condition is set for Evaluation Board CPU internal registers
		#BRR ↵	Breakpoint is canceled
		#BM ↵	Combined break conditions set for program data RAM address and registers
		#BMR ↵	Cancel combined break conditions for program data ROM address and registers
		#BRES ↵	All break conditions canceled
		#BC ↵	Break condition displayed
		#BE ↵	Enter break enable mode
		#BSYN ↵	Enter break disable mode
		#BT ↵	Set break stop/trace modes
		#BRKSEL,REM ↵	Set BA condition clear/remain modes
8	Move	#MP,a1,a2,a3 ↵	Contents of program area addresses a1 to a2 are moved to addresses a3 and after
		#MD,a1,a2,a3 ↵	Contents of data area addresses a1 to a2 are moved to addresses a3 and after
9	Data Set	#SP,a ↵	Data from program area address "a" are written to memory
		#SD,a ↵	Data from data area address "a" are written to memory
10	Change CPU Internal Registers	#DR ↵	Display Evaluation Board CPU internal registers
		#SR ↵	Set Evaluation Board CPU internal registers
		#I ↵	Reset Evaluation Board CPU
		#DXY ↵	Display X, Y, MX and MY
		#SXY ↵	Set data for X and Y display and MX, MY

Item No.	Function	Command Format	Outline of Operation
11	History	#H,p1,p2 ↵	Display history data for pointer 1 and pointer 2
		#HB ↵	Display upstream history data
		#HG ↵	Display 21 line history data
		#HP ↵	Display history pointer
		#HPS,a ↵	Set history pointer
		#HC,S/C/E ↵	Sets up the history information acquisition before (S), before/after (C) and after (E)
		#HA,a1,a2 ↵	Sets up the history information acquisition from program area a1 to a2
		#HAR,a1,a2 ↵	Sets up the prohibition of the history information acquisition from program area a1 to a2
		#HAD ↵	Indicates history acquisition program area
		#HS,a ↵	Retrieves and indicates the history information which executed a program address "a"
		#HSW,a ↵ #HSR,a ↵	Retrieves and indicates the history information which wrote or read the data area address "a"
12	File	#RF,file ↵	Move program file to memory
		#RFD,file ↵	Move data file to memory
		#VF,file ↵	Compare program file and contents of memory
		#VFD,file ↵	Compare data file and contents of memory
		#WF,file ↵	Save contents of memory to program file
		#WFD,file ↵	Save contents of memory to data file
		#CL,file ↵	Load ICE set condition from file
		#CS,file ↵	Save ICE set condition to file
		#OPTLD,1,file ↵ #OPTLD,2,file ↵	Load function option data from file Load segment option data from file
13	Coverage	#CVD ↵	Indicates coverage information
		#CVR ↵	Clears coverage information
14	ROM Access	#RP ↵	Move contents of ROM to program memory
		#VP ↵	Compare contents of ROM with contents of program memory
		#ROM ↵	Set ROM type
15	Terminate ICE	#Q ↵	Terminate ICE and return to operating system control
16	Command Display	#HELP ↵	Display ICE instruction
17	Self Diagnosis	#CHK ↵	Report results of ICE self diagnostic test

↵ means press the RETURN key.

EPSON International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.

- HEADQUARTERS -
1960 E. Grand Avenue
El Segundo, CA 90245, U.S.A.
Phone: +1-310-955-5300 Fax: +1-310-955-5400

- SALES OFFICES -

West
150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone: +1-408-922-0200 Fax: +1-408-922-0238

Central
101 Virginia Street, Suite 290
Crystal Lake, IL 60014, U.S.A.
Phone: +1-815-455-7630 Fax: +1-815-455-7633

Northeast
301 Edgewater Place, Suite 120
Wakefield, MA 01880, U.S.A.
Phone: +1-781-246-3600 Fax: +1-781-246-5443

Southeast
3010 Royal Blvd. South, Suite 170
Alpharetta, GA 30005, U.S.A.
Phone: +1-877-EEA-0020 Fax: +1-770-777-2637

EUROPE

EPSON EUROPE ELECTRONICS GmbH

- HEADQUARTERS -
Riesstrasse 15
80992 Munich, GERMANY
Phone: +49-(0)89-14005-0 Fax: +49-(0)89-14005-110

SALES OFFICE
Altstadtstrasse 176
51379 Leverkusen, GERMANY
Phone: +49-(0)2171-5045-0 Fax: +49-(0)2171-5045-10

UK BRANCH OFFICE
Unit 2.4, Doncastle House, Doncastle Road
Bracknell, Berkshire RG12 8PE, ENGLAND
Phone: +44-(0)1344-381700 Fax: +44-(0)1344-381701

FRENCH BRANCH OFFICE
1 Avenue de l' Atlantique, LP 915 Les Conquerants
Z.A. de Courtaboeuf 2, F-91976 Les Ulis Cedex, FRANCE
Phone: +33-(0)1-64862350 Fax: +33-(0)1-64862355

BARCELONA BRANCH OFFICE

Barcelona Design Center
Edificio Prima Sant Cugat
Avda. Alcalde Barrils num. 64-68
E-08190 Sant Cugat del Vallès, SPAIN
Phone: +34-93-544-2490 Fax: +34-93-544-2491

ASIA

EPSON (CHINA) CO., LTD.
28F, Beijing Silver Tower 2# North RD DongSanHuan
ChaoYang District, Beijing, CHINA
Phone: 64106655 Fax: 64107319

SHANGHAI BRANCH
4F, Bldg., 27, No. 69, Gui Jing Road
Caohejing, Shanghai, CHINA
Phone: 21-6485-5552 Fax: 21-6485-0775

EPSON HONG KONG LTD.
20/F., Harbour Centre, 25 Harbour Road
Wanchai, Hong Kong
Phone: +852-2585-4600 Fax: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
10F, No. 287, Nanking East Road, Sec. 3
Taipei
Phone: 02-2717-7360 Fax: 02-2712-9164
Telex: 24444 EPSONTB

HSINCHU OFFICE
13F-3, No. 295, Kuang-Fu Road, Sec. 2
HsinChu 300
Phone: 03-573-9900 Fax: 03-573-9169

EPSON SINGAPORE PTE., LTD.
No. 1 Temasek Avenue, #36-00
Millenia Tower, SINGAPORE 039192
Phone: +65-337-7911 Fax: +65-334-2716

SEIKO EPSON CORPORATION KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: 02-784-6027 Fax: 02-767-3677

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

Electronic Device Marketing Department
IC Marketing & Engineering Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5816 Fax: +81-(0)42-587-5624

ED International Marketing Department Europe & U.S.A.
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5812 Fax: +81-(0)42-587-5564

ED International Marketing Department Asia
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814 Fax: +81-(0)42-587-5110

In pursuit of **"Saving" Technology**, Epson electronic devices.
Our lineup of semiconductors, liquid crystal displays and quartz devices
assists in creating the products of our customers' dreams.
Epson IS energy savings.

S1C621C0
Technical Manual

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

■ EPSON Electronic Devices Website

http://www.epson.co.jp/device/

First issue January, 1995
Printed March, 2001 in Japan ⓂA