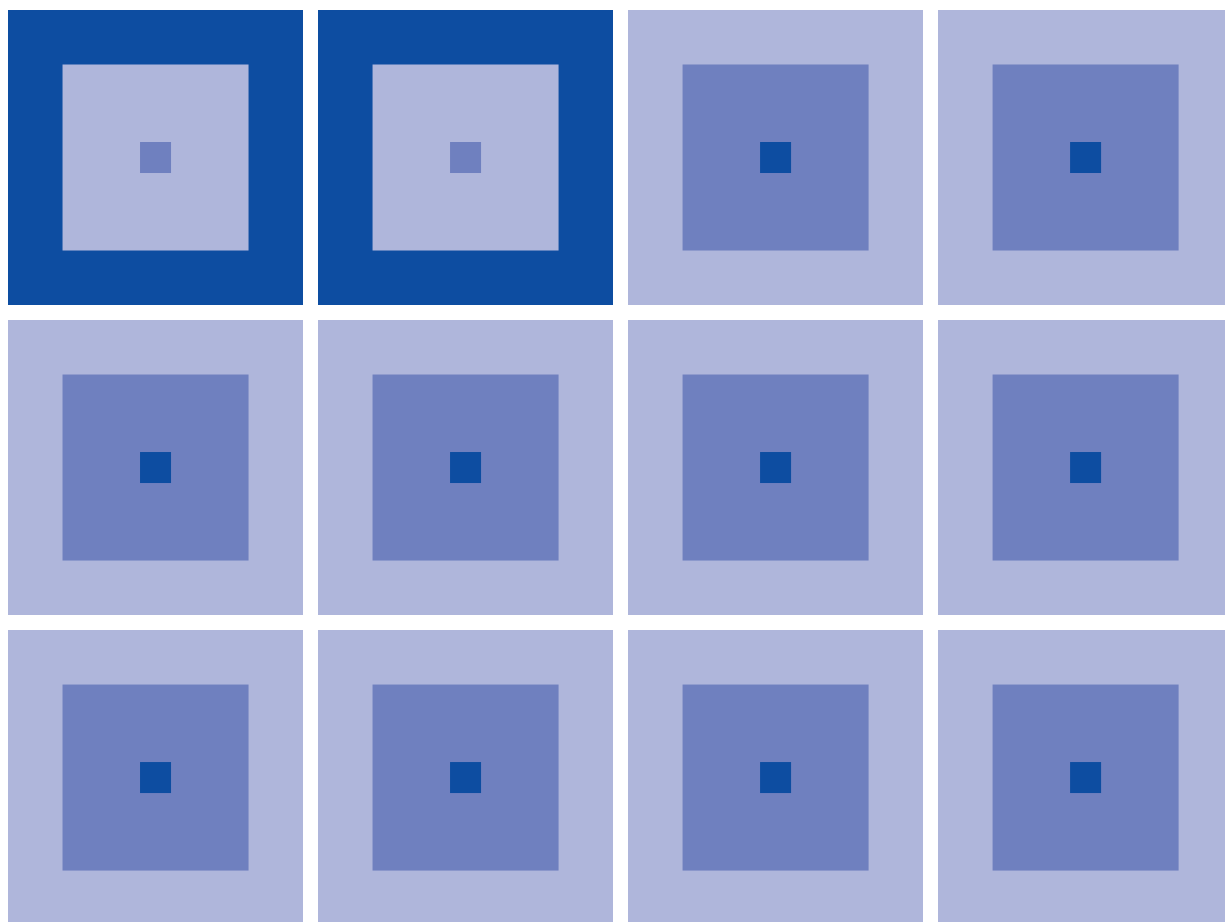


CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

S1C60N05

Technical Manual

S1C60N05 Technical Hardware



NOTICE

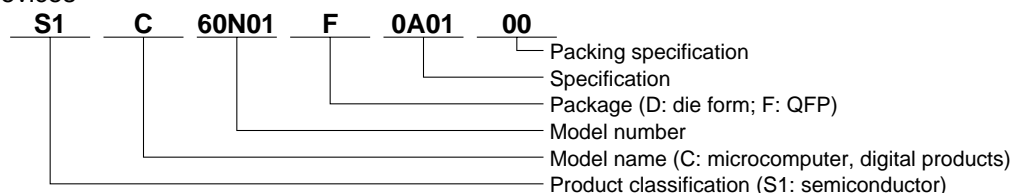
No part of this material may be reproduced or duplicated in any form or by any means without the written permission of Seiko Epson. Seiko Epson reserves the right to make changes to this material without notice. Seiko Epson does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit and, further, there is no representation that this material is applicable to products requiring high level reliability, such as medical products. Moreover, no license to any intellectual property rights is granted by implication or otherwise, and there is no representation or warranty that anything made in accordance with this material will be free from any patent or copyright infringement of a third party. This material or portions thereof may contain technology or the subject relating to strategic products under the control of the Foreign Exchange and Foreign Trade Law of Japan and may require an export license from the Ministry of International Trade and Industry or other approval from another government agency.

The information of the product number change

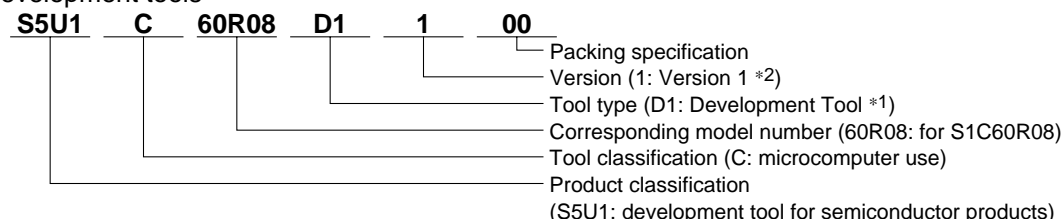
Starting April 1, 2001, the product number will be changed as listed below. To order from April 1, 2001 please use the new product number. For further information, please contact Epson sales representative.

Configuration of product number

Devices



Development tools



*1: For details about tool types, see the tables below. (In some manuals, tool types are represented by one digit.)

*2: Actual versions are not written in the manuals.

Comparison table between new and previous number

S1C60 Family processors

Previous No.	New No.
E0C6001	S1C60N01
E0C6002	S1C60N02
E0C6003	S1C60N03
E0C6004	S1C60N04
E0C6005	S1C60N05
E0C6006	S1C60N06
E0C6007	S1C60N07
E0C6008	S1C60N08
E0C6009	S1C60N09
E0C6011	S1C60N11
E0C6013	S1C60N13
E0C6014	S1C60140
E0C60R08	S1C60R08

S1C62 Family processors

Previous No.	New No.
E0C621A	S1C621A0
E0C6215	S1C62150
E0C621C	S1C621C0
E0C6S27	S1C6S2N7
E0C6S37	S1C6S3N7
E0C623A	S1C6N3A0
E0C623E	S1C6N3E0
E0C6S32	S1C6S3N2
E0C6233	S1C62N33
E0C6235	S1C62N35
E0C623B	S1C6N3B0
E0C6244	S1C62440
E0C624A	S1C624A0
E0C6S46	S1C6S460

Previous No.	New No.
E0C6247	S1C62470
E0C6248	S1C62480
E0C6S48	S1C6S480
E0C624C	S1C624C0
E0C6251	S1C62N51
E0C6256	S1C62560
E0C6292	S1C62920
E0C6262	S1C62N62
E0C6266	S1C62660
E0C6274	S1C62740
E0C6281	S1C62N81
E0C6282	S1C62N82
E0C62M2	S1C62M20
E0C62T3	S1C62T30

Comparison table between new and previous number of development tools

Development tools for the S1C60/62 Family

Previous No.	New No.
ASM62	S5U1C62000A
DEV6001	S5U1C60N01D
DEV6002	S5U1C60N02D
DEV6003	S5U1C60N03D
DEV6004	S5U1C60N04D
DEV6005	S5U1C60N05D
DEV6006	S5U1C60N06D
DEV6007	S5U1C60N07D
DEV6008	S5U1C60N08D
DEV6009	S5U1C60N09D
DEV6011	S5U1C60N11D
DEV60R08	S5U1C60R08D
DEV621A	S5U1C621A0D
DEV621C	S5U1C621C0D
DEV623B	S5U1C623B0D
DEV6244	S5U1C62440D
DEV624A	S5U1C624A0D
DEV624C	S5U1C624C0D
DEV6248	S5U1C62480D
DEV6247	S5U1C62470D

Previous No.	New No.
DEV6262	S5U1C62620D
DEV6266	S5U1C62660D
DEV6274	S5U1C62740D
DEV6292	S5U1C62920D
DEV62M2	S5U1C62M20D
DEV6233	S5U1C62N33D
DEV6235	S5U1C62N35D
DEV6251	S5U1C62N51D
DEV6256	S5U1C62560D
DEV6281	S5U1C62N81D
DEV6282	S5U1C62N82D
DEV6S27	S5U1C6S2N7D
DEV6S32	S5U1C6S3N2D
DEV6S37	S5U1C6S3N7D
EVA6008	S5U1C60N08E
EVA6011	S5U1C60N11E
EVA621AR	S5U1C621A0E2
EVA621C	S5U1C621C0E
EVA6237	S5U1C62N37E
EVA623A	S5U1C623A0E

Previous No.	New No.
EVA623B	S5U1C623B0E
EVA623E	S5U1C623E0E
EVA6247	S5U1C62470E
EVA6248	S5U1C62480E
EVA6251R	S5U1C62N51E1
EVA6256	S5U1C62N56E
EVA6262	S5U1C62620E
EVA6266	S5U1C62660E
EVA6274	S5U1C62740E
EVA6281	S5U1C62N81E
EVA6282	S5U1C62N82E
EVA62M1	S5U1C62M10E
EVA62T3	S5U1C62T30E
EVA6S27	S5U1C6S2N7E
EVA6S32R	S5U1C6S3N2E2
ICE62R	S5U1C62000H
KIT6003	S5U1C60N03K
KIT6004	S5U1C60N04K
KIT6007	S5U1C60N07K

CONTENTS

CHAPTER 1	INTRODUCTION	1
	1.1 Configuration	1
	1.2 Features	2
	1.3 Block Diagram	3
	1.4 Pin Layout Diagram	4
	1.5 Pin Description	5
CHAPTER 2	POWER SUPPLY AND INITIAL RESET	6
	2.1 Power Supply	6
	2.2 Initial Reset	8
	Oscillation detection circuit	9
	Reset pin (RESET)	9
	Simultaneous high input to input ports (K00–K03)	9
	Internal register following initialization	10
	2.3 Test Pin (TEST)	10
CHAPTER 3	CPU, ROM, RAM	11
	3.1 CPU	11
	3.2 ROM	12
	3.3 RAM	12
CHAPTER 4	PERIPHERAL CIRCUITS AND OPERATION	13
	4.1 Memory Map	13
	4.2 Oscillation Circuit	16
	Crystal oscillation circuit	16
	CR oscillation circuit	17

4.3	Input Ports (K00–K03)	18
	Configuration of input ports	18
	Input comparison registers and interrupt function ...	19
	Mask option	20
	Control of input ports	20
4.4	Output Ports (R00–R03)	22
	Configuration of output ports	22
	Mask option	23
	Control of output ports	25
4.5	I/O Ports (P00–P03)	28
	Configuration of I/O ports	28
	I/O control register and I/O mode	28
	Mask option	29
	Control of I/O ports	29
4.6	LCD Driver (COM0–COM3, SEG0–SEG19)	31
	Configuration of LCD driver	31
	Cadence adjustment of oscillation frequency	37
	Mask option (segment allocation)	38
	Control of LCD driver	40
4.7	Clock Timer	41
	Configuration of clock timer	41
	Interrupt function	42
	Control of clock timer	43
4.8	A/D Converter	45
	Configuration of A/D converter	45
	Operation of A/D converter	46
	Interrupt function	51
	Usage example of the A/D converter	51
	Control of A/D converter	53
4.9	Heavy Load Protection Function	57
	Operation of heavy load protection function	57
	Control of heavy load protection function	58
4.10	Interrupt and HALT	59
	Interrupt factors	60
	Specific masks and factor flags for interrupt	61
	Interrupt vectors	61
	Control of interrupt	62

CHAPTER 5	BASIC EXTERNAL WIRING DIAGRAM	63
CHAPTER 6	ELECTRICAL CHARACTERISTICS	65
6.1	Absolute Maximum Rating	65
6.2	Recommended Operating Conditions	66
6.3	DC Characteristics	67
6.4	Analog Circuit Characteristics and Power Current Consumption	69
6.5	Oscillation Characteristics	73
CHAPTER 7	PACKAGE	75
7.1	Plastic Package	75
7.2	Ceramic Package for Test Samples	76
CHAPTER 8	PAD LAYOUT	77
8.1	Diagram of Pad Layout	77
8.2	Pad Coordinates	78
CHAPTER 9	PRECAUTIONS ON MOUNTING	79
	Oscillation circuit	79
	Reset circuit	79
	Power supply circuit	79
	Arrangement of signal lines	80
	Precautions for visible radiation (when bare chip is mounted)	80
Appendices	TECHNICAL INFORMATION	81
Appendix A	Design Steps for Designing Thermometer	81
	Thermometer design steps	81
	How to obtain capacitor value and oscillation frequency ..	83
	Setting up counter initial value	84
	Computation method of displayed temperature by linear approximation	85

Appendix B Error Factors 87

 Thermistor resistance dispersion 87

 A/D converter error factors 87

 Error by floating capacity 90

 Software error 90

Appendix C AT Thermistor 91

CHAPTER 1 INTRODUCTION

Each member of the S1C60N05 Series of single chip micro-computers feature a 4-bit S1C6200B core CPU, 1,536 words of ROM (12 bits per word), 80 words of RAM (4 bits per word), an LCD driver, 4 bits for input ports (K00–K03), 4 bits for output ports (R00–R03), one 4-bit I/O port (P00–P03), clock timer and A/D converter.

Because of their low voltage operation and low power consumption, the S1C60N05 Series are ideal for a wide range of applications.

1.1 Configuration

The S1C60N05 Series are configured as follows, depending on the supply voltage.

Table 1.1.1
Configuration of the
S1C60N05 Series

Model	Supply voltage	Oscillation circuits
S1C60N05	1.8–3.5 V	Crystal or CR
S1C60L05	1.2–2.0 V	Crystal or CR

1.2 Features

Core CPU	S1C6200B
Built-in oscillation circuit	Crystal or CR oscillation circuit, 32,768 Hz (typ.)
Instruction set	100 instructions
ROM capacity	1,536 words × 12 bits
RAM capacity (data RAM)	80 words × 4 bits
Input port	4 bits (Supplementary pull-down resistors may be used)
Output port	4 bits (Piezo buzzer and programmable frequency output can be driven directly by mask option)
Input/output port	4 bits
LCD driver	20 segments × 4 common duty (or 3 and 2 common duty)
Timer	Clock timer
A/D converter	CR oscillation type A/D converter built-in (2 channels)
Interrupts:	
External interrupt	Input port interrupt 1 system
Internal interrupt	Timer interrupt 1 system
	A/D converter interrupt 1 system
Supply voltage	1.5 V (1.2–2.0 V) S1C60L05 (During A/D conversion) 3.0 V (1.8–3.5 V) S1C60N05
Current consumption (typ.)	0.8 μA (Crystal oscillation CLK = 32,768 Hz, when halted) 1.5 μA (Crystal oscillation CLK = 32,768 Hz, when executing)
Supply form	QFP6-60pin (plastic) or chip

1.3 Block Diagram

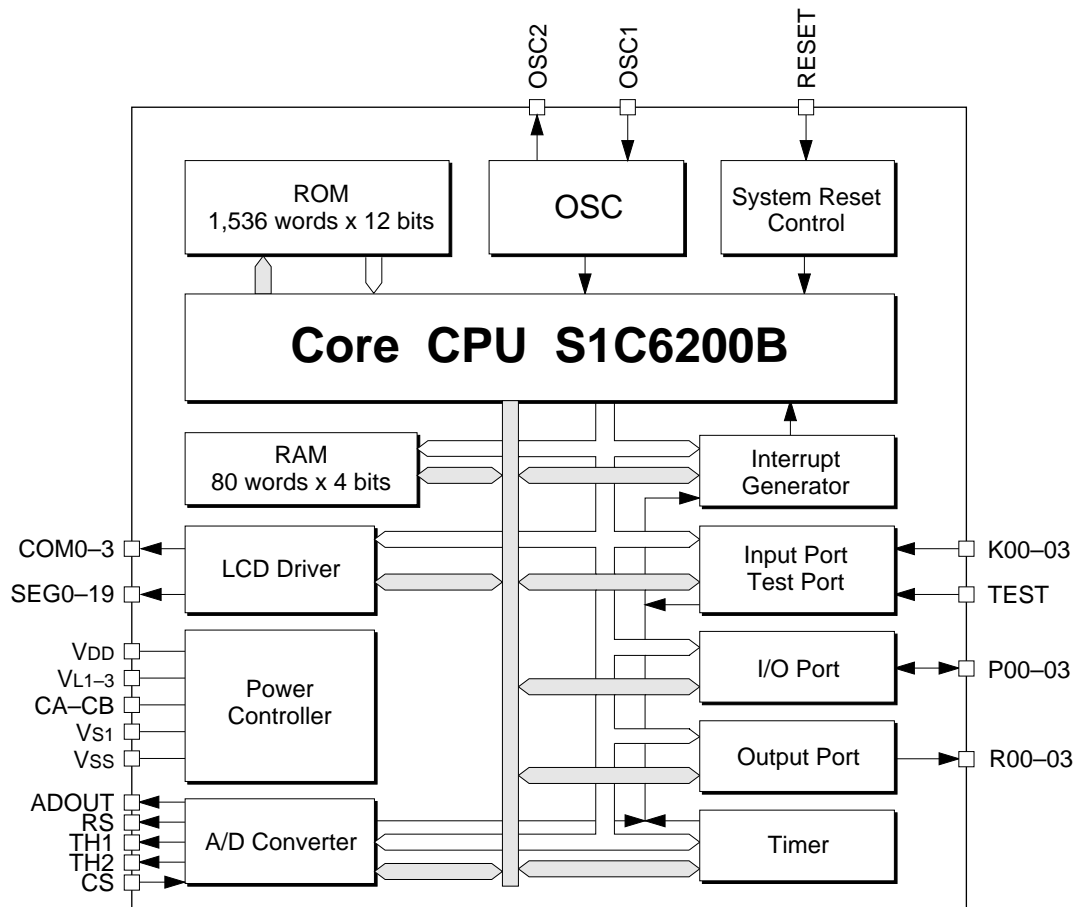
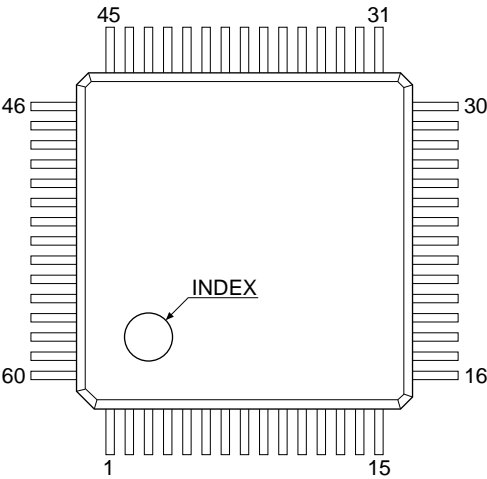


Fig. 1.3.1
Block diagram

1.4 Pin Layout Diagram

QFP6-60pin



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	N.C.	16	N.C.	31	TEST	46	VL3
2	N.C.	17	ADOUT	32	RESET	47	VL2
3	K00	18	SEG0	33	SEG12	48	VL1
4	K01	19	SEG1	34	SEG13	49	CA
5	K02	20	SEG2	35	SEG14	50	CB
6	K03	21	SEG3	36	SEG15	51	VSS
7	R00	22	SEG4	37	SEG16	52	VDD
8	R01	23	SEG5	38	SEG17	53	OSC1
9	R02	24	SEG6	39	SEG18	54	OSC2
10	R03	25	SEG7	40	SEG19	55	Vs1
11	RS	26	SEG8	41	COM0	56	P00
12	TH1	27	SEG9	42	COM1	57	P01
13	TH2	28	SEG10	43	COM2	58	P02
14	CS	29	SEG11	44	COM3	59	P03
15	N.C.	30	N.C.	45	N.C.	60	N.C.

N.C. = No connection

Fig. 1.4.1
Pin assignment

1.5 Pin Description

Table 1.5.1 Pin description

Terminal name	Pin No.	Input/Output	Function
VDD	52	(I)	Power source (+) terminal
VSS	51	(I)	Power source (-) terminal
VS1	55	O	Oscillation and internal logic system regulated voltage output terminal
VL1	48	O	LCD system regulated voltage output terminal
VL2	47	O	LCD system booster output terminal
VL3	46	O	LCD system booster output terminal
CA, CB	49, 50	–	Booster capacitor connecting terminal
OSC1	53	I	Crystal or CR oscillation input terminal
OSC2	54	O	Crystal or CR oscillation output terminal
K00–K03	3–6	I	Input terminal
P00–P03	56–59	I/O	I/O terminal
R00–R03	7–10	O	Output terminal
SEG0–19	18–29 33–40	O	LCD segment output terminal (convertible to DC output terminal by mask option)
COM0–3	41–44	O	LCD common output terminal
CS	14	I	A/D converter CR oscillation input terminal
RS	11	O	A/D converter CR oscillation output terminal
TH1, TH2	12, 13	O	A/D converter CR oscillation output terminal
ADOUT	17	O	A/D converter oscillation frequency output terminal
RESET	32	I	Initial setting input terminal
TEST	31	I	Test input terminal

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

With a single external power supply (*1) supplied to VDD through VSS, the S1C60N05 Series generate the necessary internal voltages with the regulated voltage circuit (<VS1> for oscillators and internal circuit) and the voltage booster/reducer (<VL2, VL3 or VL1, VL3> for LCDs).

When the S1C60N05 LCD power is selected for 4.5 V LCD panel by mask option, the S1C60N05 short-circuits between <VL2> and <VSS> internally, and the voltage booster/reducer generates <VL1> and <VL3>. When 3.0 V LCD panel is selected, the S1C60N05 short-circuits between <VL3> and <VSS>, and the voltage reducer generates <VL1> and <VL2>. The S1C60L05 short-circuits between <VL1> and <VSS>, and the voltage booster generates <VL2> and <VL3>.

The voltage <VS1> for the internal circuit that is generated by the regulated voltage circuit is -1.2 V (VDD standard).

Figure 2.1.1 shows the power supply configuration of the S1C60N05 Series in each condition.

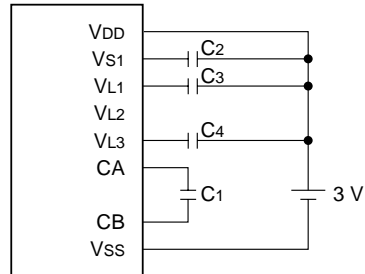
*1 Supply voltage: S1C60N05 3.0 V
S1C60L05 1.5 V

- Note* - External loads cannot be driven by the output voltage of the regulated voltage circuit and the voltage booster/reducer.
- See Chapter 6, "ELECTRICAL CHARACTERISTICS", for voltage values.

• S1C60N05

4.5 V LCD panel

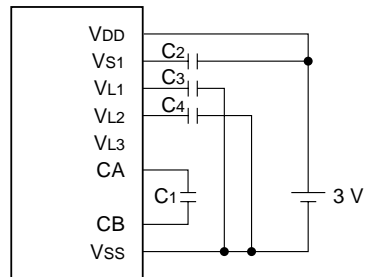
1/4, 1/3, 1/2 duty, 1/3 bias



Note: VL2 is shorted to Vss inside the IC.

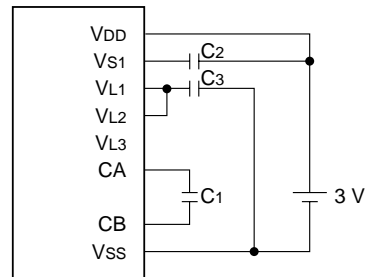
3 V LCD panel

1/4, 1/3, 1/2 duty, 1/3 bias



3 V LCD panel

1/4, 1/3, 1/2 duty, 1/2 bias

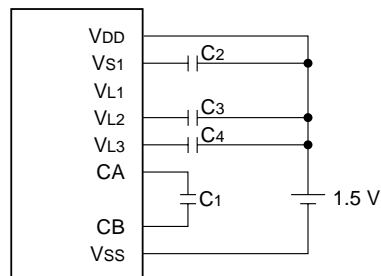


Note: VL3 is shorted to Vss inside the IC.

• S1C60L05

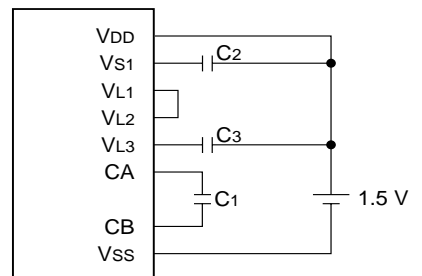
4.5 V LCD panel

1/4, 1/3, 1/2 duty, 1/3 bias



3 V LCD panel

1/4, 1/3, 1/2 duty, 1/2 bias



Note: VL1 is shorted to Vss inside the IC.

Fig. 2.1.1 External element configuration of power system

2.2 Initial Reset

To initialize the S1C60N05 Series circuits, an initial reset must be executed. There are three ways of doing this.

- (1) Initial reset by the oscillation detection circuit (*Note*)
- (2) External initial reset via the RESET pin
- (3) External initial reset by simultaneous high input to pins K00–K03 (depending on mask option)

Figure 2.2.1 shows the configuration of the initial reset circuit.

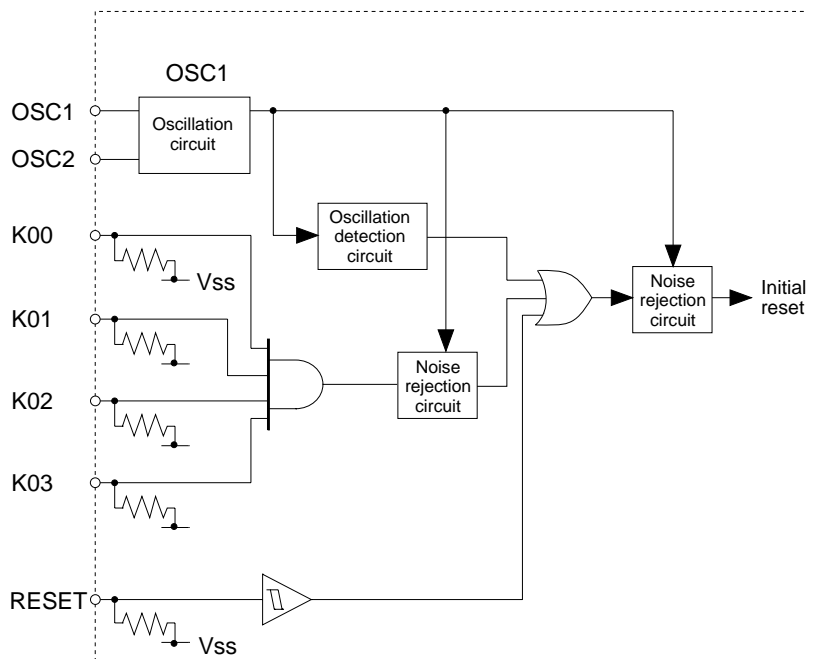


Fig. 2.2.1
Configuration of
initial reset circuit

Note Since the circuit may sometimes not operate normally with the initial resetting by the oscillation detection circuit indicated in number (1), depending on the method of making the power, you should utilize one of the initial resetting methods mentioned in numbers (2) and (3).

Oscillation detection circuit

When the oscillation circuit has been stopped until the oscillation circuit begins to oscillate when the power is turned on or for any other reason, the oscillation detection circuit will output an initial reset signal, but since the circuit may sometimes not operate normally with the initial resetting due to the oscillation detection circuit, depending on the method of making the power, you should utilize one of the initial resetting methods indicated hereafter.

Reset pin (RESET)

An initial reset can be invoked externally by making the reset pin high. This high level must be maintained for at least 5 ms (when oscillating frequency, $f_{osc} = 32 \text{ kHz}$), because the initial reset circuit contains a noise rejection circuit. When the reset pin goes low the CPU begins to operate.

Simultaneous high input to input ports (K00–K03)

Another way of invoking an initial reset externally is to input a high signal simultaneously to the input ports (K00–K03) selected with the mask option. The specified input port pins must be kept high for at least 4 sec (when oscillating frequency $f_{osc} = 32 \text{ kHz}$), because of the noise rejection circuit. Table 2.2.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

Table 2.2.1
Input port combinations

A	Not used
B	K00*K01
C	K00*K01*K02
D	K00*K01*K02*K03

When, for instance, mask option D (K00*K01*K02*K03) is selected, an initial reset is executed when the signals input to the four ports K00–K03 are all high at the same time.

If you use this function, make sure that the specified ports do not go high at the same time during normal operation.

Internal register following initialization

An initial reset initializes the CPU as shown in the table below.

Table 2.2.2
Initial values

CPU Core			
Name	Signal	Number of bits	Setting value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
New page pointer	NPP	4	1H
Stack pointer	SP	8	Undefined
Index register X	X	8	Undefined
Index register Y	Y	8	Undefined
Register pointer	RP	4	Undefined
General register A	A	4	Undefined
General register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	80×4	Undefined
Display memory	20×4	Undefined
Other peripheral circuit	—	*1

*1: See Section 4.1, "Memory Map"

2.3 Test Pin (TEST)

This pin is used when IC is inspected for shipment.
During normal operation connect it to VSS.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The S1C60N05 Series employs the S1C6200B core CPU, so that register configuration, instructions, and so forth are virtually identical to those in other processors in the family using the S1C6200B. Refer to the "S1C6200/6200A Core CPU Manual" for details of the S1C6200B.

Note the following points with regard to the S1C60N05 Series:

- (1) The SLEEP operation is not provided, so the SLP instruction cannot be used.
- (2) Because the ROM capacity is 1,536 words, 12 bits per word, bank bits are unnecessary, and PCB and NBP are not used.
- (3) The RAM page is set to 0 only, so the page part (XP, YP) of the index register that specifies addresses is invalid.

PUSH	XP	PUSH	YP
POP	XP	POP	YP
LD	XP,r	LD	YP,r
LD	r,XP	LD	r,YP

3.2 ROM

The built-in ROM, a mask ROM for the program, has a capacity of $1,536 \times 12$ -bit steps. The program area is 6 pages (0–5), each consisting of 256 steps (00H–FFH). After an initial reset, the program start address is page 1, step 00H. The interrupt vector is allocated to page 1, steps 01H–07H.

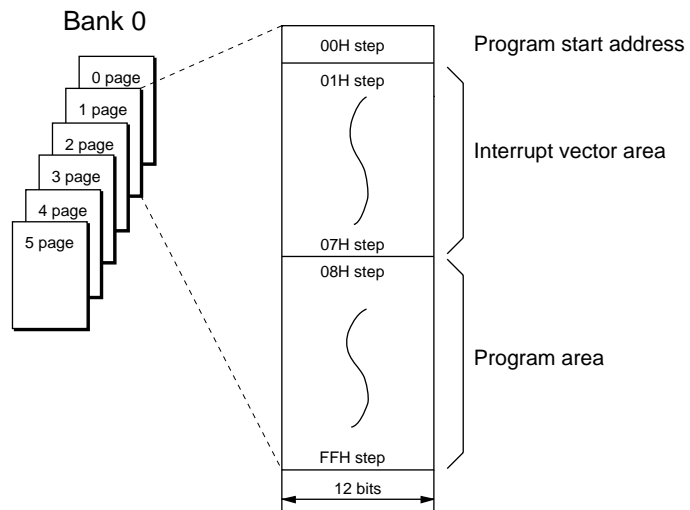


Fig. 3.2.1
ROM configuration

3.3 RAM

The RAM, a data memory for storing a variety of data, has a capacity of 80 words, 4-bit words. When programming, keep the following points in mind:

- (1) Part of the data memory is used as stack area when saving subroutine return addresses and registers, so be careful not to overlap the data area and stack area.
- (2) Subroutine calls and interrupts take up three words on the stack.
- (3) Data memory 000H–00FH is the memory area pointed by the register pointer (RP).

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

Peripheral circuits (timer, I/O, and so on) of the S1C60N05 Series are memory mapped. Thus, all the peripheral circuits can be controlled by using memory operations to access the I/O memory. The following sections describe how the peripheral circuits operate.

4.1 Memory Map

The data memory of the S1C60N05 Series has an address space of 137 words, of which 32 words are allocated to display memory and 25 words, to I/O memory. Figure 4.1.1 show the overall memory map for the S1C60N05 Series, and Tables 4.1.1(a) and (b), the memory maps for the peripheral circuits (I/O space).

Address Page	Low High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	MA	MB	MC	MD	ME	MF
0	0	RAM area (000H–04FH) 80 words x 4 bits (R/W)															
	1																
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9	Display memory area (090H–0AFH) 32 words x 4 bits (Write only)															
	A																
	B																
	C																
	D																
	E																
	F																

Fig. 4.1.1
Memory map

 Unused area

Note Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Table 4.1.1(a) I/O memory map

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
0E0H	K03	K02	K01	K00	K03	– *2	High	Low	Input port data K03
					K02	– *2	High	Low	Input port data K02
					K01	– *2	High	Low	Input port data K01
					K00	– *2	High	Low	Input port data K00
0E3H	TM3	TM2	TM1	TM0	TM3	– *3	High	Low	Clock timer data 2 Hz
					TM2	– *3	High	Low	Clock timer data 4 Hz
					TM1	– *3	High	Low	Clock timer data 8 Hz
					TM0	– *3	High	Low	Clock timer data 16 Hz
0E4H	TC3	TC2	TC1	TC0	TC3	– *3	1	0	Up/down counter data TC3
					TC2	– *3	1	0	Up/down counter data TC2
					TC1	– *3	1	0	Up/down counter data TC1
					TC0	– *3	1	0	Up/down counter data TC0 (LSB)
0E5H	TC7	TC6	TC5	TC4	TC7	– *3	1	0	Up/down counter data TC7
					TC6	– *3	1	0	Up/down counter data TC6
					TC5	– *3	1	0	Up/down counter data TC5
					TC4	– *3	1	0	Up/down counter data TC4
0E6H	TC11	TC10	TC9	TC8	TC11	– *3	1	0	Up/down counter data TC11
					TC10	– *3	1	0	Up/down counter data TC10
					TC9	– *3	1	0	Up/down counter data TC9
					TC8	– *3	1	0	Up/down counter data TC8
0E7H	TC15	TC14	TC13	TC12	TC15	– *3	1	0	Up/down counter data TC15 (MSB)
					TC14	– *3	1	0	Up/down counter data TC14
					TC13	– *3	1	0	Up/down counter data TC13
					TC12	– *3	1	0	Up/down counter data TC12
0E8H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register K03
					EIK02	0	Enable	Mask	Interrupt mask register K02
					EIK01	0	Enable	Mask	Interrupt mask register K01
					EIK00	0	Enable	Mask	Interrupt mask register K00
0EBH	0	EIT2	EIT8	EIT32	0				*5
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer) 2 Hz
					EIT8	0	Enable	Mask	Interrupt mask register (clock timer) 8 Hz
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer) 32 Hz
0ECH	0	0	0	EIAD	0				*5
					0				*5
					0				*5
					EIAD	0	Enable	Mask	Interrupt mask register (A/D)
0EDH	0	0	0	IK0	0				*5
					0				*5
					0				*5
					IK0	0	Yes	No	Interrupt factor flag (K00–K03)
0EFH	0	IT2	IT8	IT32	0				*5
					IT2	0	Yes	No	Interrupt factor flag (clock timer) 2 Hz
					IT8	0	Yes	No	Interrupt factor flag (clock timer) 8 Hz
					IT32	0	Yes	No	Interrupt factor flag (clock timer) 32 Hz

*1 Initial value following initial reset

*2 Not set in the circuit

*3 Undefined

*4 Reset (0) immediately after being read

*5 Always "0" when being read

*6 Refer to main manual

Table 4.1.1(b) I/O memory map

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
0F0H	0	0	0	IAD	0				*5
					0				*5
					0				*5
	R				IAD	0	Yes	No	Interrupt factor flag (A/D)
0F1H	CHTH	0	0	ADRUN	CHTH	0	TH2	TH1	A/D channel selection
					0				*5
	R/W	R		R/W	0				*5
					ADRUN	0	Start	Stop	A/D conversion Start/Stop
0F3H	R03	R02	R01	R00	R03	0	High	Low	Output port data R03
					R02	0	High	Low	Output port data R02
					R01	0	High	Low	Output port data R01
					BUZZER	0	On	Off	Buzzer On/Off control register
					R00	0	High	Low	Output port data R00
					FOUT	0	On	Off	Frequency output control register
0F4H	P03	P02	P01	P00	P03	– *2	High	Low	I/O port data P03
					P02	– *2	High	Low	I/O port data P02
					P01	– *2	High	Low	I/O port data P01
					P00	– *2	High	Low	I/O port data P00
0F5H	C3	C2	C1	C0	C3	– *3	1	0	Up-counter data C3
					C2	– *3	1	0	Up-counter data C2
					C1	– *3	1	0	Up-counter data C1
					C0	– *3	1	0	Up-counter data C0 (LSB)
0F6H	C7	C6	C5	C4	C7	– *3	1	0	Up-counter data C7
					C6	– *3	1	0	Up-counter data C6
					C5	– *3	1	0	Up-counter data C5
					C4	– *3	1	0	Up-counter data C4
0F7H	C11	C10	C9	C8	C11	– *3	1	0	Up-counter data C11
					C10	– *3	1	0	Up-counter data C10
					C9	– *3	1	0	Up-counter data C9
					C8	– *3	1	0	Up-counter data C8
0F8H	C15	C14	C13	C12	C15	– *3	1	0	Up-counter data C15 (MSB)
					C14	– *3	1	0	Up-counter data C14
					C13	– *3	1	0	Up-counter data C13
					C12	– *3	1	0	Up-counter data C12
0F9H	0	0	0	TMRST	0				*5
					0				*5
					0				*5
	R			W	TMRST	Reset	Reset	–	Clock timer reset
0FAH	HLMOD	0	0	0	HLMOD	0	Heavy	Normal	Heavy load protection mode register
					0				*5
	R/W	R			0				*5
					0				*5
0FBH	CSDC	0	0	0	CSDC	0	Static	Dynamic	LCD drive switch
					0				*5
					0				*5
	R/W	R			0				*5
0FCH	0	0	0	IOC	0				*5
					0				*5
					0				*5
	R			R/W	IOC	0	Out	In	I/O port I/O control register
0FDH	XBZR	0	XFOUT1	XFOUT0	XBZR	0	2 kHz	4 kHz	Buzzer frequency control
					0				*5
	R/W	R	R/W		XFOUT1	0			FOUT frequency control
					XFOUT0	0			FOUT frequency control
0FEH	0	0	0	ADCLK	0				*5
					0				*5
					0				*5
	R			R/W	ADCLK	0	65 kHz	32 kHz	A/D clock selection 65 kHz/32 kHz

4.2 Oscillation Circuit

The S1C60N05 Series has a built-in oscillation circuit. For the oscillation circuit, either crystal oscillation or CR oscillation may be selected by a mask option.

Crystal oscillation circuit

The crystal oscillation circuit generates the operating clock for the CPU and peripheral circuit on connection to an external crystal oscillator (typ. 32.768 kHz) and trimmer capacitor (5–25 pF).

Figure 4.2.1 is the block diagram of the crystal oscillation circuit.

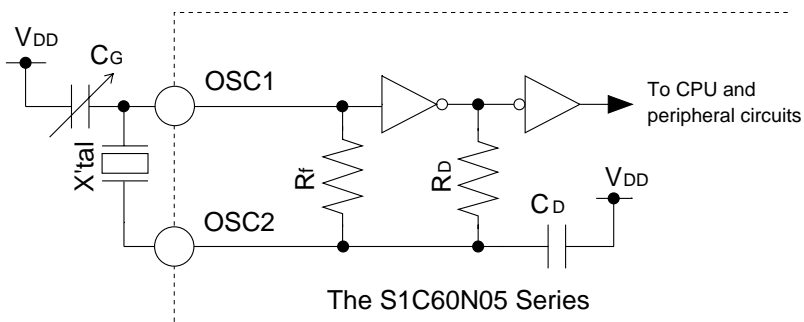


Fig. 4.2.1
Crystal oscillation circuit

As Figure 4.2.1 indicates, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal) between the OSC1 and OSC2 pins and the trimmer capacitor (CG) between the OSC1 and VDD pins.

CR oscillation circuit

For the S1C60N05 Series, CR oscillation circuit (typ. 65 kHz) may be selected by a mask option. Figure 4.2.2 is the block diagram of the CR oscillation circuit.

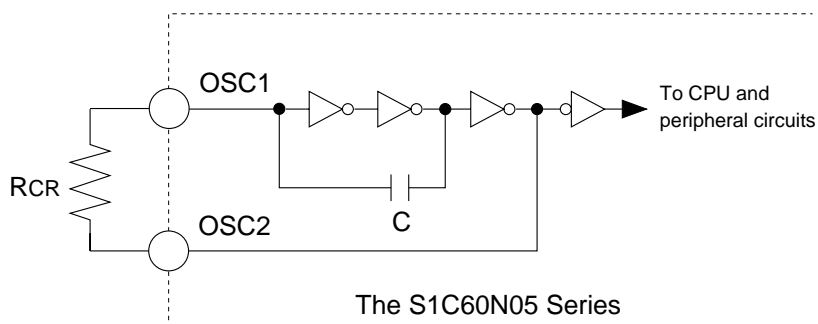


Fig. 4.2.2
CR oscillation circuit

As Figure 4.2.2 indicates, the CR oscillation circuit can be configured simply by connecting the register (RCR) between pins OSC1 and OSC2 since capacity (C) is built-in. See Chapter 6, "ELECTRICAL CHARACTERISTICS" for RCR value.

4.3 Input Ports (K00–K03)

Configuration of input ports

The S1C60N05 Series has a general-purpose input (4 bits). Each of the input port pins (K00–K03) has an internal pull-down resistance. The pull-down resistance can be selected for each bit with the mask option.

Figure 4.3.1 shows the configuration of input port.

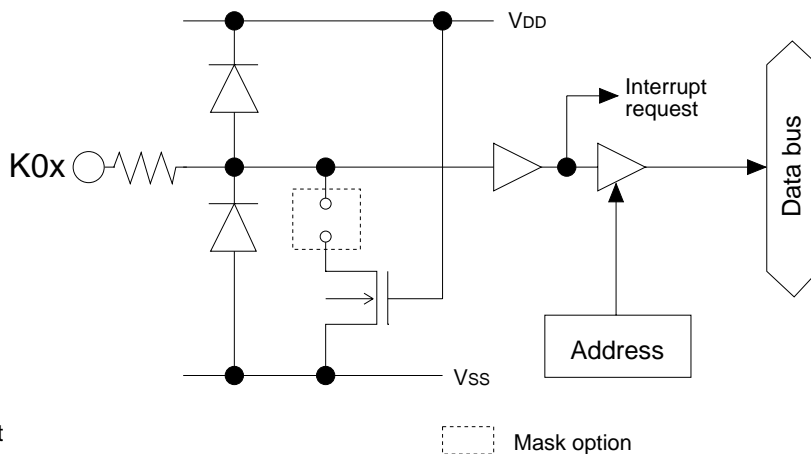


Fig. 4.3.1

Configuration of input port

Selecting "pull-down resistance enabled" with the mask option allows input from a push button, key matrix, and so forth. When "pull-down resistance disabled" is selected, the port can be used for slide switch input and interfacing with other LSIs.

Input comparison registers and interrupt function

All four input port bits (K00–K03) provide the interrupt function. The conditions for issuing an interrupt can be set by the software for the four bits. Also, whether to mask the interrupt function can be selected individually for all four bits by the software. Figure 4.3.2 shows the configuration of K00–K03.

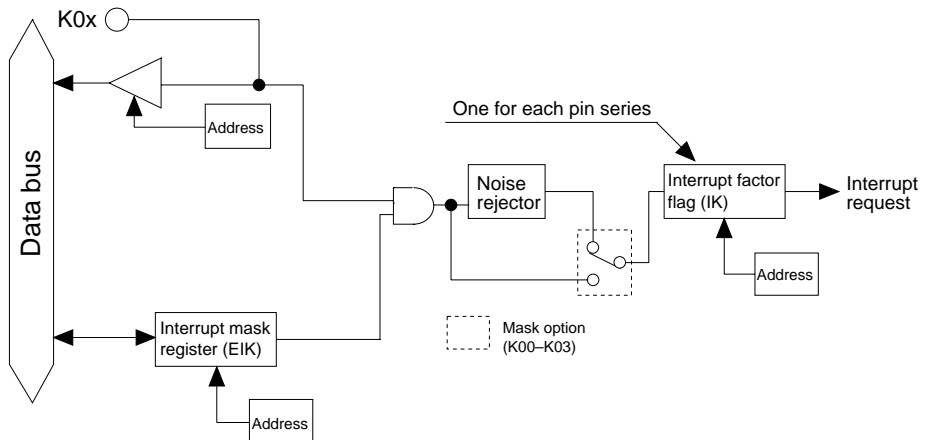


Fig. 4.3.2
Input interrupt circuit
configuration (K00–K03)

The interrupt mask registers (EIK00–EIK03) enable the interrupt mask to be selected individually for K00–K03. An interrupt occurs when the input value which are not masked change and the interrupt factor flag (IK0) is set to "1".

Mask option

The contents that can be selected with the input port mask option are as follows:

- (1) An internal pull-down resistance can be selected for each of the four bits of the input ports (K00–K03). Having selected "pull-down resistance disabled", take care that the input does not float. Select "pull-down resistance enabled" for input ports that are not being used.
- (2) The input interrupt circuit contains a noise rejection circuit to prevent interrupts from occurring through noise. The mask option enables selection of the noise rejection circuit for each separate pin series. When "use" is selected, a maximum delay of 0.5 ms ($f_{osc} = 32 \text{ kHz}$) occurs from the time an interrupt condition is established until the interrupt factor flag (IK) is set to "1".

Control of input ports

Table 4.3.1 list the input port control bits and their addresses.

Table 4.3.1 Input port control bits

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
0E0H	K03	K02	K01	K00	K03	– *2	High	Low	Input port data K03
					K02	– *2	High	Low	Input port data K02
					K01	– *2	High	Low	Input port data K01
					K00	– *2	High	Low	Input port data K00
	R								
0E8H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register K03
					EIK02	0	Enable	Mask	Interrupt mask register K02
					EIK01	0	Enable	Mask	Interrupt mask register K01
					EIK00	0	Enable	Mask	Interrupt mask register K00
	R/W								
0EDH	0	0	0	IK0	0				*5
					0				*5
					0				*5
					IK0	0	Yes	No	*4
	R								

*1 Initial value following initial reset

*2 Not set in the circuit

*3 Undefined

*4 Reset (0) immediately after being read

*5 Always "0" when being read

*6 Refer to main manual

K00–K03 Input port data (0E0H)

The input data of the input port pins can be read with these registers.

When "1" is read:	High level
When "0" is read:	Low level
Writing:	Invalid

The value read is "1" when the pin voltage of the four bits of the input ports (K00–K03) goes high (VDD), and "0" when the voltage goes low (VSS). These bits are reading, so writing cannot be done.

EIK00–EIK03 Interrupt mask registers (0E8H)

Masking the interrupt of the input port pins can be done with these registers.

When "1" is written:	Enable
When "0" is written:	Mask
Reading:	Valid

With these registers, masking of the input port bits can be done for each of the four bits. After an initial reset, these registers are all set to "0".

IK0 Interrupt factor flags (0EDH D0)

These flags indicate the occurrence of an input interrupt.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

The interrupt factor flag IK0 is associated with K00–K03, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred. These flags are reset when the software has read them. Reading of interrupt factor flags is available at EI, but be careful in the following cases.

If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. After an initial reset, these flags are set to "0".

4.4 Output Ports (R00–R03)

Configuration of output ports

The S1C60N05 Series has 4 bits for general output ports (R00–R03).

Output specifications of the output ports can be selected individually with the mask option. Three kinds of output specifications are available: complementary output and Pch open drain output. Also, the mask option enables the output ports R00 and R01 to be used as special output ports. Figure 4.4.1 shows the configuration of the output ports.

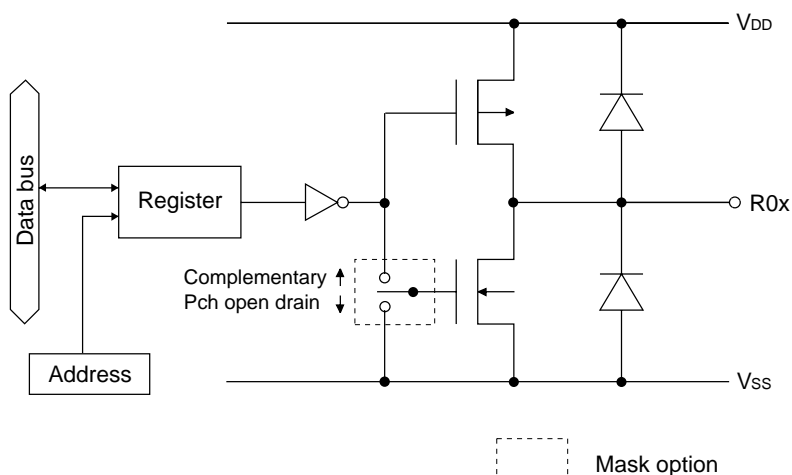


Fig. 4.4.1
Configuration of output ports

Mask option

The mask option enables the following output port selection.

(1) Output specifications of output ports

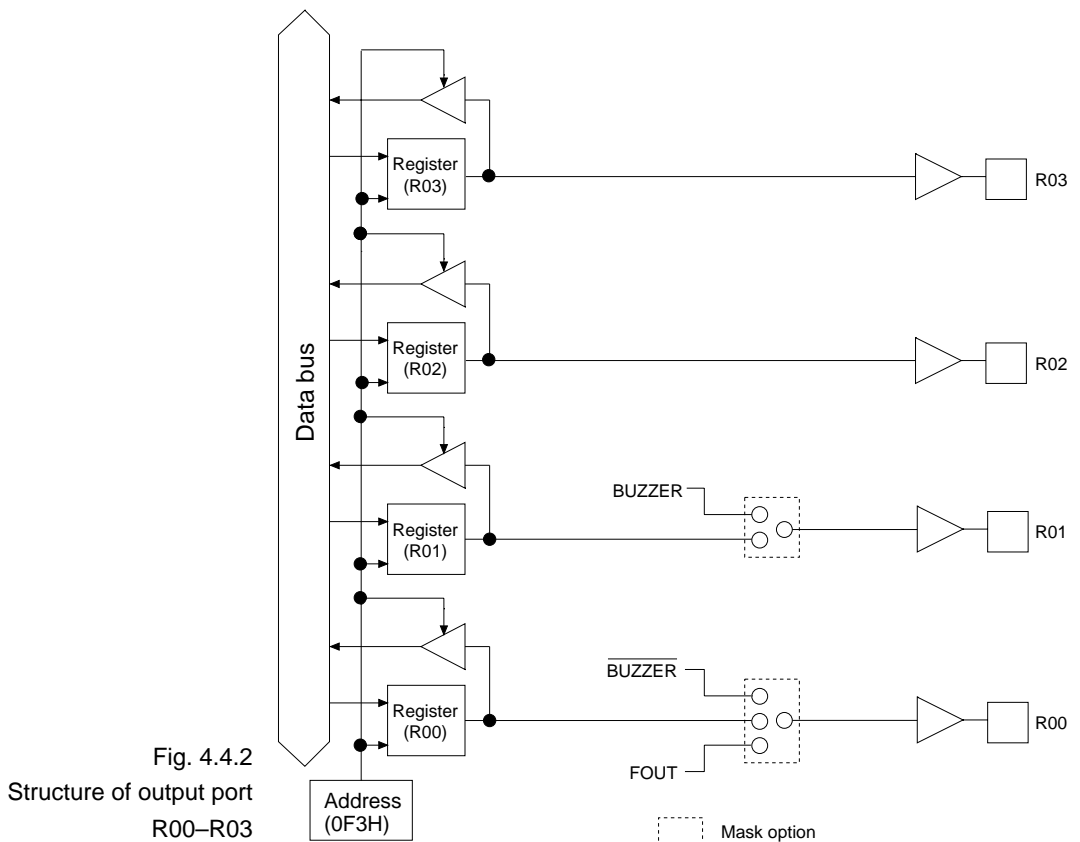
The output specifications for the output ports (R00–R03) may be either complementary output or Pch open drain output for each of the four bits. However, even when Pch open drain output is selected, a voltage exceeding the source voltage must not be applied to the output port.

(2) Special output

In addition to the regular DC output, special output can be selected for output ports R00 and R01, as shown in Table 4.4.1. Figure 4.4.2 shows the structure of output ports R00–R03.

Table 4.4.1
Special output

Pin name	When special output is selected
R00	FOUT or $\overline{\text{BUZZER}}$
R01	BUZZER



FOUT (R00) When output port R00 is set for FOUT output, this port will generate fosc (CPU operating clock frequency) or clock frequency divided into fosc. Clock frequency may be selected individually for F1–F4, from among 5 types by mask option; one among F1–F4 is selected by software and used. The types of frequency which may be selected are shown in Table 4.4.2.

Table 4.4.2
FOUT clock frequency

Setting value	Clock frequency (Hz) fosc = 32,768			
	F1	F2	F3	F4
	(D1,D0)=(0,0)	(D1,D0)=(0,1)	(D1,D0)=(1,0)	(D1,D0)=(1,1)
1	256 (fosc/128)	512 (fosc/64)	1,024 (fosc/32)	2,048 (fosc/16)
2	512 (fosc/64)	1,024 (fosc/32)	2,048 (fosc/16)	4,096 (fosc/8)
3	1,024 (fosc/32)	2,048 (fosc/16)	4,096 (fosc/8)	8,192 (fosc/4)
4	2,048 (fosc/16)	4,096 (fosc/8)	8,192 (fosc/4)	16,384 (fosc/2)
5	4,096 (fosc/8)	8,192 (fosc/4)	16,384 (fosc/2)	32,768 (fosc/1)

(D1, D0) = (XFOUT1, XFOUT0)

Note A hazard may occur when the FOUT signal is turned on or off.

BUZZER, $\overline{\text{BUZZER}}$ (R01, R00) Output ports R01 and R00 may be set to BUZZER output and $\overline{\text{BUZZER}}$ output (BUZZER reverse output), respectively, allowing for direct driving of the piezo-electric buzzer. $\overline{\text{BUZZER}}$ output (R00) may only be set if R01 is set to BUZZER output. In such case, whether ON/OFF of the $\overline{\text{BUZZER}}$ output is done through R00 register or is controlled through R01 simultaneously with BUZZER output is also selected by mask option. The frequency of buzzer output may be selected by software to be either 2 kHz or 4 kHz.

Note A hazard may occur when the BUZZER signal is turned on or off.

Control of output ports

Table 4.4.3 lists the output port control bits and their addresses.

Table 4.4.3 Control bits of output ports

Address	Register				Comment				
	D3	D2	D1	D0	Name	Init *1	1	0	
0F3H	R03	R02	R01	R00	R03	0	High	Low	Output port data R03
			BUZZER	FOUT	R02	0	High	Low	Output port data R02
					R01	0	High	Low	Output port data R01
	R/W				BUZZER	0	On	Off	Buzzer On/Off control register
					R00	0	High	Low	Output port data R00
					FOUT	0	On	Off	Frequency output control register
0FDH	XBZR	0	XFOUT1	XFOUT0	XBZR	0	2 kHz	4 kHz	Buzzer frequency control
	R/W	R	R/W		0				
				XFOUT1	0			FOUT frequency control	
					XFOUT0	0			FOUT frequency control

*1 Initial value following initial reset

*2 Not set in the circuit

*3 Undefined

*4 Reset (0) immediately after being read

*5 Always "0" when being read

*6 Refer to main manual

R00–R03 Output port data (0F3H)

Sets the output data for the output ports.

When "1" is written: High output

When "0" is written: Low output

Reading: Valid

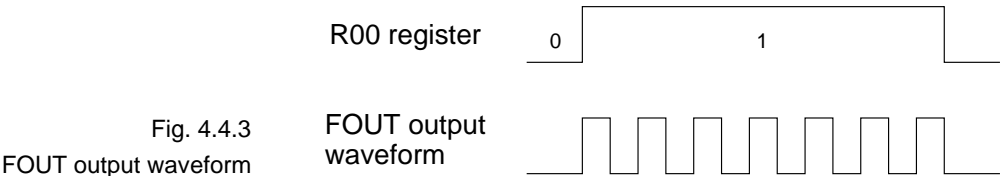
The output port pins output the data written to the corresponding registers (R00–R03) without changing it. When "1" is written to the register, the output port pin goes high (VDD), and when "0" is written, the output port pin goes low (VSS). After an initial reset, all registers are set to "0".

R00 (when FOUT is selected) Special output port data (0F3H D0)
Controls the FOUT (clock) output.

When "1" is written: Clock output
When "0" is written: Low level (DC) output
Reading: Valid

FOUT output can be controlled by writing data to R00. After an initial reset, this register is set to "0".

Figure 4.4.3 shows the output waveform for FOUT output.



XFOUT0, XFOUT1 FOUT frequency control (0FDH D0, 0FDH D1)
Selects the output frequency when R00 port is set for FOUT output.

Table 4.4.4
FOUT frequency selection

XFOUT1	XFOUT0	Frequency selection
0	0	F1
0	1	F2
1	0	F3
1	1	F4

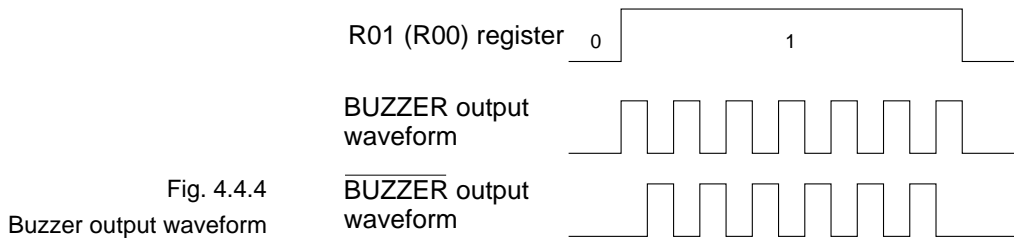
After an initial reset, these registers are set to "0".

R00, R01 (when $\overline{\text{BUZZER}}$ and BUZZER is selected)	Special output port data (0F3H D0, 0F3H D1) Controls the buzzer output.
	When "1" is written: Buzzer output
	When "0" is written: Low level (DC) output
	Reading: Valid

$\overline{\text{BUZZER}}$ and BUZZER output can be controlled by writing data to R00 and R01.

When $\overline{\text{BUZZER}}$ output by R01 register control is selected by mask option, BUZZER output and $\overline{\text{BUZZER}}$ output can be controlled simultaneously by writing data to R01 register. After an initial reset, these registers are set to "0".

Figure 4.4.4 shows the output waveform for buzzer output.



XBZR	Buzzer frequency control (0FDH D3) Selects the frequency of the buzzer signal.
------	---

When "1" is written:	2 kHz
When "0" is written:	4 kHz
Reading:	Valid

When R00 and R01 port is set to buzzer output, the frequency of the buzzer signal can be selected by this register. When "1" is written to this register, the frequency is set in 2 kHz, and in 4 kHz when "0" is written. After an initial reset, this register is set to "0".

4.5 I/O Ports (P00–P03)

Configuration of I/O ports

The S1C60N05 Series has a 4-bit general-purpose I/O port. Figure 4.5.1 shows the configuration of the I/O port. The four bits of the I/O port P00–P03 can be set to either input mode or output mode. The mode can be set by writing data to the I/O control register (IOC).

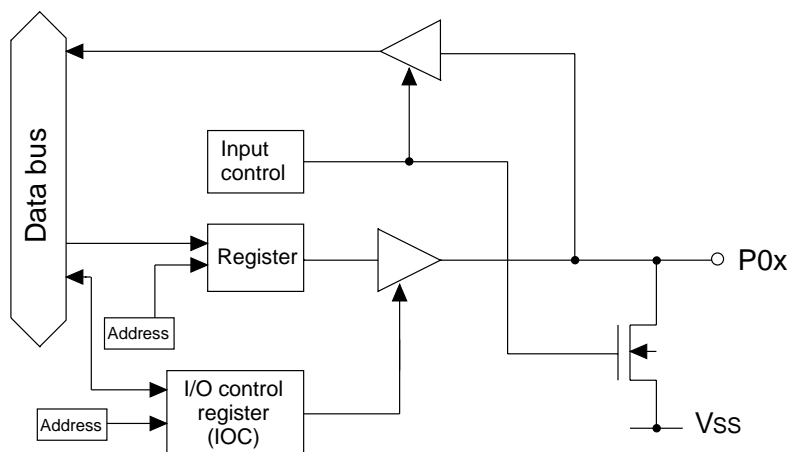


Fig. 4.5.1
Configuration of I/O port

I/O control register and I/O mode

Input or output mode can be set for the four bits of I/O port P00–P03 by writing data into I/O control register IOC. To set the input mode, "0" is written to the I/O control register. When an I/O port is set to input mode, its impedance becomes high and it works as an input port. However, the input line is pulled down when input data is read.

The output mode is set when "1" is written to the I/O control register (IOC). When an I/O port set to output mode works as an output port, it outputs a high signal (VDD) when the port output data is "1", and a low signal (VSS) when the port output data is "0".

After an initial reset, the I/O control register is set to "0", and the I/O port enters the input mode.

Mask option

The output specification during output mode (IOC = "1") of the I/O port can be set with the mask option for either complementary output or Pch open drain output. This setting can be performed for each bit of the I/O port. However, when Pch open drain output has been selected, voltage in excess of the supply voltage must not be applied to the port.

Control of I/O ports

Table 4.5.1 lists the I/O port control bits and their addresses.

Table 4.5.1 I/O port control bits

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
0F4H	P03	P02	P01	P00	P03	– *2	High	Low	I/O port data P03
					P02	– *2	High	Low	I/O port data P02
					P01	– *2	High	Low	I/O port data P01
					P00	– *2	High	Low	I/O port data P00
0FCH	0	0	0	IOC	0				*5
					0				*5
					0				*5
					IOC	0	Out	In	I/O port I/O control register

*1 Initial value following initial reset

*2 Not set in the circuit

*3 Undefined

*4 Reset (0) immediately after being read

*5 Always "0" when being read

*6 Refer to main manual

P00–P03 I/O port data (0F4H)

I/O port data can be read and output data can be written through the port.

• When writing data

When "1" is written: High level

When "0" is written: Low level

When an I/O port is set to the output mode, the written data is output from the I/O port pin unchanged. When "1" is written as the port data, the port pin goes high (VDD), and when "0" is written, the level goes low (VSS). Port data can also be written in the input mode.

- When reading data

When "1" is read: High level

When "0" is read: Low level

The pin voltage level of the I/O port is read. When the I/O port is in the input mode the voltage level being input to the port pin can be read; in the output mode the output voltage level can be read. When the pin voltage is high (VDD) the port data read is "1", and when the pin voltage is low (VSS) the data is "0". Also, the built-in pull-down resistance functions during reading, so the I/O port pin is pulled down.

- Note*
- When the I/O port is set to the output mode and a low-impedance load is connected to the port pin, the data written to the register may differ from the data read.
 - When the I/O port is set to the input mode and a low-level voltage (Vss) is input by the built-in pull-down resistance, an erroneous input results if the time constant of the capacitive load of the input line and the built-in pull-down resistance load is greater than the read-out time. When the input data is being read, the time that the input line is pulled down is equivalent to 0.5 cycles of the CPU system clock. Hence, the electric potential of the pins must settle within 0.5 cycles. If this condition cannot be met, some measure must be devised, such as arranging a pull-down resistance externally, or performing multiple read-outs.

IOC I/O control register (0FCH D0)

The input or output I/O port mode can be set with this register.

When "1" is written: Output mode

When "0" is written: Input mode

Reading: Valid

The input or output mode of the I/O port is set in units of four bits. For instance, IOC sets the mode for P00-P03. Writing "1" to the I/O control register makes the I/O port enter the output mode, and writing "0", the input mode. After an initial reset, the IOC register is set to "0", so the I/O port is in the input mode.

4.6 LCD Driver (COM0–COM3, SEG0–SEG19)

Configuration of LCD driver

The S1C60N05 Series has four common pins and 20 (SEG0–SEG19) segment pins, so that an LCD with a maximum of 80 (20×4) segments can be driven. The power for driving the LCD is generated by the CPU internal circuit, so there is no need to supply power externally.

The driving method is 1/4 duty (or 1/3, 1/2 duty by mask option) dynamic drive, adopting the four types of potential (1/3 bias), VDD, VL1, VL2 and VL3. Moreover, the 1/2 bias dynamic drive that uses three types of potential, VDD, VL1 = VL2 and VL3, can be selected by setting the mask option (drive duty can also be selected from 1/4, 1/3 or 1/2). 1/2 bias drive is effective when the LCD system regulated voltage circuit is not used. The VL1 terminal and the VL2 terminal should be connected outside of the IC.

The frame frequency is 32 Hz for 1/4 duty and 1/2 duty, and 42.7 Hz for 1/3 duty (in the case of $f_{osc} = 32.768$ kHz). Figure 4.6.1 shows the drive waveform for 1/4 duty (1/3 bias), Figure 4.6.2 shows the drive waveform for 1/3 duty (1/3 bias), Figure 4.6.3 shows the drive waveform for 1/2 duty (1/3 bias), Figure 4.6.4 shows the drive waveform for 1/4 duty (1/2 bias), Figure 4.6.5 shows the drive waveform for 1/3 duty (1/2 bias) and Figure 4.6.6 shows the drive waveform for 1/2 duty (1/2 bias).

Note f_{osc} indicates the oscillation frequency of the oscillation circuit.

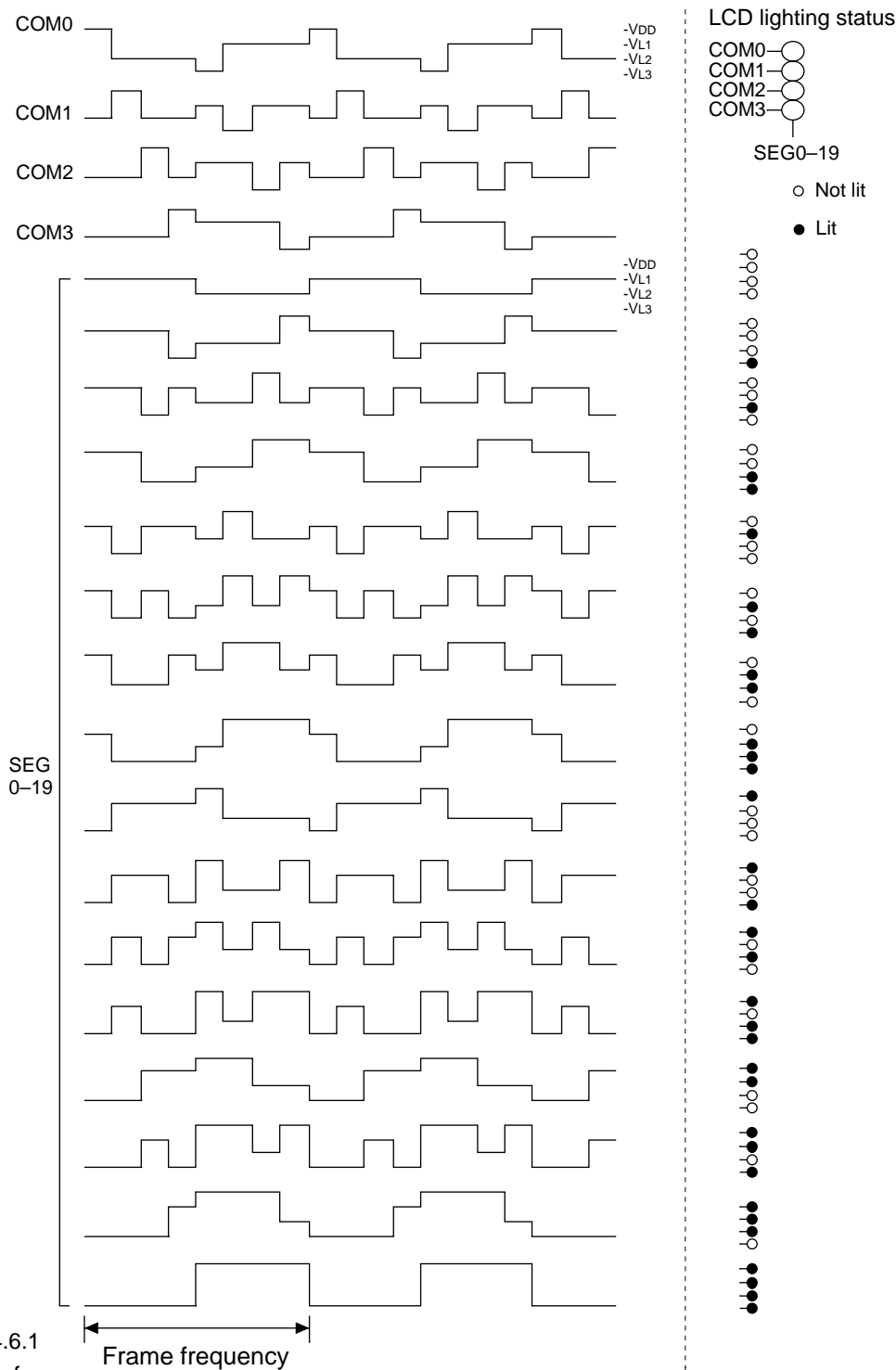


Fig. 4.6.1
Drive waveform for
1/4 duty (1/3 bias)

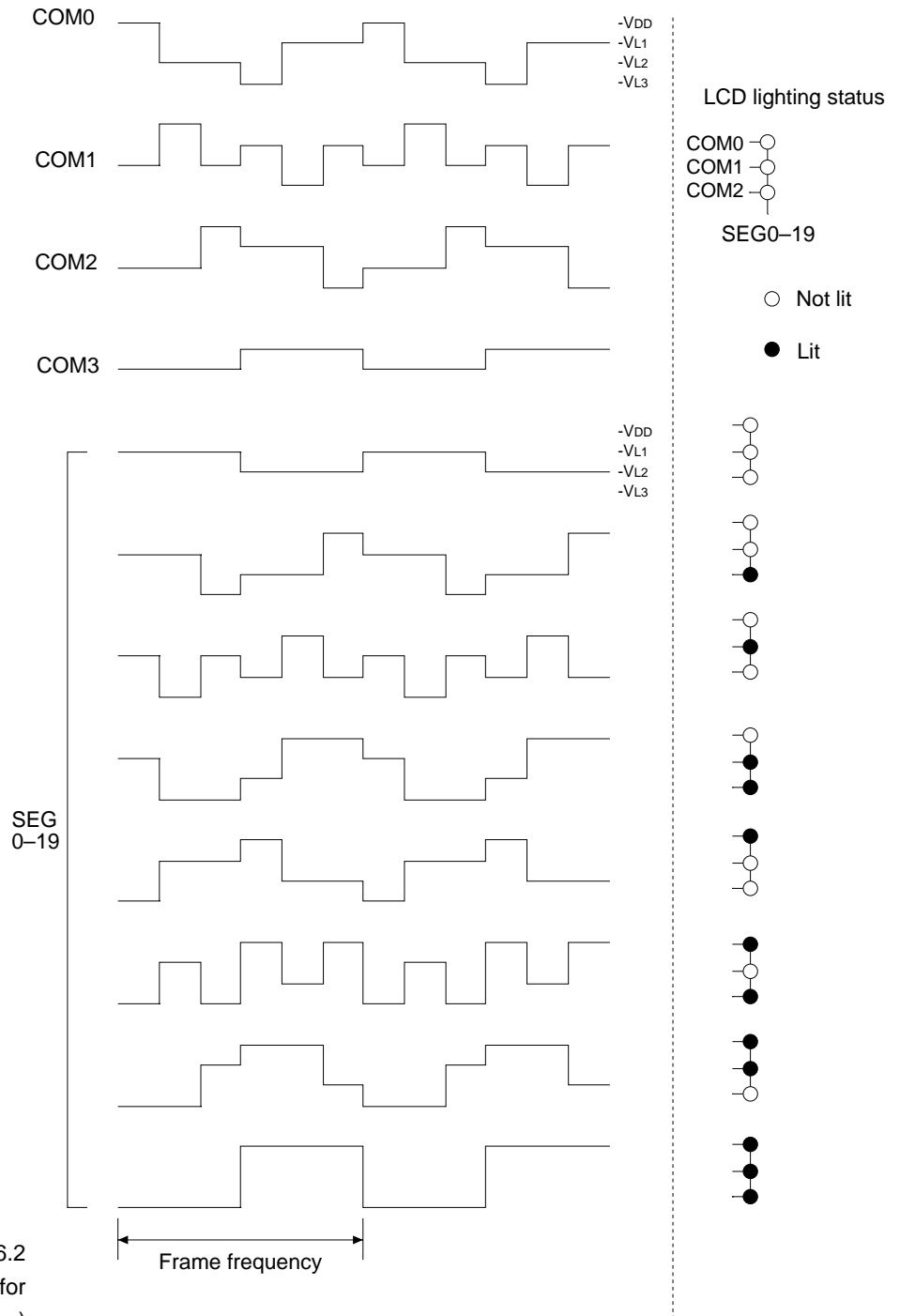


Fig. 4.6.2
Drive waveform for
1/3 duty (1/3 bias)

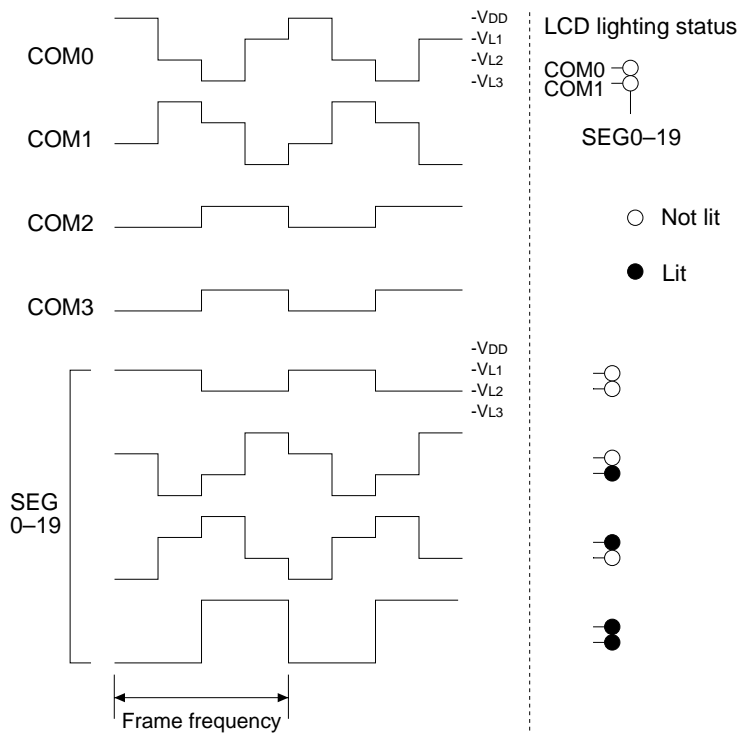


Fig. 4.6.3
Drive waveform for
1/2 duty (1/3 bias)

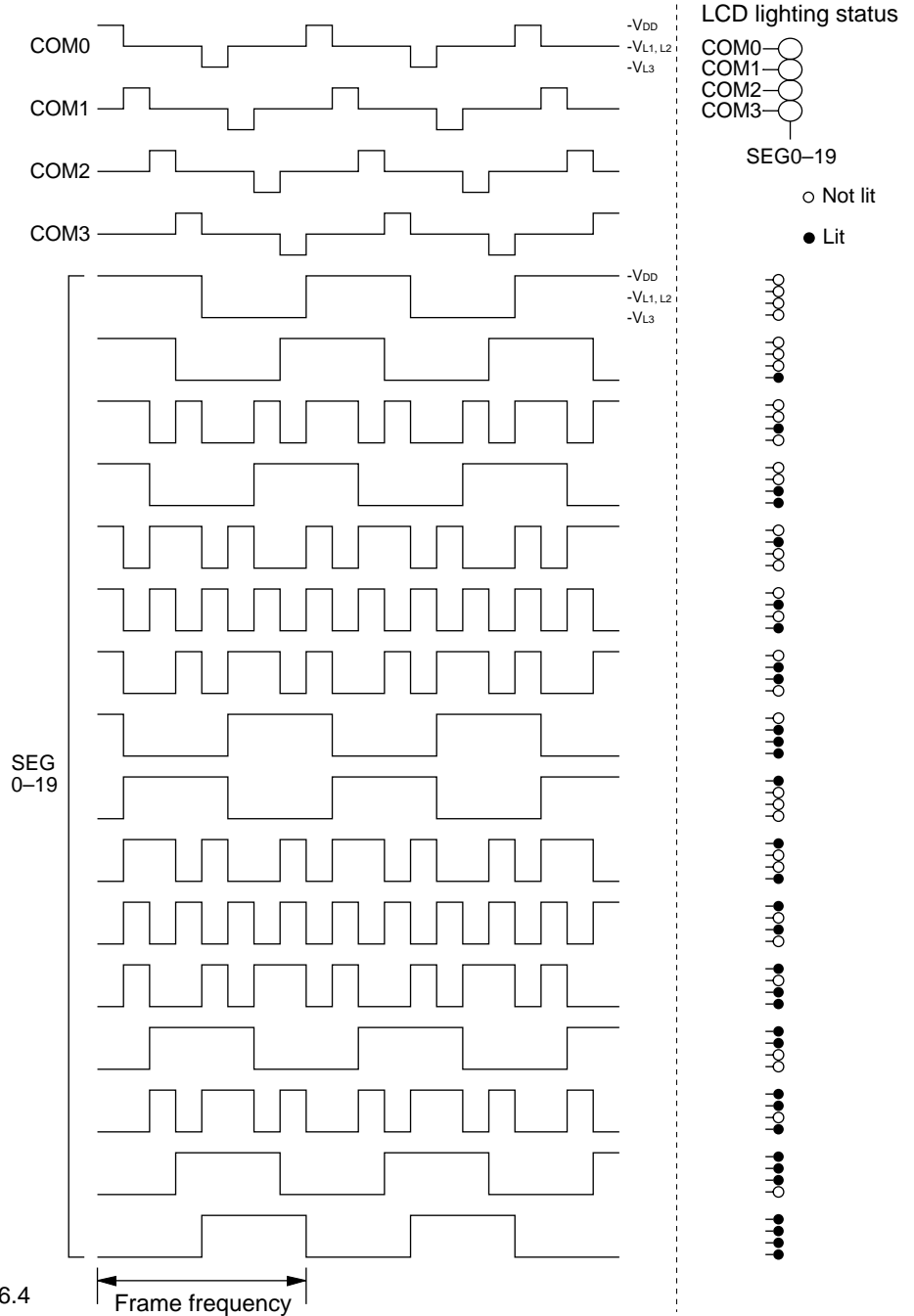
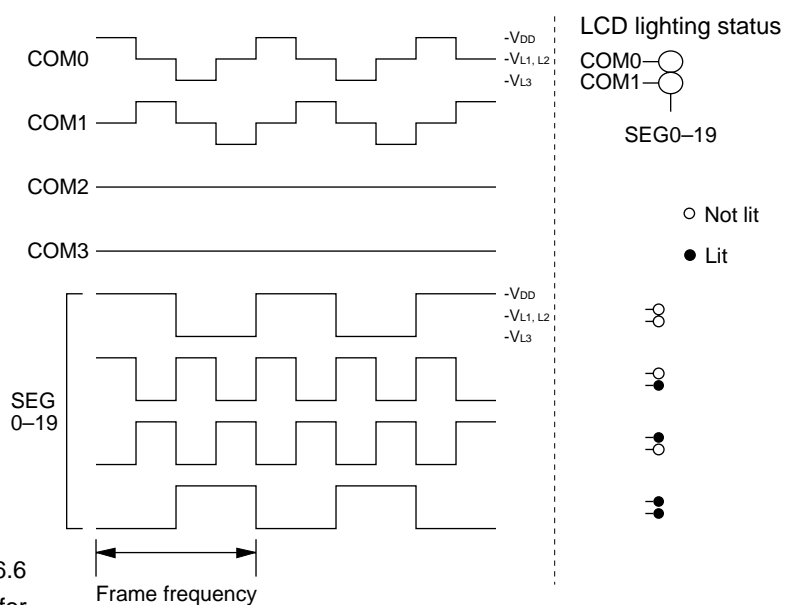
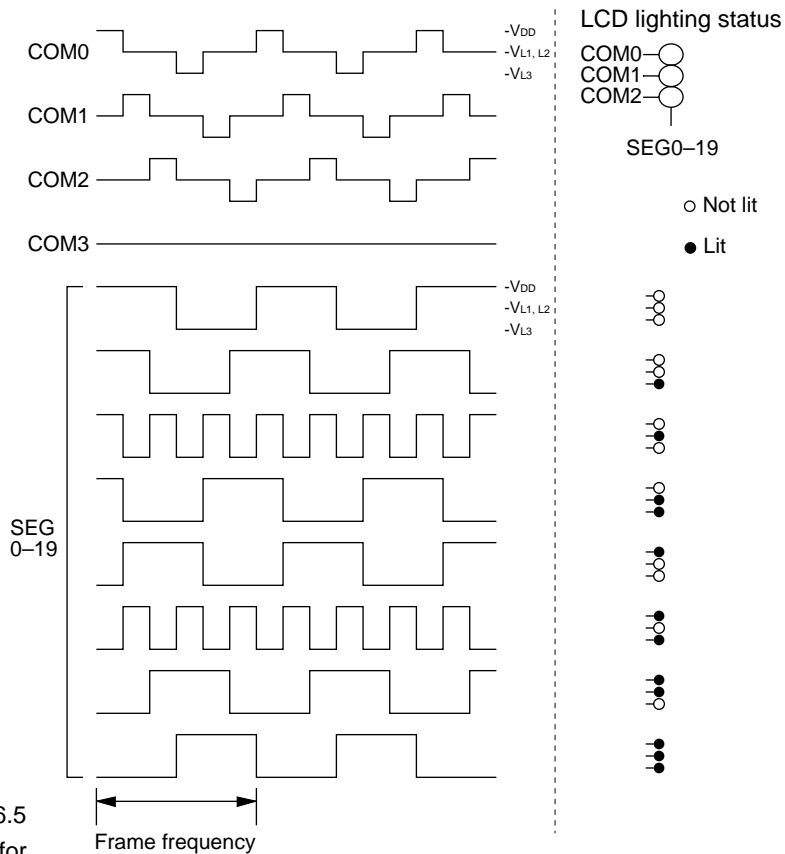


Fig. 4.6.4
Drive waveform for
1/4 duty (1/2 bias)



Cadence adjustment of oscillation frequency

In the S1C60N05 Series, the LCD drive duty can be set to 1/1 duty by software. This function enables easy adjustment (cadence adjustment) of the oscillation frequency of the OSC circuit.

The procedure to set to 1/1 duty drive is as follows:

- ① Write "1" to the CSDC register at address "0FBH D3".
- ② Write the same value to all registers corresponding to COMs 0 through 3 of the display memory.

The frame frequency is 32 Hz ($f_{OSC1}/1,024$, when $f_{OSC1} = 32.768$ kHz).

- Note**
- Even when 1/3 or 1/2 duty is selected by the mask option, the display data corresponding to all COM are valid during 1/1 duty driving. Hence, for 1/1 duty drive, set the same value for all display memory corresponding to COMs 0 through 3.
 - For cadence adjustment, set the display data corresponding to COMs 0 through 3, so that all the LCD segments go on.

Figure 4.6.7 shows the 1/1 duty drive waveform (1/3 bias).

Figure 4.6.8 shows the 1/1 duty drive waveform (1/2 bias).

Fig. 4.6.7
1/1 duty drive waveform
(1/3 bias)

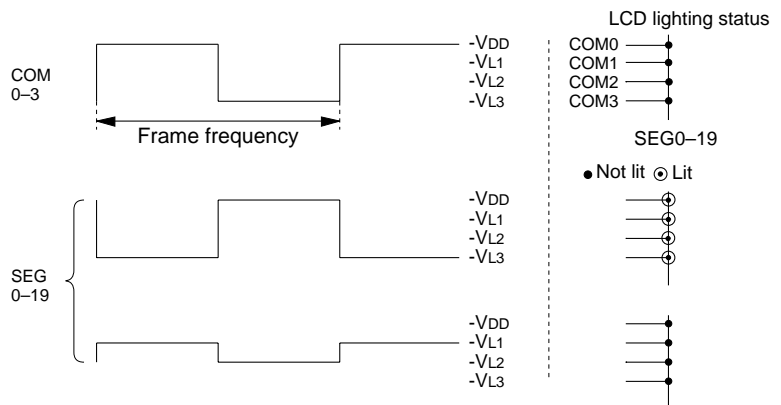
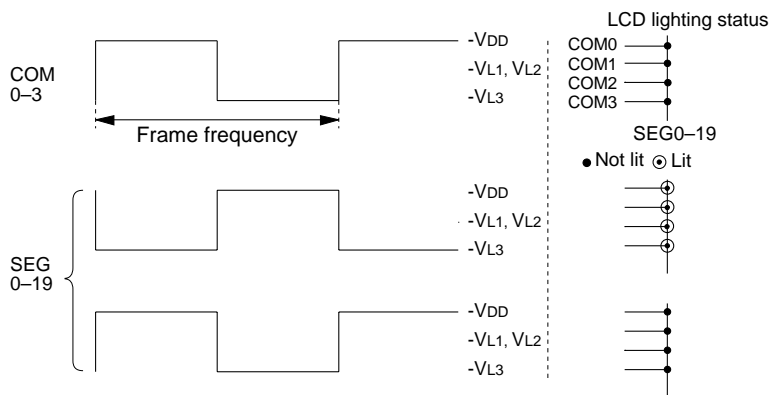


Fig. 4.6.8
1/1 duty drive waveform
(1/2 bias)



Mask option
(segment allocation)

(1) Segment allocation

As shown in Figure 4.1.1, the S1C60N05 Series display data is decided by the display data written to the display memory (write-only) at address "090H-0AFH".

The address and bits of the display memory can be made to correspond to the segment pins (SEG0-SEG19) in any combination through mask option. This simplifies design by increasing the degree of freedom with which the liquid crystal panel can be designed.

Figure 4.6.9 shows an example of the relationship between the LCD segments (on the panel) and the display memory in the case of 1/3 duty.

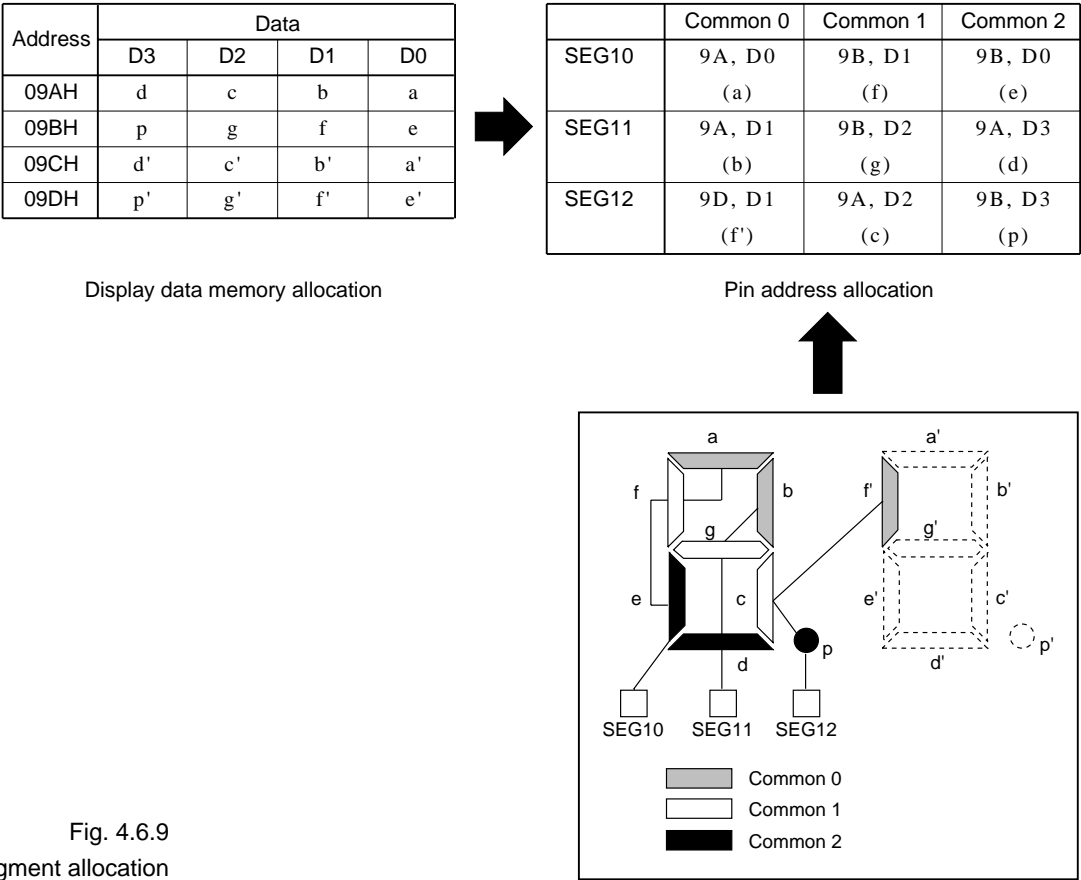


Fig. 4.6.9
Segment allocation

(2) Drive duty

According to the mask option, either 1/4, 1/3 or 1/2 duty can be selected as the LCD drive duty.

Table 4.6.1 shows the differences in the number of segments according to the selected duty.

Table 4.6.1
Differences according to
selected duty

Duty	Pins used in common	Maximum number of segments	Frame frequency (when fosc = 32 kHz)
1/4	COM0–3	80 (20 × 4)	32 Hz
1/3	COM0–2	60 (20 × 3)	42.7 Hz
1/2	COM0–1	40 (20 × 2)	32 Hz

(3) Output specification

- ① The segment pins (SEG0–SEG19) are selected by mask option in pairs for either segment signal output or DC output (VDD and VSS binary output). When DC output is selected, the data corresponding to COM0 of each segment pin is output.
- ② When DC output is selected, either complementary output or Pch open drain output can be selected for each pin by mask option.

Note The pin pairs are the combination of SEG (2*n) and SEG (2*n + 1) (where n is an integer from 0 to 9).

(4) Drive bias

For the drive bias of the S1C60N05 or the S1C60L05, either 1/3 bias or 1/2 bias can be selected by the mask option.

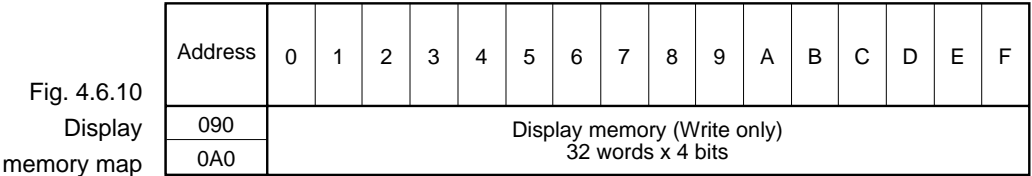
Control of LCD driver

Table 4.6.2 shows the control bits of the LCD driver and their addresses. Figure 4.6.10 shows the display memory map.

Table 4.6.2 Control bits of LCD driver

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
0FBH	CSDC	0	0	0	CSDC	0	Static	Dynamic	LCD drive switch
					0				*5
					0				*5
	R/W	R			0				*5

- *1 Initial value following initial reset
- *2 Not set in the circuit
- *3 Undefined
- *4 Reset (0) immediately after being read
- *5 Always "0" when being read
- *6 Refer to main manual



CSDC LCD drive switch (0FBH D3)
The LCD drive format can be selected with this switch.

When "1" is written: Static drive
When "0" is written: Dynamic drive
Reading: Valid

After an initial reset, dynamic drive (CSDC = "0") is selected.

Display memory (090H–0AFH)
The LCD segments are turned on or off according to this data.

When "1" is written: On
When "0" is written: Off
Reading: Invalid

By writing data into the display memory allocated to the LCD segment (on the panel), the segment can be turned on or off. After an initial reset, the contents of the display memory are undefined.

4.7 Clock Timer

Configuration of clock timer

The S1C60N05 Series has a built-in clock timer driven by the source oscillator. The clock timer is configured as a seven-bit binary counter that serves as a frequency divider taking a 256 Hz source clock from a prescaler. The four high-order bits (16 Hz–2 Hz) can be read by the software. Figure 4.7.1 is the block diagram of the clock timer.

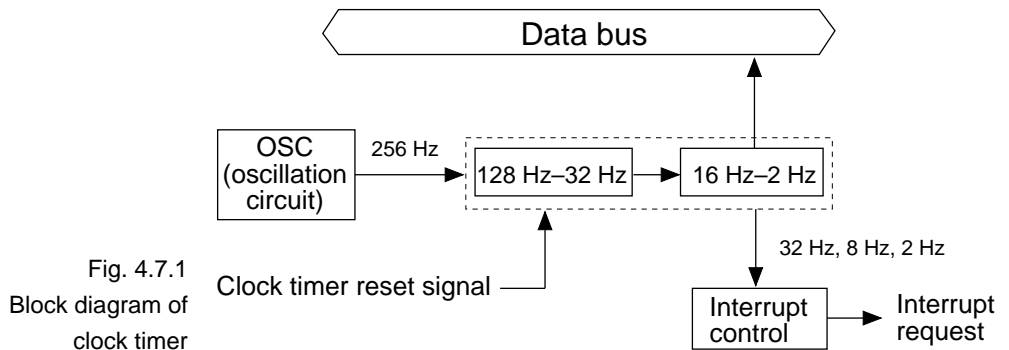


Fig. 4.7.1
Block diagram of
clock timer

Normally, this clock timer is used for all kinds of timing purpose, such as clocks.

Interrupt function

The clock timer can interrupt on the falling edge of the 32 Hz, 8 Hz, and 2 Hz signals. The software can mask any of these interrupt signals.

Figure 4.7.2 is the timing chart of the clock timer.

Address	Register bits	Frequency	Clock timer timing chart
0E3H	D0	16 Hz	
	D1	8 Hz	
	D2	4 Hz	
	D3	2 Hz	
Occurrence of 32 Hz interrupt request			
Occurrence of 8 Hz interrupt request			
Occurrence of 2 Hz interrupt request			

Fig. 4.7.2 Timing chart of the clock timer

As shown in Figure 4.7.2, an interrupt is generated on the falling edge of the 32 Hz, 8 Hz, and 2 Hz frequencies. When this happens, the corresponding interrupt event flag (IT32, IT8, IT2) is set to "1". Masking the separate interrupts can be done with the interrupt mask register (EIT32, EIT8, EIT2). However, regardless of the interrupt mask register setting, the interrupt event flags will be set to "1" on the falling edge of their corresponding signal (e.g. the falling edge of the 2 Hz signal sets the 2 Hz interrupt factor flag to "1").

Note Write to the interrupt mask register (EIT32, EIT8, EIT2) only in the DI status (interrupt flag = "0"). Otherwise, it causes malfunction.

Control of clock timer

Table 4.7.1 shows the clock timer control bits and their addresses.

Table 4.7.1 Control bits of clock timer

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
0E3H	TM3	TM2	TM1	TM0	TM3	– *3	High	Low	Clock timer data 2 Hz
					TM2	– *3	High	Low	Clock timer data 4 Hz
					TM1	– *3	High	Low	Clock timer data 8 Hz
					TM0	– *3	High	Low	Clock timer data 16 Hz
0EBH	0	EIT2	EIT8	EIT32	0	0	Enable	Mask	Interrupt mask register (clock timer) 2 Hz *5
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer) 2 Hz
	R	R/W			EIT8	0	Enable	Mask	Interrupt mask register (clock timer) 8 Hz
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer) 32 Hz
0EFH	0	IT2	IT8	IT32	0				
					IT2	0	Yes	No	Interrupt factor flag (clock timer) 2 Hz *5
					IT8	0	Yes	No	Interrupt factor flag (clock timer) 8 Hz *4
					IT32	0	Yes	No	Interrupt factor flag (clock timer) 32 Hz *4
0F9H	0	0	0	TMRST	0				*5
					0				*5
					0				*5
	R			W	TMRST	Reset	Reset	–	Clock timer reset *5

*1 Initial value following initial reset

*2 Not set in the circuit

*3 Undefined

*4 Reset (0) immediately after being read

*5 Always "0" when being read

*6 Refer to main manual

TM0–TM3 Timer data (0E3H)

The 16 Hz to 2 Hz timer data of the clock timer can be read from this register. These four bits are read-only, and write operations are invalid.

After an initial reset, the timer data is initialized to "0H".

EIT32, EIT8, EIT2 Interrupt mask registers (0EBH D0–D2)

These registers are used to mask the clock timer interrupt.

When "1" is written: Enabled

When "0" is written: Masked

Reading: Valid

The interrupt mask register bits (EIT32, EIT8, EIT2) mask the corresponding interrupt frequencies (32 Hz, 8 Hz, 2 Hz).

After an initial reset, these registers are all set to "0".

IT32, IT8, IT2 Interrupt factor flags (0EFH D0–D2)

These flags indicate the status of the clock timer interrupt.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

The interrupt factor flags (IT32, IT8, IT2) correspond to the clock timer interrupts (32 Hz, 8 Hz, 2 Hz). The software can determine from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" on the falling edge of the signal. These flags can be reset when the register is read by the software. Reading of interrupt factor flags is available at EI, but be careful in the following cases.

If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

After an initial reset, these flags are set to "0".

TMRST Clock timer reset (0F9H D0)

This bit resets the clock timer.

When "1" is written:	Clock timer reset
When "0" is written:	No operation
Reading:	Always "0"

The clock timer is reset by writing "1" to TMRST. The clock timer starts immediately after this. No operation results when "0" is written to TMRST.

This bit is write-only, and so is always "0" when read.

4.8 A/D Converter

Configuration of A/D converter

The S1C60N05 Series has a CR oscillation type A/D converter with two input channels. This A/D converter is equipped with two CR oscillation circuit systems and a counter that measures their oscillation frequency. Counted values represent connected resistance values converted into digital values. Connect a reference resistance that does not change oscillation frequency according to temperature between the RS and CS terminals and a sensor that does change resistance values according to temperature between the TH and CS terminals. Then, oscillate them alternately. The difference in the counted value can be evaluated as the difference between the respective oscillation frequencies. Therefore, various sensor circuit such as a temperature-measuring circuit using a thermistor can be easily created, for example.

The configuration of the A/D converter is shown in Figure 4.8.1.

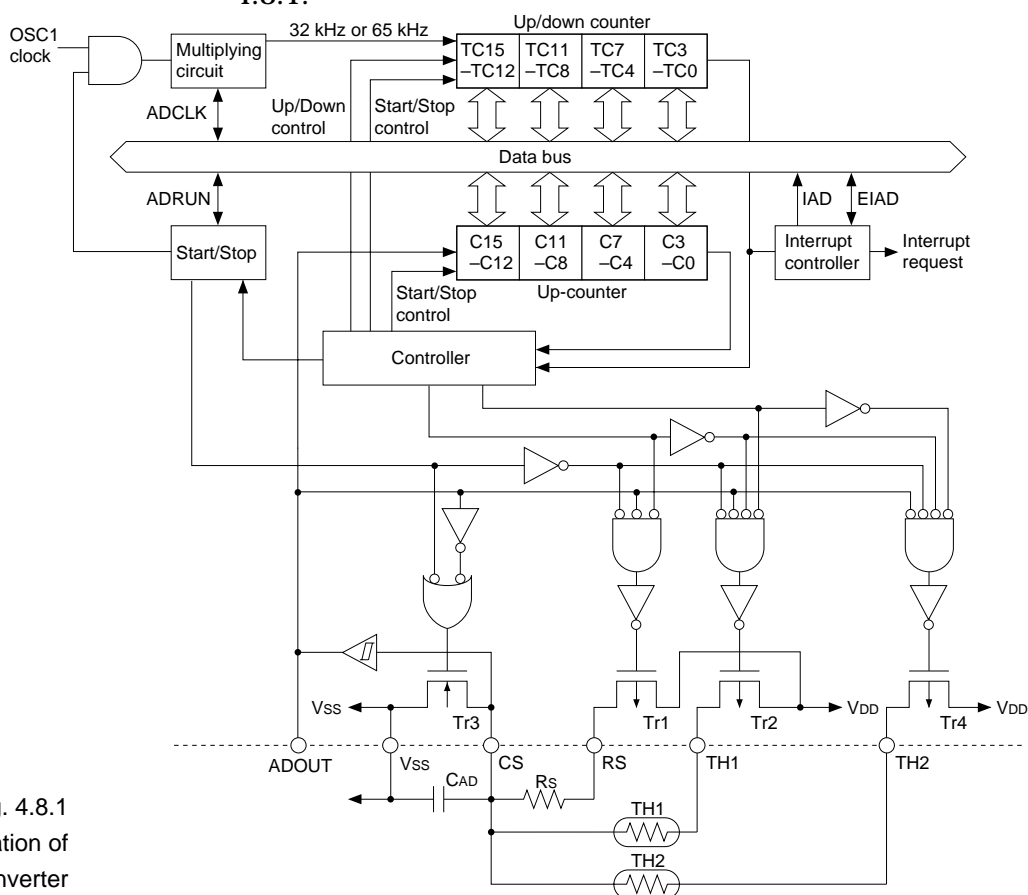


Fig. 4.8.1
Configuration of
A/D converter

Connect a reference resistance that only slightly changes resistance values according to environmental conditions between the oscillating I/O terminals RS and CS. Connect a sensor that changes resistance values between the TH and CS terminals. Furthermore, by connecting a condenser between the CS and VSS, a CR oscillation circuit is completed.

Operation of A/D converter

This A/D converter performs CR oscillation using one of the two resistances connected to external devices. Their oscillation frequency serves as a clock from which the oscillation frequency is counted. Difference in counted oscillation frequency can be evaluated in terms of the difference between the respective resistance values. Measurement results can be obtained from the changes in resistance values after correcting the difference according to the program.

(1) External resistances and condenser

Connect a sensor (a variable resistance element such as a thermistor) between the TH1/TH2 and CS terminals. Next, set the reference value of the item to be measured (e.g. reference temperature in the case of temperature measurement) and connect the reference resistance equivalent to the sensor resistance value at the above reference value between the RS and CS terminals. An element that does not change due to temperature or other environmental conditions must be used as the reference resistance.

Connect an oscillating condenser that is used for CR oscillation of both the reference resistance and the sensor between the CS and VSS terminals.

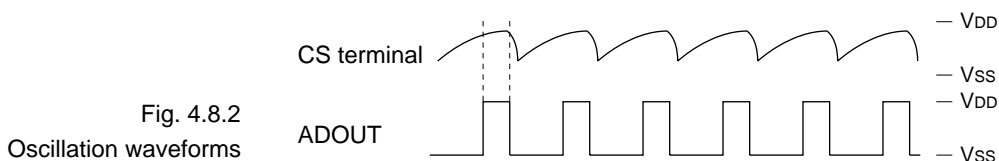
(2) Oscillation circuit

The CR oscillation circuit is designed so that either the reference resistance side or the sensor side can be operated independently by the oscillation control circuit. A/D conversion begins when "1" is written in the ADRUN register (0F1H D0). At the same time, the oscillation circuit also turns on. At first, the circuit of the reference resistance side (RS) is operated by the oscillation control circuit. Then, the circuit of the sensor side (TH1 or TH2) turns on when counting by the oscillation clock of the reference resistance is terminated.

TH1 or TH2 is controlled by the CHTH register (0F1H D3). Each circuit performs the same oscillating operation as follows (in this example, CHTH = "0", TH1 is selected): The Tr1 (Tr2) turns on first, and the condenser connected between the CS and VSS terminals is charged through the reference resistance (sensor). If the voltage level of the CS terminal decreases, the Tr1 (Tr2) turns off and the Tr3 turns on. As a result, the condenser becomes discharged, and oscillation is performed according to CR time constant. The time constant changes as the sensor resistance value fluctuates, producing a difference from the oscillation frequency of the reference resistance.

Oscillation waveforms are shaped by the Schmitt trigger and transmitted to counter. The clock transmitted to the counter is also output from the ADOUT terminal. As a result, oscillation frequency can be identified by the oscilloscope. Since this monitor has no effect on oscillation frequency, it can be used to adjust CR oscillation frequency.

Oscillation waveforms and waveforms output from the ADOUT terminal are shown in Figure 4.8.2.



(3) Counter

The A/D converter incorporates two types of 16-bit counters. One is the up-counter C0–C15 that counts the aforementioned oscillation clock, and the other is up/down counter TC0–TC15 that counts the internal clock for reference counting. Each counter permits reading and writing on a 4-bit basis.

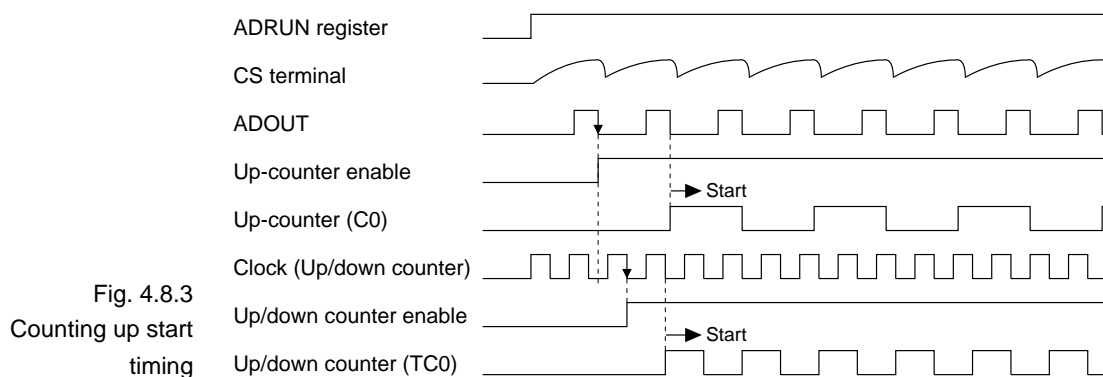
The input unit of the up/down counter TC0–TC15 incorporates a multiplying circuit so that either the OSC1 clock (Typ. 32.768 kHz) or its multiplication clock (Typ. 65.536 kHz) can be selected as an input clock.

When A/D conversion is initiated by the ADRUN register, oscillation by the reference resistance begins first, and the up-counter C0–C15 starts counting up according to the oscillation clock. At the same time, the up/down counter TC0–TC15 starts counting up.

Timing in starting oscillation and starting counting up are shown in Figure 4.8.3.

The up-counter becomes ENABLE at the falling edge of the first clock after CR oscillation is initiated and starts counting up from the falling edge of the next clock.

The up/down counter becomes ENABLE at the falling edge of the internal clock which is input immediately after the first CR oscillation clock has fallen. Then, it starts counting up from the falling edge of the next internal clock.



If the up-counter C0–C15 becomes "0000H" due to overflow, the sensor side of the oscillation circuit turns on, and the up-counter starts counting up according to the oscillation clock on the sensor side.

The up/down counter TC0–TC15 shifts to the counting-down mode at this point and starts counting down from the value measured as a result of oscillation by the reference resistance.

Timing in starting counting when oscillation is switched, is same as Figure 4.8.3.

When the up/down counter TC0–TC15 has counted down to "0000H", the counting operation of both counters and CR oscillation stops, and an interrupt occurs. At the same time, the ADRUN register is set to "0", and the A/D converter circuit stops operation completely.

The sensor is oscillated for the same period of time as the reference resistance is oscillated after the up/down counter TC0–TC15 is set to "0000H" prior to A/D conversion. Therefore, the difference in oscillation frequency can be measured from the values counted by the up-counter C0–C15.

Since the reference resistance is oscillated until the up-counter C0–C15 overflows, an appropriate initial value needs to be set before A/D conversion is started. If a smaller initial value is set, a longer counting period is possible, thereby ensuring more accurate detection. Likewise, if the input clock of the up/down counter TC0–TC15 is set at 65 kHz, the degree of precision is reduced. However, since CR oscillation frequency is normally set lower than the clock frequency of the up/down counter TC0–TC15 to ensure accurate measurement, the up/down counter TC0–TC15 may overflow while counting the oscillation frequency of the reference resistance.

If an overflow occurs, CR oscillation and A/D conversion is terminated immediately. Also in such cases, the up/down counter indicates "0000H", and interrupt occurs. However, it is impossible to judge whether the interrupt has occurred due to an overflow or normal termination. Note that correct measurement is impossible if an overflow occurs. The initial value to be set depends on the measurable range by the sensor or where to set the reference resistance value within that range.

The initial value must be set taking the above into consideration.

Convert the initial value into a complement (value subtracted from 0000H) before setting it on the up-counter C0–C15. Since the data output from the up-counter C0–C15 after A/D conversion matches data detected by the sensor, process the difference between that value and the initial value before it is converted into a complement according to the program and calculate the target value. The above operations are shown in Figure 4.8.4.

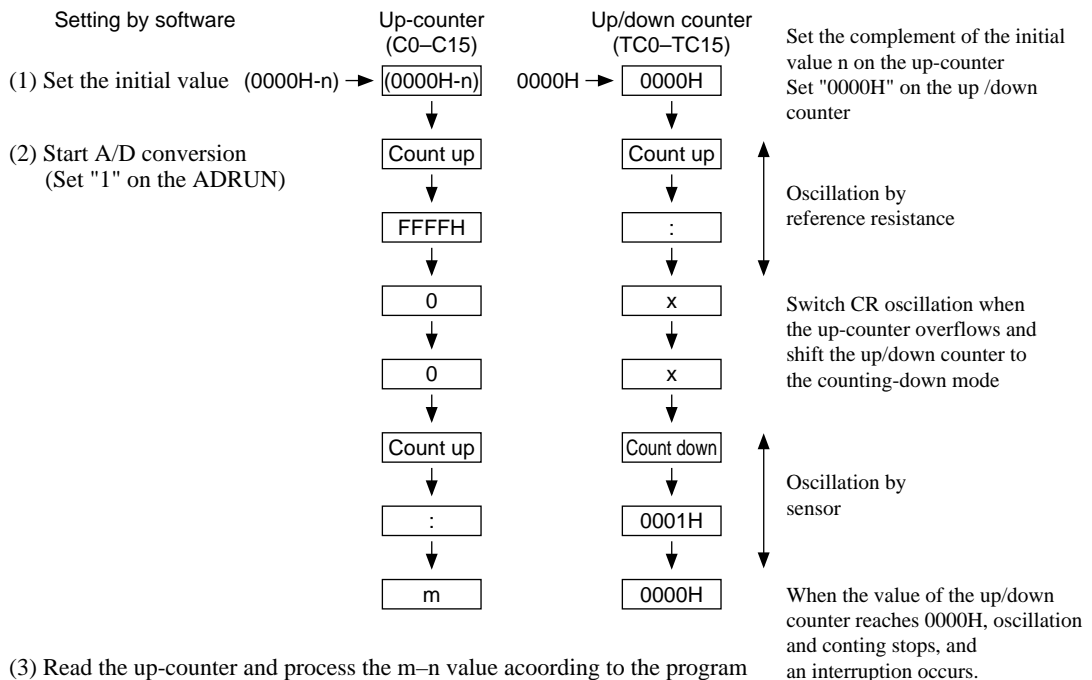


Fig. 4.8.4

Sequence of A/D conversion

- Note**
- Before setting "1" to ADRUN, an input channel must be selected from TH1 and TH2 (TH1 by default).
 - Set the initial value of the up-counter C0–C15 taking into account the measurable range and the overflow of the up/down counter TC0–TC15.
 - If the up/down counter TC0–TC15 is measured after A/D conversion, it may not indicate "0000H". This is not due to incorrect timing in terminating A/D conversion but because the counting down clock is input after the control signal is output to the up-counter to terminate counting.

Interrupt function

The A/D converter has a function which allows interrupt to occur after A/D conversion.

When the up/down counter TC0-TC15 is counted down to "0000H", both counters stop counting. The interrupt factor flag IAD is set to "1" at the falling edge of the next clock. If the up/down counter TC0-TC15 overflow during counting-up operation, the interrupt factor flag is set to "1" at the rising edge of the clock immediately after the counter reaches "0000H".

This interrupt factor allows masking by the interrupt mask register EIAD. If the EIAD is set at "1", an interrupt occurs in the CPU. If the EIAD is set at "0", the interrupt factor flag is set to "1". However, no interrupt will occur in the CPU. The interrupt factor flag is reset to "0" by a reading operation.

Timing of interrupt by the A/D converter is shown in Figure 4.8.5.

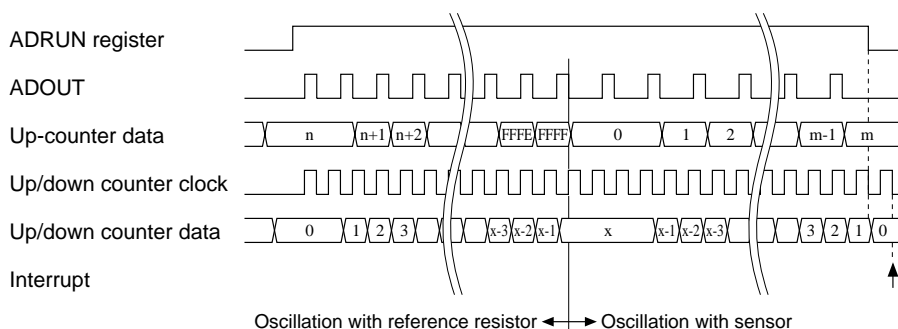


Fig. 4.8.5
Timing of A/D
converter interrupt

Usage example of the A/D converter

Temperature measurement is possible with the A/D converter in which a thermistor is used as a sensor. Elements to be connected and counter setting in the case of temperature measurement are as follows:

Example: Temperature measurement at -20°C to 70°C
 Reference resistance 49.8 kΩ
 Thermistor 50 kΩ
 Oscillating condenser 2,200 pF

When the above elements are connected, the oscillation frequency of the reference resistance becomes about 10 kHz, and the oscillation frequency of the thermistor varies within the range of about 1 kHz to 50 kHz at -20°C to 70°C. Reference resistance is adjusted to the thermistor resistance value at 25°C.

In addition, Figure 4.8.6 indicates the resistance and oscillation frequency ratio TYP at the time of A/D conversion.

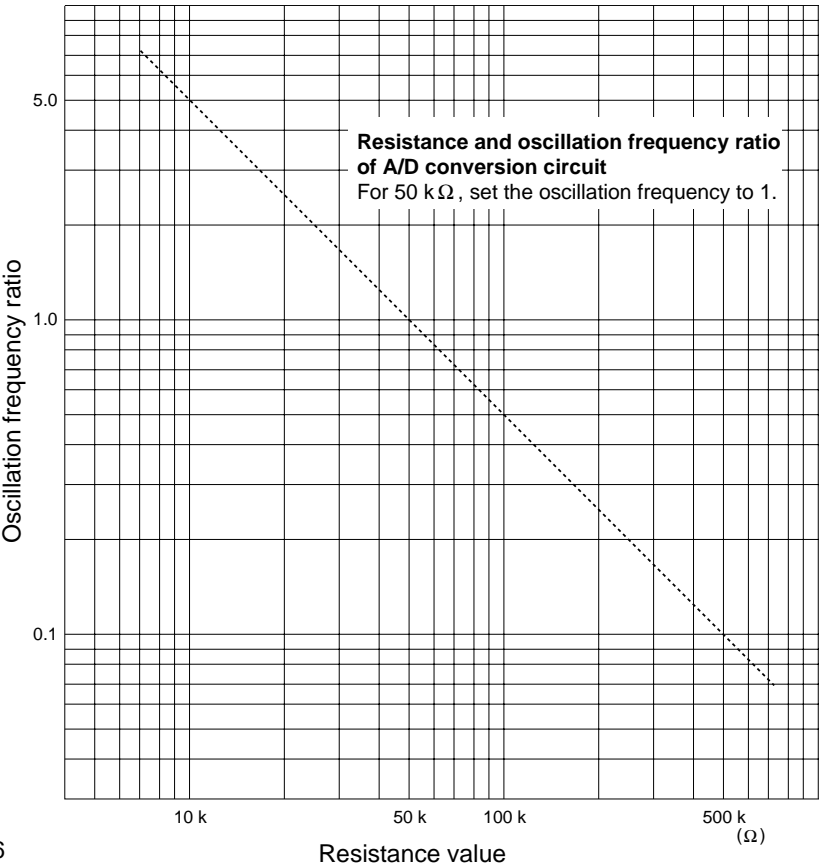


Fig. 4.8.6
Resistance and oscillation
frequency ratio

Control of A/D converter

Table 4.8.2 shows the A/D converter control bits and their addresses.

Table 4.8.2 Control bits of clock timer

Address	Register				Name	Init ^{*1}	1	0	Comment
	D3	D2	D1	D0					
0E4H	TC3	TC2	TC1	TC0	TC3	— ^{*3}	1	0	Up/down counter data TC3
					TC2	— ^{*3}	1	0	Up/down counter data TC2
	R/W				TC1	— ^{*3}	1	0	Up/down counter data TC1
					TC0	— ^{*3}	1	0	Up/down counter data TC0 (LSB)
0E5H	TC7	TC6	TC5	TC4	TC7	— ^{*3}	1	0	Up/down counter data TC7
					TC6	— ^{*3}	1	0	Up/down counter data TC6
	R/W				TC5	— ^{*3}	1	0	Up/down counter data TC5
					TC4	— ^{*3}	1	0	Up/down counter data TC4
0E6H	TC11	TC10	TC9	TC8	TC11	— ^{*3}	1	0	Up/down counter data TC11
					TC10	— ^{*3}	1	0	Up/down counter data TC10
	R/W				TC9	— ^{*3}	1	0	Up/down counter data TC9
					TC8	— ^{*3}	1	0	Up/down counter data TC8
0E7H	TC15	TC14	TC13	TC12	TC15	— ^{*3}	1	0	Up/down counter data TC15 (MSB)
					TC14	— ^{*3}	1	0	Up/down counter data TC14
	R/W				TC13	— ^{*3}	1	0	Up/down counter data TC13
					TC12	— ^{*3}	1	0	Up/down counter data TC12
0F5H	C3	C2	C1	C0	C3	— ^{*3}	1	0	Up-counter data C3
					C2	— ^{*3}	1	0	Up-counter data C2
	R/W				C1	— ^{*3}	1	0	Up-counter data C1
					C0	— ^{*3}	1	0	Up-counter data C0 (LSB)
0F6H	C7	C6	C5	C4	C7	— ^{*3}	1	0	Up-counter data C7
					C6	— ^{*3}	1	0	Up-counter data C6
	R/W				C5	— ^{*3}	1	0	Up-counter data C5
					C4	— ^{*3}	1	0	Up-counter data C4
0F7H	C11	C10	C9	C8	C11	— ^{*3}	1	0	Up-counter data C11
					C10	— ^{*3}	1	0	Up-counter data C10
	R/W				C9	— ^{*3}	1	0	Up-counter data C9
					C8	— ^{*3}	1	0	Up-counter data C8
0F8H	C15	C14	C13	C12	C15	— ^{*3}	1	0	Up-counter data C15 (MSB)
					C14	— ^{*3}	1	0	Up-counter data C14
	R/W				C13	— ^{*3}	1	0	Up-counter data C13
					C12	— ^{*3}	1	0	Up-counter data C12
0F1H	CHTH	0	0	ADRUN	CHTH	0	TH2	TH1	A/D channel selection
					0				^{*5}
	R/W	R		R/W	ADRUN	0	Start	Stop	A/D conversion Start/Stop
0FEH	0	0	0	ADCLK	0				^{*5}
					0				^{*5}
	R			R/W	ADCLK	0	65 kHz	32 kHz	A/D clock selection 65 kHz/32 kHz
0ECH	0	0	0	EIAD	0				^{*5}
					0				^{*5}
	R			R/W	EIAD	0	Enable	Mask	Interrupt mask register (A/D)
0F0H	0	0	0	IAD	0				^{*5}
					0				^{*5}
	R				IAD	0	Yes	No	Interrupt factor flag (A/D)

^{*1} Initial value following initial reset

^{*2} Not set in the circuit

^{*3} Undefined

^{*4} Reset (0) immediately after being read

^{*5} Always "0" when being read

^{*6} Refer to main manual

TC0–TC15 Up/down counter (0E4H–0E7H)

Writing and reading is possible on a 4-bit basis by the up/down counter that is used to adjust the CR oscillation time between the reference resistance and the variable resistance elements.

The up/down counter counts up during oscillation of the reference resistance and counts down from the value it reached when counting up to "0000H" during oscillation of the sensor.

"0000H" needs to be entered in the counter prior to A/D conversion in order to adjust the counting time of both counts.

After an initial reset, data in this counter become indefinite.

C0–C15 Up-counter (0F5H–0F8H)

This counter counts up according to the CR oscillation clock. It permits writing and reading on a 4-bit basis.

The complement of the number of clocks to be counted by the oscillation of the reference resistance, must be entered in this counter prior to A/D conversion.

If A/D conversion is initiated, the counter counts up from the set initial value, first according to the oscillation clock of the reference resistance. When the counter reaches "0000H" due to overflow, the oscillation of the reference resistance stops, and the sensor starts oscillating. The counter continues counting according to the sensor oscillation clock.

Counting time during the oscillation of the reference resistance is calculated by the up/down counter TC0–TC15. Up-counter C0–C15 stops counting when the same period of time elapses. Difference from the reference resistance can be evaluated from the value indicated by the counter when it stops. Calculate the target value by processing the above difference according to the program.

Measurable range and the overflow of the up/down counter TC0–TC15 must be taken into account when setting an initial value to be entered prior to A/D conversion.

After an initial reset, data in this counter become indefinite.

ADCLK Input clock selection (0FEH D0)

Select the input clock of the up/down counter TC0–TC15.

When "1" is written: 65 kHz

When "0" is written: 32 kHz

Reading: Valid

Select the output clock of the multiplying circuit for the counting operation of the up/down counter TC0–TC15.

When "1" is written in the ADCLK, 65 kHz, a multitude of the OSC1 clock is selected. When "0" is written, the OSC1 clock is selected at 32 kHz.

If 65 kHz is selected, A/D conversion becomes more accurate. However, the initial value must be set on the up-counter C0–C15 so that the up/down counter TC0–TC15 will not overflow while CR oscillation is being counted. After an initial reset, ADCLK is set to "0".

ADRUN A/D conversion START/STOP (0F1H D0)

Start A/D conversion.

When "1" is written: A/D conversion starts

When "0" is written: A/D conversion stops

Reading: Valid

When "1" is written in the ADRUN, A/D conversion begins.

The register remains at "1" during A/D conversion and is set to "0" when A/D conversion is terminated.

When "0" is written in the ADRUN during A/D conversion, A/D conversion is paused.

ADRUN is set to "0" at initial reset, when the up/down counter overflows or when measurement is finished.

CHTH A/D channel selection (0F1H D3)

Select an A/D converter channel.

When "1" is written: TH2 is selected

When "0" is written: TH1 is selected

Reading: Valid

Before running the A/D converter, either TH1 or TH2 must be selected as an input channel.

After an initial reset, CHTH is set to "0".

EIAD Interrupt mask register (0ECH D0)

Select whether to mask interrupt with the A/D converter.

When "1" is written: Enable

When "0" is written: Mask

Reading: Valid

The A/D converter interrupt is permitted when "1" is written in the EIAD. When "0" is written, interrupt is masked.

After an initial reset, this register is set to "0".

IAD Interrupt factor flag (0F0H D0)

This flag indicates interrupt caused by the A/D converter.

When "1" is read: Interrupt has occurred

When "0" is read: Interrupt has not occurred

Writing: Invalid

IAD is set to "1" when A/D conversion is terminated (when the up/down counter counted up or down to "0000H"). From the status of this flag, the software can decide whether an A/D converter interrupt has occurred.

This flag is reset when the software has read it.

Reading of interrupt factor flag is available at EI, but be careful in the following cases.

If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

After an initial reset, this flag is set to "0".

4.9 Heavy Load Protection Function

Operation of heavy load protection function

The S1C60N05 Series has a heavy load protection function for when the battery load becomes heavy and the supply voltage drops, such as when an external buzzer sounds or an external lamp lights. This function works in the heavy load protection mode.

The normal mode changes to the heavy load protection mode in the following case:

- When the software changes the mode to the heavy load protection mode (HLMOD = "1")

In the heavy load protection mode, the internally regulated voltage is switched to the high-stability mode from the low current consumption mode. Consequently, more current is consumed in the heavy load protection mode than in the normal mode. Unless necessary, do not select the heavy load protection mode with the software.

Control of heavy load protection function

Table 4.9.1 shows the control bits and their addresses for the heavy load protection function.

Table 4.9.1 Control bits for heavy load protection function

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
0FAH	HLMOD	0	0	0	HLMOD	0	Heavy	Normal	Heavy load protection mode register
					0				*5
	R/W	R			0				*5
					0				*5

- *1 Initial value following initial reset
- *2 Not set in the circuit
- *3 Undefined
- *4 Reset (0) immediately after being read
- *5 Always "0" when being read
- *6 Refer to main manual

HLMOD Heavy load protection mode on/off (0FAH D3)

When "1" is written: Heavy load protection mode on
When "0" is written: Heavy load protection mode off
Reading: Valid

When HLMOD is set to "1", the IC enters the heavy load protection mode.

In the heavy load protection mode, the consumed current becomes larger. Unless necessary, do not select the heavy load protection mode with the software.

4.10 Interrupt and HALT

The S1C60N05 Series provides the following interrupt settings, each of which is maskable.

External interrupt: Input interrupt (one)
 Internal interrupt: Timer interrupt (one)
 A/D converter interrupt (one)

To enable interrupts, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable). When an interrupt occurs, the interrupt flag is automatically reset to "0" (DI) and interrupts after that are inhibited.

When a HALT instruction is input, the CPU operating clock stops and the CPU enters the halt state. The CPU is reactivated from the halt state when an interrupt request occurs.

Figure 4.10.1 shows the configuration of the interrupt circuit.

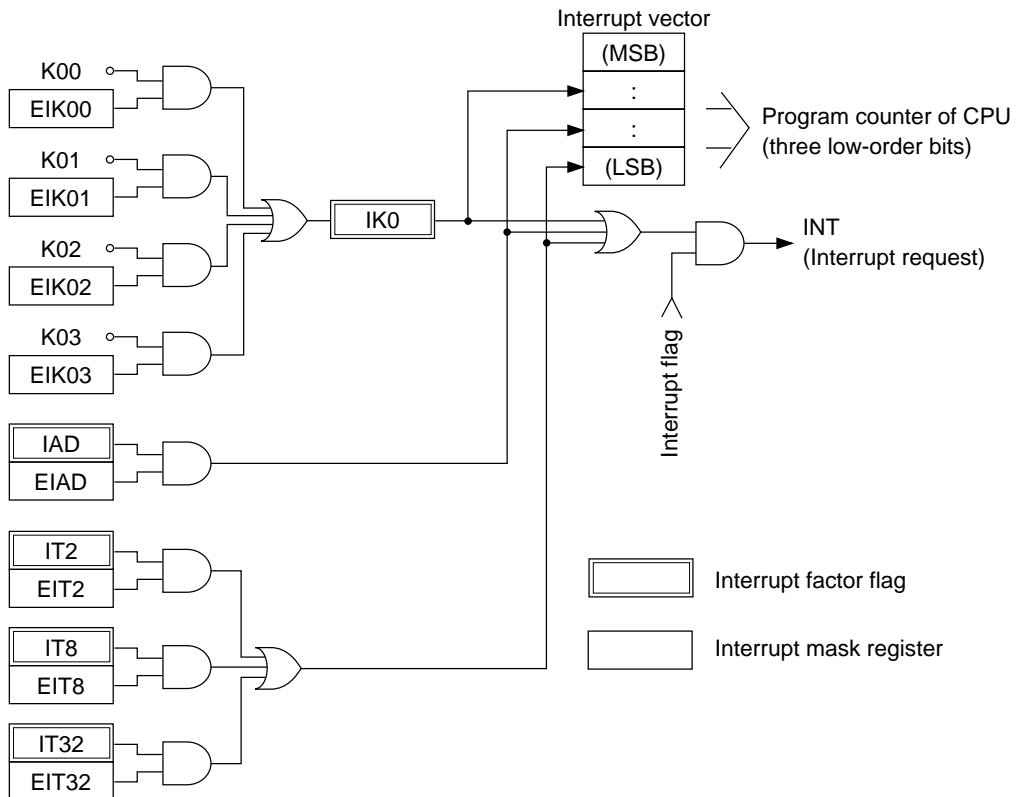


Fig. 4.10.1
 Configuration of
 interrupt circuit

Interrupt factors

Table 4.10.1 shows the factors that generate interrupt requests.

The interrupt factor flags are set to "1" depending on the corresponding interrupt factors.

The CPU is interrupted when the following two conditions occur and an interrupt factor flag is set to "1".

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is a read-only register, but can be reset to "0" when the register data is read.

After an initial reset, the interrupt factor flags are reset to "0".

Note Reading of interrupt factor flags is available at EI, but be careful in the following cases.

If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

Table 4.10.1
Interrupt factors

Interrupt factor	Interrupt factor flag
Colck timer 2 Hz falling edge	IT2 (0EFH D2)
Colck timer 8 Hz falling edge	IT8 (0EFH D1)
Colck timer 32 Hz falling edge	IT32 (0EFH D0)
A/D converter A/D conversion completion	IAD (0F0H D0)
Input data (K00–K03) Rising edge	IK0 (0EDH D0)

Specific masks and factor flags for interrupt

The interrupt factor flags can be masked by the corresponding interrupt mask registers. The interrupt mask registers are read/write registers. They are enabled (interrupt enabled) when "1" is written to them, and masked (interrupt disabled) when "0" is written to them. After an initial reset, the interrupt mask register is set to "0".

Table 4.10.2 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.10.2
Interrupt mask registers and
interrupt factor flags

Interrupt mask register		Interrupt factor flag	
EIT2	(0EBH D2)	IT2	(0EFH D2)
EIT8	(0EBH D1)	IT8	(0EFH D1)
EIT32	(0EBH D0)	IT32	(0EFH D0)
EIAD	(0ECH D0)	IAD	(0F0H D0)
EIK03*	(0E8H D3)	IK0	(0EDH D0)
EIK02*	(0E8H D2)		
EIK01*	(0E8H D1)		
EIK00*	(0E8H D0)		

* There is an interrupt mask register for each input port pin.

Interrupt vectors

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is suspended, interrupt processing is executed in the following order:

- ① The address data (value of the program counter) of the program step to be executed next is saved on the stack (RAM).
- ② The interrupt request causes the value of the interrupt vector (page 1, 01H-07H) to be loaded into the program counter.
- ③ The program at the specified address is executed (execution of interrupt processing routine).

Note The processing in steps 1 and 2, above, takes 12 cycles of the CPU system clock.

Control of interrupt

Table 4.10.3 shows the interrupt control bits and their addresses.

Table 4.10.3 Interrupt control bits

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
0E8H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register K03
					EIK02	0	Enable	Mask	Interrupt mask register K02
	R/W				EIK01	0	Enable	Mask	Interrupt mask register K01
					EIK00	0	Enable	Mask	Interrupt mask register K00
0EBH	0	EIT2	EIT8	EIT32	0	0	Enable	Mask	Interrupt mask register (clock timer) 2 Hz *5
	R	R/W			EIT8	0	Enable	Mask	Interrupt mask register (clock timer) 8 Hz
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer) 32 Hz
0ECH	0	0	0	EIAD	0				*5
					0				*5
	R			R/W	EIAD	0	Enable	Mask	Interrupt mask register (A/D) *5
0EDH	0	0	0	IK0	0				*5
					0				*5
	R				0	0	Yes	No	Interrupt factor flag (K00–K03) *5
0EFH	0	IT2	IT8	IT32	IK0	0	Yes	No	Interrupt factor flag (K00–K03) *4
					0				*5
					IT2	0	Yes	No	Interrupt factor flag (clock timer) 2 Hz *4
					IT8	0	Yes	No	Interrupt factor flag (clock timer) 8 Hz *4
0F0H					IT32	0	Yes	No	Interrupt factor flag (clock timer) 32 Hz *4
	0	0	0	IAD	0				*5
					0				*5
	R				0	0	Yes	No	Interrupt factor flag (A/D) *4

*1 Initial value following initial reset

*2 Not set in the circuit

*3 Undefined

*4 Reset (0) immediately after being read

*5 Always "0" when being read

*6 Refer to main manual

EIT32, EIT8, EIT2 Interrupt mask registers (0EBH D0–D2)

IT32, IT8, IT2 Interrupt factor flags (0EFH D0–D2)

See 4.7, "Clock Timer".

EIAD Interrupt mask register (0ECH D0)

IAD Interrupt factor flag (0F0H D0)

See 4.8, "A/D Converter".

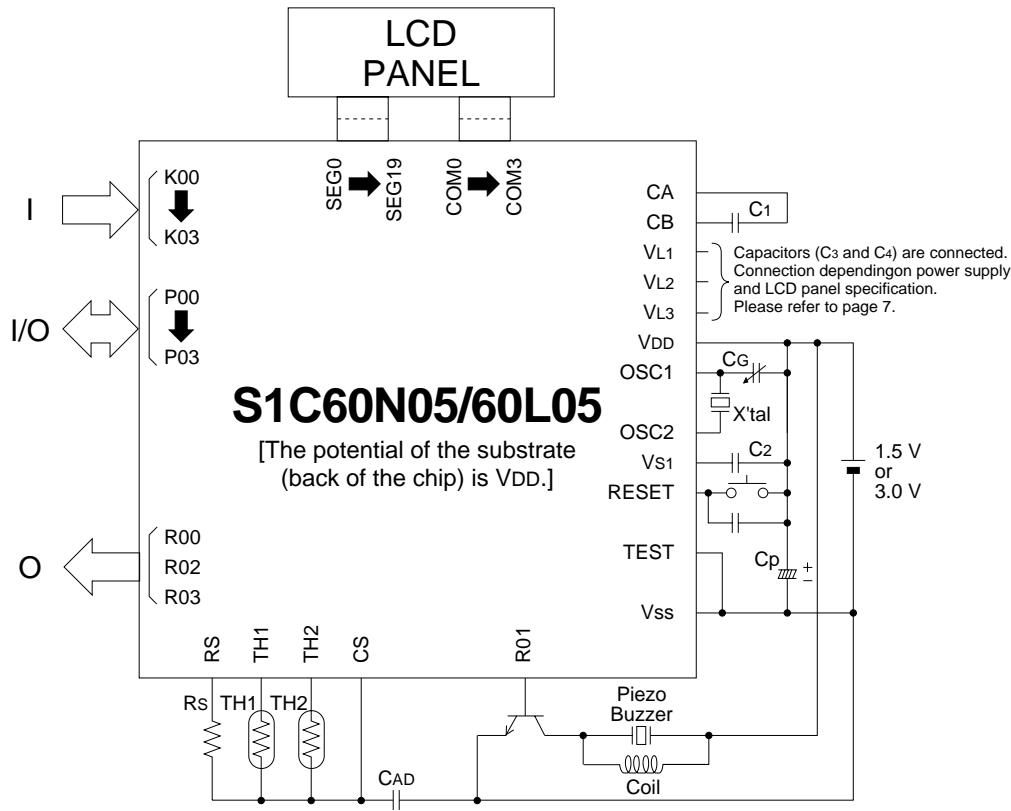
EIK00–EIK03 Interrupt mask registers (0E8H)

IK0 Interrupt factor flag (0EDH D0)

See 4.3, "Input Ports".

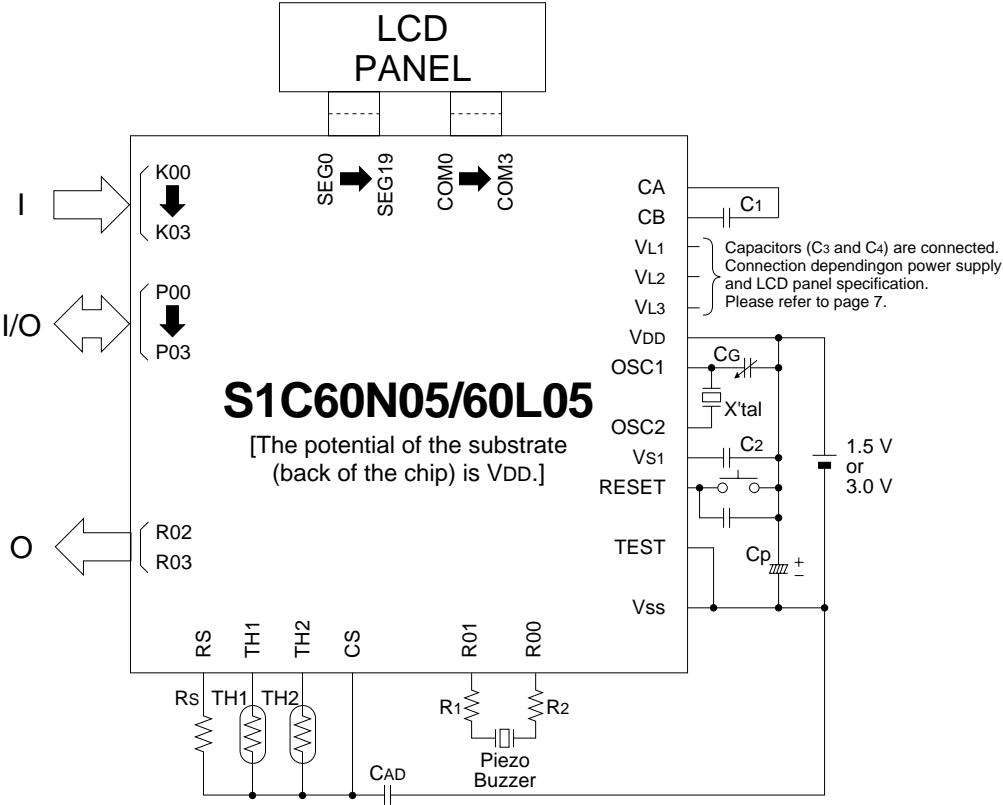
CHAPTER 5 BASIC EXTERNAL WIRING DIAGRAM

(1) Piezo Buzzer Single Terminal Driving



X'tal	Crystal oscillator	32,768 Hz	CI(MAX) = 35 kΩ
Cg	Trimmer capacitor	5–25 pF	
C1, C2, C3, C4	Capacitor	0.1 μF	
Cp	Capacitor	3.3 μF	
TH1, TH2	Thermistor	50 kΩ	
Rs	Resistor	49.8 kΩ	
CAD	Capacitor	2,200 pF	

(2) Piezo Buzzer Direct Driving



X'tal	Crystal oscillator	32,768 Hz CI(MAX) = 35 kΩ
Cg	Trimmer capacitor	5–25 pF
C1, C2, C3, C4	Capacitor	0.1 μF
Cp	Capacitor	3.3 μF
TH1, TH2	Thermistor	50 kΩ
Rs	Resistor	49.8 kΩ
R1, R2	Resistor	100 Ω
CAD	Capacitor	2,200 pF

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Rating

S1C60N05

(V_{DD}=0V)

Item	Symbol	Rated value	Unit
Power voltage	V _{SS}	-5.0 to 0.5	V
Input voltage (1)	V _I	V _{SS} -0.3 to 0.5	V
Input voltage (2)	V _I OSC	V _{SS} -0.3 to 0.5	V
Operating temperature	T _{opr}	-20 to 70	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temperature / Time	T _{sol}	260°C, 10sec (lead section)	—
Allowable dissipation ^{*1}	P _D	250	mW

^{*1} In case of QFP6-60 pin plastic package

S1C60L05

(V_{DD}=0V)

Item	Symbol	Rated value	Unit
Power voltage	V _{SS}	-5.0 to 0.5	V
Input voltage (1)	V _I	V _{SS} -0.3 to 0.5	V
Input voltage (2)	V _I OSC	V _{SS} -0.3 to 0.5	V
Operating temperature	T _{opr}	-20 to 70	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temperature / Time	T _{sol}	260°C, 10sec (lead section)	—
Allowable dissipation ^{*1}	P _D	250	mW

^{*1} In case of QFP6-60 pin plastic package

6.2 Recommended Operating Conditions

S1C60N05

(Ta=-20 to 70°C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Power voltage	VSS	VDD=0V	-3.5	-3.0	-1.8	V
Oscillation frequency	fOSC1	Crystal oscillation		32,768		Hz
	fOSC2	CR oscillation, R=420kΩ		65	80	kHz
Booster capacitor	C1		0.1			μF
Capacitor between VDD and VS1	C2		0.1			μF

S1C60L05

(Ta=-20 to 70°C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Power voltage	VSS	VDD=0V *1	-2.0	-1.5	-1.2	V
Oscillation frequency	fOSC1	Crystal oscillation		32,768		Hz
	fOSC2	CR oscillation, R=420kΩ		65	80	kHz
Booster capacitor	C1		0.1			μF
Capacitor between VDD and VS1	C2		0.1			μF

*1 When there is no software control during CR oscillation or crystal oscillation.

6.3 DC Characteristics

S1C60N05

Unless otherwise specified

VDD=0 V, VSS=-3.0 V, fosc=32,768 Hz, Ta=25°C, VS1, VL1, VL2 and VL3 are internal voltages, and C1=C2=0.1 μF

Item	Symbol	Condition	Min	Typ	Max	Unit
High level input voltage (1)	VIH1	K00-K03, P00-P03	0.2•Vss		0	V
High level input voltage (2)	VIH2	RESET, TEST	0.15•Vss		0	V
Low level input voltage (1)	VIL1	K00-K03, P00-P03	Vss		0.8•Vss	V
Low level input voltage (2)	VIL2	RESET, TEST	Vss		0.85•Vss	V
High level input current (1)	IIH1	VIH1=0V Without pull down resistor	0		0.5	μA
High level input current (2)	IIH2	VIH2=0V With pull down resistor	10		40	μA
High level input current (3)	IIH3	VIH3=0V With pull down resistor	30		100	μA
Low level input current	IIL	VIL=Vss	-0.5		0	μA
High level output current (1)	IOH1	VOH1=0.1•Vss			-1.0	mA
High level output current (2)	IOH2	VOH2=0.1•Vss (built-in protection resistance)			-1.0	mA
High level output current (3)	IOH3	VOH3=-1.0V			-1.0	mA
Low level output current (1)	IOL1	VOL1=0.9•Vss	3.0			mA
Low level output current (2)	IOL2	VOL2=0.9•Vss (built-in protection resistance)	3.0			mA
Low level output current (3)	IOL3	VOL3=-2.0V	3.0			mA
Common output current	IOH4	VOH4=-0.05V	3		-3	μA
	IOL4	VOL4=VL3+0.05V				μA
Segment output current (during LCD output)	IOH5	VOH5=-0.05V	3		-3	μA
	IOL5	VOL5=VL3+0.05V				μA
Segment output current (during DC output)	IOH6	VOH6=0.1•Vss	300		-300	μA
	IOL6	VOL6=0.9•Vss				μA

S1C60L05

Unless otherwise specified

$V_{DD}=0\text{ V}$, $V_{SS}=-1.5\text{ V}$, $f_{osc}=32,768\text{ Hz}$, $T_a=25^{\circ}\text{C}$, V_{S1} , V_{L1} , V_{L2} and V_{L3} are internal voltages, and $C_1=C_2=0.1\text{ }\mu\text{F}$

Item	Symbol	Condition	Min	Typ	Max	Unit
High level input voltage (1)	V_{IH1}	K00–K03, P00–P03	$0.2 \cdot V_{SS}$		0	V
High level input voltage (2)	V_{IH2}	RESET, TEST	$0.15 \cdot V_{SS}$		0	V
Low level input voltage (1)	V_{IL1}	K00–K03, P00–P03	V_{SS}		$0.8 \cdot V_{SS}$	V
Low level input voltage (2)	V_{IL2}	RESET, TEST	V_{SS}		$0.85 \cdot V_{SS}$	V
High level input current (1)	I_{IH1}	$V_{IH1}=0\text{V}$ Without pull down resistor	0		0.5	μA
High level input current (2)	I_{IH2}	$V_{IH2}=0\text{V}$ With pull down resistor	5		20	μA
High level input current (3)	I_{IH3}	$V_{IH3}=0\text{V}$ With pull down resistor	9.0		100	μA
Low level input current	I_{IL}	$V_{IL}=V_{SS}$	-0.5		0	μA
High level output current (1)	I_{OH1}	$V_{OH1}=0.1 \cdot V_{SS}$			-200	μA
High level output current (2)	I_{OH2}	$V_{OH2}=0.1 \cdot V_{SS}$ (built-in protection resistance)			-200	μA
High level output current (3)	I_{OH3}	$V_{OH3}=-0.5\text{V}$			-200	μA
Low level output current (1)	I_{OL1}	$V_{OL1}=0.9 \cdot V_{SS}$	700			μA
Low level output current (2)	I_{OL2}	$V_{OL2}=0.9 \cdot V_{SS}$ (built-in protection resistance)	700			μA
Low level output current (3)	I_{OL3}	$V_{OL3}=-1.0\text{V}$	700			μA
Common output current	I_{OH4}	$V_{OH4}=-0.05\text{V}$			-3	μA
	I_{OL4}	$V_{OL4}=V_{L3}+0.05\text{V}$	3			μA
Segment output current (during LCD output)	I_{OH5}	$V_{OH5}=-0.05\text{V}$			-3	μA
	I_{OL5}	$V_{OL5}=V_{L3}+0.05\text{V}$	3			μA
Segment output current (during DC output)	I_{OH6}	$V_{OH6}=0.1 \cdot V_{SS}$			-100	μA
	I_{OL6}	$V_{OL6}=0.9 \cdot V_{SS}$	130			μA

6.4 Analog Circuit Characteristics and Power Current Consumption

S1C60N05 (Normal Operating Mode)

Unless otherwise specified

$V_{DD}=0$ V, $V_{SS}=-3.0$ V, $f_{osc}=32,768$ Hz, $T_a=25^{\circ}\text{C}$, $C_G=25$ pF, V_{S1} , V_{L1} , V_{L2} and V_{L3} are internal voltages, and $C_1=C_2=0.1$ μF

(During A/D conversion: $R_S=49.8$ k Ω , $T_H=50$ k Ω , $C_{AD}=2,200$ pF)

Item	Symbol	Condition	Min	Typ	Max	Unit
Internal voltage	V_{L1}	Connect $1\text{M}\Omega$ load resistor between V_{DD} and V_{L1} (without panel load)	$1/2 \cdot V_{L2}$ -0.1		$1/2 \cdot V_{L2}$ $\times 0.9$	V
	V_{L2}	Connect $1\text{M}\Omega$ load resistor between V_{DD} and V_{L2} (without panel load)		V_{SS}		V
	V_{L3}	Connect $1\text{M}\Omega$ load resistor between V_{DD} and V_{L3} (without panel load)	$3/2 \cdot V_{L2}$ -0.1		$3/2 \cdot V_{L2}$ $\times 0.9$	V
Power current consumption	IOP	During HALT		0.8	1.4	μA
		During execution		1.5	5.0	μA
		During A/D conversion (HALT)		30	40	μA

S1C60N05 (Heavy Load Protection Mode)

Unless otherwise specified

$V_{DD}=0$ V, $V_{SS}=-3.0$ V, $f_{osc}=32,768$ Hz, $T_a=25^{\circ}\text{C}$, $C_G=25$ pF, V_{S1} , V_{L1} , V_{L2} and V_{L3} are internal voltages, and $C_1=C_2=0.1$ μF

(During A/D conversion: $R_S=49.8$ k Ω , $T_H=50$ k Ω , $C_{AD}=2,200$ pF)

Item	Symbol	Condition	Min	Typ	Max	Unit
Internal voltage	V_{L1}	Connect $1\text{M}\Omega$ load resistor between V_{DD} and V_{L1} (without panel load)	$1/2 \cdot V_{L2}$ -0.1		$1/2 \cdot V_{L2}$ $\times 0.85$	V
	V_{L2}	Connect $1\text{M}\Omega$ load resistor between V_{DD} and V_{L2} (without panel load)		V_{SS}		V
	V_{L3}	Connect $1\text{M}\Omega$ load resistor between V_{DD} and V_{L3} (without panel load)	$3/2 \cdot V_{L2}$ -0.1		$3/2 \cdot V_{L2}$ $\times 0.85$	V
Power current consumption	IOP	During HALT		2.0	5.5	μA
		During execution		5.5	10.0	μA
		During A/D conversion (HALT)		31	41.5	μA

S1C60L05 (Normal Operating Mode)

Unless otherwise specified

$V_{DD}=0\text{ V}$, $V_{SS}=-1.5\text{ V}$, $f_{osc}=32,768\text{ Hz}$, $T_a=25^{\circ}\text{C}$, $C_G=25\text{ pF}$, V_{S1} , V_{L1} , V_{L2} and V_{L3} are internal voltages, and $C_1=C_2=0.1\text{ }\mu\text{F}$

(During A/D conversion: $R_S=49.8\text{ k}\Omega$, $T_H=50\text{ k}\Omega$, $C_{AD}=2,200\text{ pF}$)

Item	Symbol	Condition	Min	Typ	Max	Unit
Internal voltage	V_{L1}	Connect $1\text{ M}\Omega$ load resistor between V_{DD} and V_{L1} (without panel load)		V_{SS}		V
	V_{L2}	Connect $1\text{ M}\Omega$ load resistor between V_{DD} and V_{L2} (without panel load)	$2 \cdot V_{L1}$ -0.1		$2 \cdot V_{L1}$ $\times 0.9$	V
	V_{L3}	Connect $1\text{ M}\Omega$ load resistor between V_{DD} and V_{L3} (without panel load)	$3 \cdot V_{L1}$ -0.1		$3 \cdot V_{L1}$ $\times 0.9$	V
Power current consumption	IOP	During HALT		0.8	1.4	μA
		During execution	Without panel load	1.5	5.0	μA
		During A/D conversion (HALT)		30	40	μA

S1C60L05 (Heavy Load Protection Mode)

Unless otherwise specified

$V_{DD}=0\text{ V}$, $V_{SS}=-1.5\text{ V}$, $f_{osc}=32,768\text{ Hz}$, $T_a=25^{\circ}\text{C}$, $C_G=25\text{ pF}$, V_{S1} , V_{L1} , V_{L2} and V_{L3} are internal voltages, and $C_1=C_2=0.1\text{ }\mu\text{F}$

(During A/D conversion: $R_S=49.8\text{ k}\Omega$, $T_H=50\text{ k}\Omega$, $C_{AD}=2,200\text{ pF}$)

Item	Symbol	Condition	Min	Typ	Max	Unit
Internal voltage	V_{L1}	Connect $1\text{ M}\Omega$ load resistor between V_{DD} and V_{L1} (without panel load)		V_{SS}		V
	V_{L2}	Connect $1\text{ M}\Omega$ load resistor between V_{DD} and V_{L2} (without panel load)	$2 \cdot V_{L1}$ -0.1		$2 \cdot V_{L1}$ $\times 0.85$	V
	V_{L3}	Connect $1\text{ M}\Omega$ load resistor between V_{DD} and V_{L3} (without panel load)	$3 \cdot V_{L1}$ -0.1		$3 \cdot V_{L1}$ $\times 0.85$	V
Power current consumption	IOP	During HALT		2.0	5.5	μA
		During execution	Without panel load	5.5	10.0	μA
		During A/D conversion (HALT)		31	41.5	μA

S1C60N05 (CR, Normal Operating Mode)

Unless otherwise specified

$V_{DD}=0$ V, $V_{SS}=-3.0$ V, $f_{osc}=65$ kHz, $T_a=25^{\circ}\text{C}$, $C_G=25$ pF, V_{S1} , V_{L1} , V_{L2} and V_{L3} are internal voltages, and $C_1=C_2=0.1$ μF , Recommended external resistance for CR oscillation = 420 k Ω

(During A/D conversion: $R_S=49.8$ k Ω , $T_H=50$ k Ω , $C_{AD}=2,200$ pF)

Item	Symbol	Condition	Min	Typ	Max	Unit
Internal voltage	V_{L1}	Connect 1M Ω load resistor between V_{DD} and V_{L1} (without panel load)	$1/2 \cdot V_{L2}$ -0.1		$1/2 \cdot V_{L2}$ $\times 0.9$	V
	V_{L2}	Connect 1M Ω load resistor between V_{DD} and V_{L2} (without panel load)		V_{SS}		V
	V_{L3}	Connect 1M Ω load resistor between V_{DD} and V_{L3} (without panel load)	$3/2 \cdot V_{L2}$ -0.1		$3/2 \cdot V_{L2}$ $\times 0.9$	V
Power current consumption	IOP	During HALT		8.0	15.0	μA
		During execution		15.0	20.0	μA
		During A/D conversion (HALT)		37	52.5	μA

S1C60N05 (CR, Heavy Load Protection Mode)

Unless otherwise specified

$V_{DD}=0$ V, $V_{SS}=-3.0$ V, $f_{osc}=65$ kHz, $T_a=25^{\circ}\text{C}$, $C_G=25$ pF, V_{S1} , V_{L1} , V_{L2} and V_{L3} are internal voltages, and $C_1=C_2=0.1$ μF , Recommended external resistance for CR oscillation = 420 k Ω

(During A/D conversion: $R_S=49.8$ k Ω , $T_H=50$ k Ω , $C_{AD}=2,200$ pF)

Item	Symbol	Condition	Min	Typ	Max	Unit
Internal voltage	V_{L1}	Connect 1M Ω load resistor between V_{DD} and V_{L1} (without panel load)	$1/2 \cdot V_{L2}$ -0.1		$1/2 \cdot V_{L2}$ $\times 0.85$	V
	V_{L2}	Connect 1M Ω load resistor between V_{DD} and V_{L2} (without panel load)		V_{SS}		V
	V_{L3}	Connect 1M Ω load resistor between V_{DD} and V_{L3} (without panel load)	$3/2 \cdot V_{L2}$ -0.1		$3/2 \cdot V_{L2}$ $\times 0.85$	V
Power current consumption	IOP	During HALT		16.0	30.0	μA
		During execution		30.0	40.0	μA
		During A/D conversion (HALT)		45	57.5	μA

S1C60L05 (CR, Normal Operating Mode)

Unless otherwise specified

VDD=0 V, VSS=-1.5 V, fosc=65 kHz, Ta=25°C, CG=25 pF, VS1, VL1, VL2 and VL3 are internal voltages, and C1=C2=0.1 μF, Recommended external resistance for CR oscillation = 420 kΩ

(During A/D conversion: RS=49.8 kΩ, TH=50 kΩ, CAD=2,200 pF)

Item	Symbol	Condition		Min	Typ	Max	Unit
Internal voltage	VL1	Connect 1MΩ load resistor between VDD and VL1 (without panel load)			VSS		V
	VL2	Connect 1MΩ load resistor between VDD and VL2 (without panel load)		2•VL1 -0.1		2•VL1 × 0.9	V
	VL3	Connect 1MΩ load resistor between VDD and VL3 (without panel load)		3•VL1 -0.1		3•VL1 × 0.9	V
Power current consumption	IOP	During HALT	Without panel load		8.0	15.0	μA
		During execution			15.0	20.0	μA
		During A/D conversion (HALT)			37	52.5	μA

S1C60L05 (CR, Heavy Load Protection Mode)

Unless otherwise specified

VDD=0 V, VSS=-1.5 V, fosc=65 kHz, Ta=25°C, CG=25 pF, VS1, VL1, VL2 and VL3 are internal voltages, and C1=C2=0.1 μF, Recommended external resistance for CR oscillation = 420 kΩ

(During A/D conversion: RS=49.8 kΩ, TH=50 kΩ, CAD=2,200 pF)

Item	Symbol	Condition		Min	Typ	Max	Unit
Internal voltage	VL1	Connect 1MΩ load resistor between VDD and VL1 (without panel load)			VSS		V
	VL2	Connect 1MΩ load resistor between VDD and VL2 (without panel load)		2•VL1 -0.1		2•VL1 × 0.85	V
	VL3	Connect 1MΩ load resistor between VDD and VL3 (without panel load)		3•VL1 -0.1		3•VL1 × 0.85	V
Power current consumption	IOP	During HALT	Without panel load		16.0	30.0	μA
		During execution			30.0	40.0	μA
		During A/D conversion (HALT)			45	57.5	μA

6.5 Oscillation Characteristics

Oscillation characteristics will vary according to different conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

S1C60N05

Unless otherwise specified

V_{DD}=0 V, V_{SS}=-3.0 V, Crystal : Q13MC146, C_G=25 pF, C_D=built-in, T_a=25°C

Item	Symbol	Condition	Min	Typ	Max	Unit
Oscillation start voltage	V _{sta} (V _{SS})	t _{sta} ≤5sec	-1.8			V
Oscillation stop voltage	V _{stp} (V _{SS})	t _{stp} ≤10sec	-1.8			V
Built-in capacity (drain)	C _D	Including the parasitic capacity inside the IC		20		pF
Frequency voltage deviation	f/V	V _{SS} =-1.8 to -3.5V			5	ppm
Frequency IC deviation	f/IC		-10		10	ppm
Frequency adjustment range	f/C _G	C _G =5–25pF	40			ppm
Higher harmonic oscillation start voltage	V _{hho} (V _{SS})	C _G =5pF			-3.6	V
Allowable leak resistance	R _{leak}	Between OSC1 and V _{DD} , and between V _{SS} and OSC1	200			MΩ

S1C60L05

Unless otherwise specified

V_{DD}=0 V, V_{SS}=-1.5 V, Crystal : Q13MC146, C_G=25 pF, C_D=built-in, T_a=25°C

Item	Symbol	Condition	Min	Typ	Max	Unit
Oscillation start voltage	V _{sta} (V _{SS})	t _{sta} ≤5sec	-1.2			V
Oscillation stop voltage	V _{stp} (V _{SS})	t _{stp} ≤10sec	-1.2			V
Built-in capacity (drain)	C _D	Including the parasitic capacity inside the IC		20		pF
Frequency voltage deviation	f/V	V _{SS} =-1.2 to -2.0V (-0.9)* ¹			5	ppm
Frequency IC deviation	f/IC		-10		10	ppm
Frequency adjustment range	f/C _G	C _G =5–25pF	40			ppm
Higher harmonic oscillation start voltage	V _{hho} (V _{SS})	C _G =5pF			-2.0	V
Allowable leak resistance	R _{leak}	Between OSC1 and V _{DD} , and between V _{SS} and OSC1	200			MΩ

*1 Items enclosed in parentheses () are those used when operating at heavy load protection mode.

S1C60N05 (CR)

Unless otherwise specified

VDD=0 V, VSS=-3.0 V, RCR=480 kΩ, Ta=25°C

Item	Symbol	Condition	Min	Typ	Max	Unit
Oscillation frequency dispersion	fosc		-20	65kHz	20	%
Oscillation start voltage	Vsta		-1.8			V
Oscillation start time	tsta	Vss=-1.8 to -3.5V		3		ms
Oscillation stop voltage	Vstp		-1.8			V

S1C60L05 (CR)

Unless otherwise specified

VDD=0 V, VSS=-1.5 V, RCR=480 kΩ, Ta=25°C

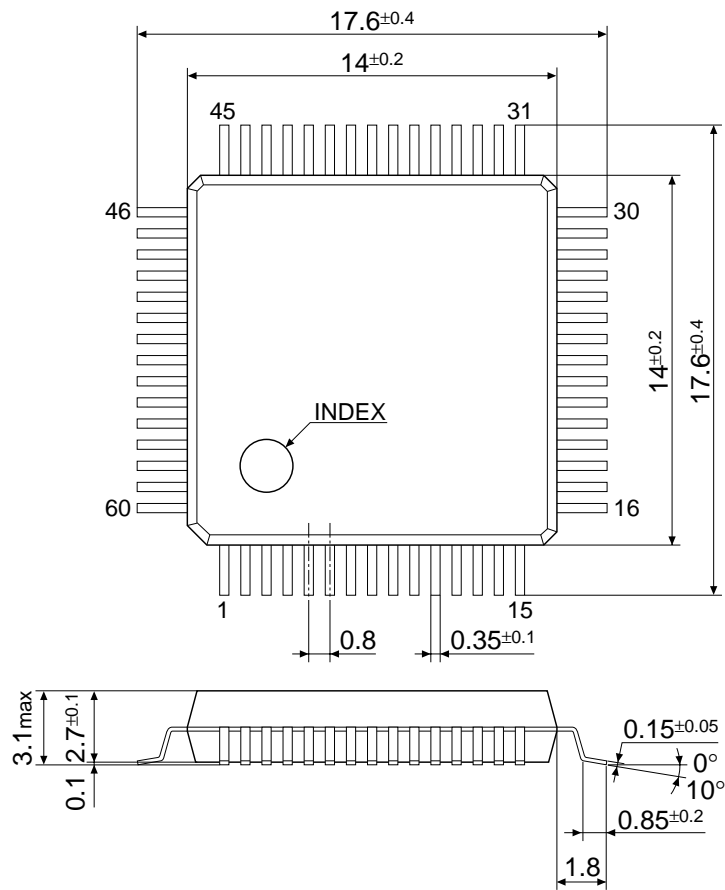
Item	Symbol	Condition	Min	Typ	Max	Unit
Oscillation frequency dispersion	fosc		-20	65kHz	20	%
Oscillation start voltage	Vsta		-1.2			V
Oscillation start time	tsta	Vss=-1.2 to -2.0V		3		ms
Oscillation stop voltage	Vstp		-1.2			V

CHAPTER 7 PACKAGE

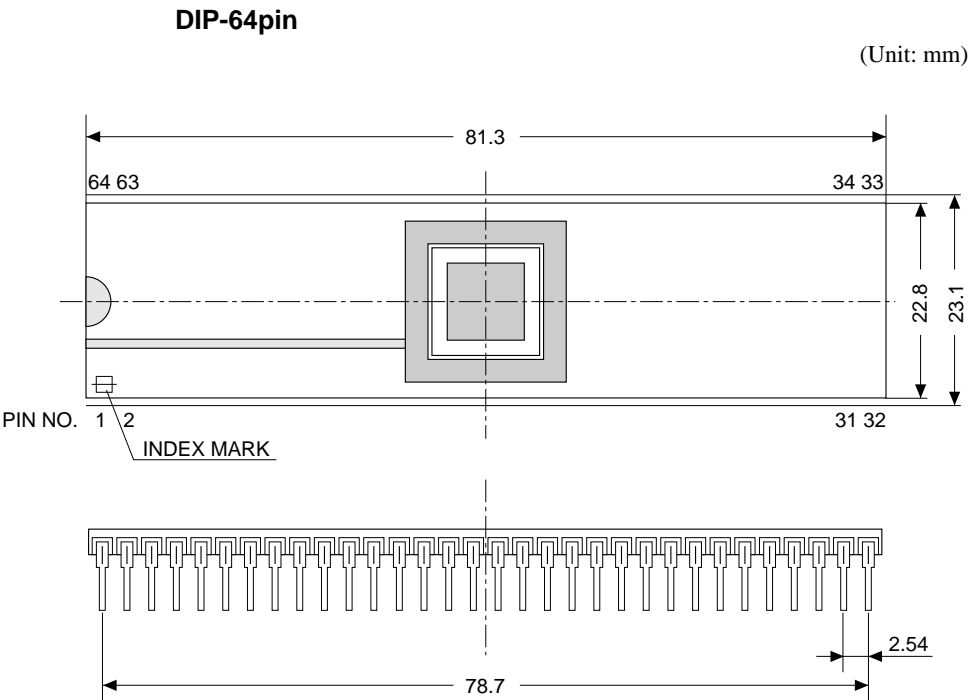
7.1 Plastic Package

QFP6-60pin

(Unit: mm)



7.2 Ceramic Package for Test Samples

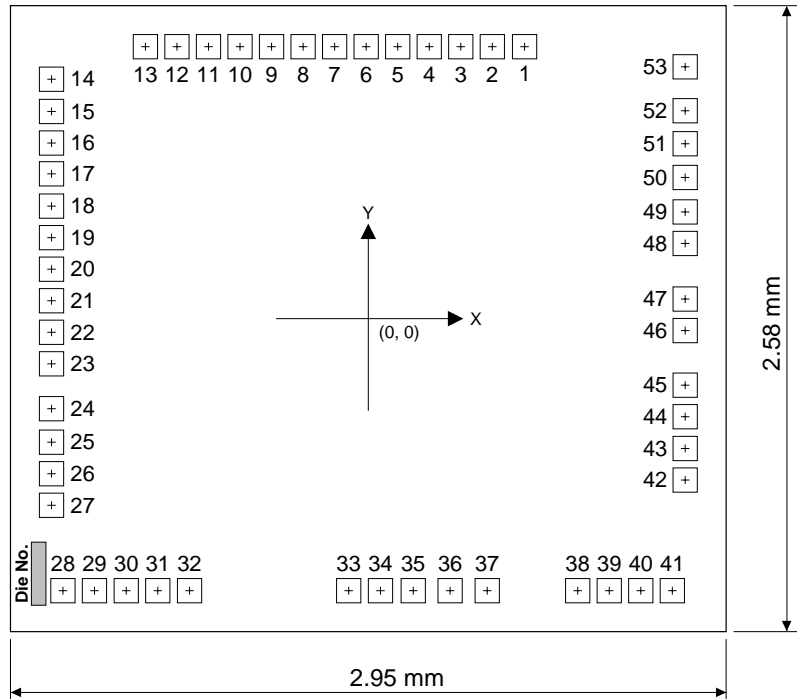


No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	N.C.	17	OSC1	33	R02	49	SEG6
2	SEG17	18	OSC2	34	R03	50	SEG7
3	SEG18	19	V _{S1}	35	RS	51	SEG8
4	SEG19	20	P00	36	TH1	52	SEG9
5	COM0	21	P01	37	TH2	53	SEG10
6	COM1	22	P02	38	CS	54	SEG11
7	COM2	23	P03	39	N.C.	55	N.C.
8	COM3	24	N.C.	40	N.C.	56	N.C.
9	N.C.	25	N.C.	41	N.C.	57	TEST
10	V _{L3}	26	N.C.	42	ADOUT	58	RESET
11	V _{L2}	27	K00	43	SEG0	59	SEG12
12	V _{L1}	28	K01	44	SEG1	60	SEG13
13	CA	29	K02	45	SEG2	61	SEG14
14	CB	30	K03	46	SEG3	62	SEG15
15	V _{SS}	31	R00	47	SEG4	63	SEG16
16	V _{DD}	32	R01	48	SEG5	64	N.C.

N.C. = No Connection

CHAPTER 8 PAD LAYOUT

8.1 Diagram of Pad Layout



8.2 Pad Coordinates

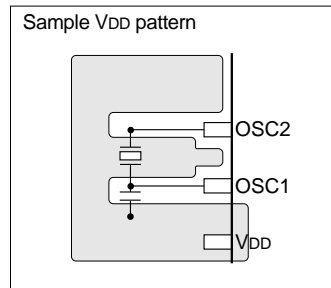
Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y
1	ADOUT	644	1,121	28	VL3	-1,259	-1,121
2	SEG0	511	1,121	29	VL2	-1,129	-1,121
3	SEG1	381	1,121	30	VL1	-998	-1,121
4	SEG2	251	1,121	31	CA	-868	-1,121
5	SEG3	121	1,121	32	CB	-737	-1,121
6	SEG4	-9	1,121	33	Vss	-81	-1,121
7	SEG5	-139	1,121	34	VDD	50	-1,121
8	SEG6	-269	1,121	35	OSC1	185	-1,121
9	SEG7	-399	1,121	36	OSC2	337	-1,121
10	SEG8	-529	1,121	37	Vs1	490	-1,121
11	SEG9	-659	1,121	38	P00	863	-1,121
12	SEG10	-789	1,121	39	P01	993	-1,121
13	SEG11	-919	1,121	40	P02	1,123	-1,121
14	TEST	-1,306	987	41	P03	1,253	-1,121
15	RESET	-1,306	854	42	K00	1,306	-665
16	SEG12	-1,306	724	43	K01	1,306	-535
17	SEG13	-1,306	597	44	K02	1,306	-404
18	SEG14	-1,306	464	45	K03	1,306	-274
19	SEG15	-1,306	334	46	R00	1,306	-49
20	SEG16	-1,306	204	47	R01	1,306	81
21	SEG17	-1,306	74	48	R02	1,306	310
22	SEG18	-1,306	-56	49	R03	1,306	440
23	SEG19	-1,306	-186	50	RS	1,306	582
24	COM0	-1,306	-371	51	TH1	1,306	721
25	COM1	-1,306	-509	52	TH2	1,306	857
26	COM2	-1,306	-639	53	CS	1,306	1,038
27	COM3	-1,306	-769				

(Unit: μm)

CHAPTER 9 PRECAUTIONS ON MOUNTING

Oscillation circuit

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.).
In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:
 - (1) Components which are connected to the OSC1 and OSC2 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.
 - (2) As shown in the right hand figure, make a VDD pattern as large as possible at circumscription of the OSC1 and OSC2 terminals. Furthermore, do not use this VDD pattern for any purpose other than the oscillation system.



- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1 and VSS, please keep enough distance between OSC1 and VSS or other signals on the board pattern.

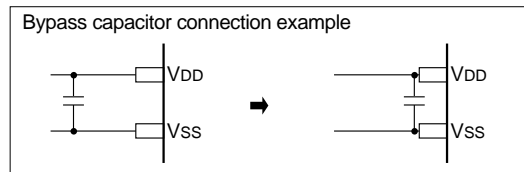
Reset circuit

- The power-on reset signal which is input to the RESET terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product. When the built-in pull-down resistor is added to the RESET terminal by mask option, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the RESET terminal in the shortest line.

Power supply circuit

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:
 - (1) The power supply should be connected to the VDD and VSS terminal with patterns as short and large as possible.

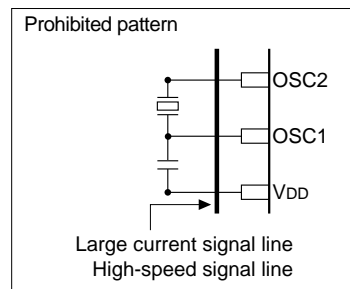
- (2) When connecting between the VDD and VSS terminals with a bypass capacitor, the terminals should be connected as short as possible.



- (3) Components which are connected to the VS1, VL1-VL3 terminals, such as capacitors and resistors, should be connected in the shortest line.
In particular, the VL1-VL3 voltages affect the display quality.

- Do not connect anything to the VL1-VL3 terminals when the LCD driver is not used.
- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction.
Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit.

Arrangement of signal lines



Precautions for visible radiation (when bare chip is mounted)

- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.
 - (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.
 - (2) The inspection process of the product needs an environment that shields the IC from visible radiation.
 - (3) As well as the face of the IC, shield the back and side too.

Appendices TECHNICAL INFORMATION

This chapter presents the information necessary for designing a thermometer using a Seiko Epson S1C60N05 and a Thermistor manufactured by Ishizuka Denshi Inc.

Appendix A Design Steps for Designing Thermometer

This section describes the design steps for the thermometer using the S1C60N05 and the Thermistor.

Thermometer design steps

The following shows the design steps:

- (1) Obtain the external capacitor value and the oscillation frequency.
- (2) Obtain the initial value that is set to the up-counter of the A/D converter.
- (3) After A/D conversion, calculate the displayed temperature from the counter value that has been set in the up-counter.

Details of these steps are described in later sections.

Before designing the thermometer, the measured temperature range, standard temperature, and thermistor to be used have to be determined.

Measured temperature range Determine for your application.

Standard temperature The standard temperature is the most precise value. Determine the standard temperature as the temperature that you want to be the most precise.

Thermistor Select the thermistor considering the measured temperature range and the standard temperature. It also should match the IC.

Note that this document assumes the following:

Measured temperature range: -30°C–70°C

Standard temperature: 20°C

Thermistor: Thermistor 103AT (Compatibility with S1C60N05)

The following A/D converter circuit diagram is shown for your reference.

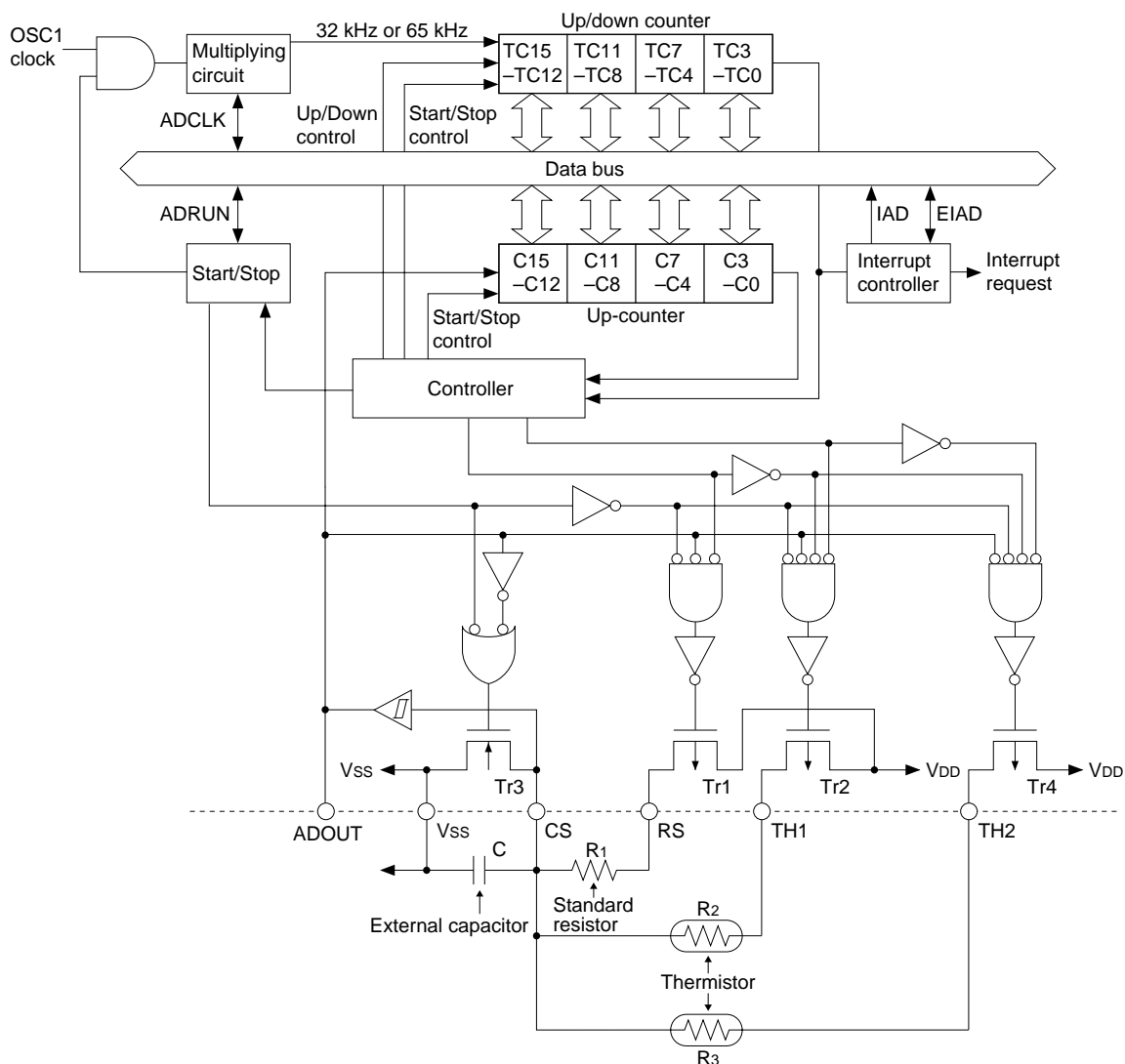


Fig. A.1
A/D converter configuration

How to obtain capacitor value and oscillation frequency

The standard resistor and the thermistor are oscillated according to S1C60N05 A/D converter principles. It is necessary to determine the value of the external capacitor for the oscillation. This section describes how to determine the standard resistor value, the external capacitor value and the CR oscillation frequency.

Table A.1

Item	Description	Thermistor 103AT usage example
Standard resistor value (R ₁)	Thermistor resistance value at the standard temperature.	At 25°C, the 103AT resistance is 10 kΩ. Thus the standard resistance is 10 kΩ.
Computation of capacitor for oscillation	<p>The relationship between the frequency, capacitor, and the resistor is as follows:</p> $f = \frac{K}{CR}$ <p> f: Oscillation frequency K: CR oscillation frequency coefficient C: Capacitor R: Resistance </p> <p>From the equation above, C can be obtained based on f and K conditions of S1C60N05. If the C value is smaller within the conditions, the precision is higher.</p>	<p>The f and K conditions of S1C60N05 are as follows:</p> <p>f(max) = 85 kHz (limit of IC operation) 1 ≤ K ≤ 3 (Oscillation coefficient in S1C60N05)</p> <p>With these conditions, the following equation can be derived:</p> $85 \text{ kHz} \geq \frac{K}{CR_{2(TMAX)}}$ <p>R_{2(TMAX)}: Minimum resistance of Thermistor</p> <p>K=3 is the worst condition, then</p> $C \geq \frac{3}{85 \times 10^3 \times 2.23 \times 10^3} = 15,800 \text{ (pF)}$ <p>As a result, the following is determined:</p> <p>C = 22,000 (pF) (Value for general purpose product)</p>
Computation of frequency from the standard resistance	<p>If the C value is determined by the above equation, the frequency (f_{CR1}) by the standard resistance can be obtained by the following equation:</p> $f_{CR1} \text{ (kHz)} = \frac{K}{CR_1}$	<p>The following is obtained:</p> $f_{CR1} = \frac{(1 \text{ to } 3)}{22,000 \times 10^{-12} \times 10 \times 10^3} = 4.5 \text{ to } 13.5 \text{ (kHz)}$

By the above equations, the capacitor value (22,000 pF) and the oscillation frequency (4.5–13.5 kHz) by the standard resistance are determined.

For the details of 103AT, see Appendix C.

Setting up counter initial value

The capacitor value and the oscillation frequency by the standard resistance are determined in the previous section.

This section describes how to set the initial value of the A/D converter's up counter.

For A/D converter principals, see the technical manual for the S1C60N05.

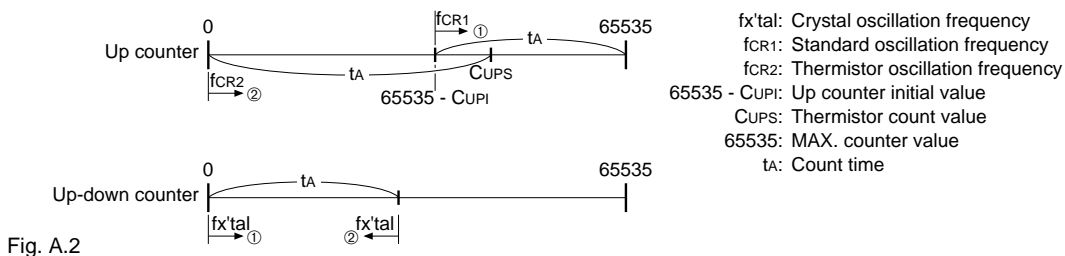


Figure A.2 shows the relationship between the up counter and the up-down counter.

The following conditions should be satisfied:

Condition (A): The up-down counter should not overflow during an up-count

Condition (B): The up counter should not overflow during a down-count

With these conditions, the up counter initial value can be obtained with the following equations:

Table A.2

Item	Description	Thermistor 103AT usage example
Obtain the up counter initial value from the condition (A)	<p>From the condition (A) the following equation is derived:</p> $65535 > t_A \cdot f_{x'tal} = \frac{65535 - CUP_i}{f_{CR1}} \times f_{x'tal}$ $CUP_i > \left(1 - \frac{f_{CR1}}{f_{x'tal}}\right) \times 65535$ <p>Initial value $\leq 65535 - CUP_i \dots(a)$</p>	<p>From $f_{x'tal} = 65 \text{ kHz}$, $f_{CR1} = 4.5\text{--}13.5 \text{ kHz}$</p> $CUP_i = \left(1 - \frac{4.5 \times 10^3}{65 \times 10^3}\right) \times 65535 \approx 59571$ $CUP_i = \left(1 - \frac{13.5 \times 10^3}{65 \times 10^3}\right) \times 65535 \approx 50707$ <p>Initial value $\leq 65535 - 59571 = 5964 \dots(a)'$</p>
Obtain the up counter initial value from the condition (B)	<p>From the condition (B) the following equation is derived:</p> $65535 > CUPS = t_A \times f_{CR2(3)}$ $= \frac{f_{CR2}}{f_{CR1}} \times (65535 - CUP_i)$ $CUP_i = \left(1 - \frac{f_{CR1}}{f_{CR2(3)}}\right) \times 65535$ <p>Initial value $\leq 65535 - CUP_i \dots(b)$</p> <p>From the above equations (a) and (b) the initial value can be determined.</p>	<p>$f_{CR1} = 4.5\text{--}13.5 \text{ kHz}$, $f_{CR2} = 85 \text{ kHz}$ (IC operational maximum)</p> $CUP_i = \left(1 - \frac{4.5 \times 10^3}{85 \times 10^3}\right) \times 65535 \approx 60608$ $CUP_i = \left(1 - \frac{13.5 \times 10^3}{85 \times 10^3}\right) \times 65535 \approx 53837$ <p>Initial value $\leq 65535 - 60608 = 4927 \dots(b)'$</p> <p>From (a)' and (b)', the initial value should be set less than 4927. Here, it is set to 3000. (Under the conditions, if the initial value is smaller, the precision is higher.)</p>

The initial value (3,000) for the up counter is derived from the above equations.

Computation method of displayed temperature by linear approximation

The following shows the linear approximation equation to derive the displayed temperature.

Displayed temperature (°C) = (Count after A/D conversion - Count for minimum in the temperature range) × linear approximation coefficient + minimum value of the temperature range

This equation derives the displayed temperature. The following shows the method. First, each value is described.

[Count value after A/D conversion]

This is the up counter value after an A/D conversion.

[Count for the minimum value of the temperature range]

[Minimum value of the temperature range]

To derive the displayed temperature by the linear approximation, the temperature range must be determined for the linear approximation. In this example, the measured temperature range is -30 to 70°C.

If the temperature range for the linear approximation is set for every 10°C, the temperature range is -30 to -20°C, -20 to -10°C, and so on. The smallest value of each temperature range segment is the minimum value of the temperature range. The largest value is the maximum value of the temperature range.

The count value for the minimum value for the temperature range is expressed by the following equation:

$$\begin{aligned} \text{A/D converter count value} &= \frac{f_{CR2(3)}}{f_{CR1}} \times \text{up counter initial value} \\ &= \frac{(K/CR2(3))}{(K/CR1)} \times \text{up counter initial value} \\ &= \frac{R_1}{R2(3)} \times \text{up counter initial value} \end{aligned}$$

By substituting R2 (Thermistor resistance), R1 (standard resistance), and the up counter initial value with actual values, the count value for the minimum of the temperature range is obtained.

[Linear approximation coefficient]

The linear approximation coefficient is the value that shows how many degrees (centigrade) for one count in the temperature range. The linear approximation coefficient is expressed by the following equation:

$$\begin{aligned} \text{Linear approximation coefficient} &= \\ &= \frac{\text{Temperature range}}{\text{Count for max. of temperature range} - \text{Count for min. of temperature range}} \end{aligned}$$

(As you can see, the temperature range is smaller, the precision is higher.)

The following table shows the various values for every 10°C.

Table A.3

Temperature (°C)	103AT Thermistor R ₂ resistance (kΩ)	Linear approximation coefficient in the specified temperature range	Count value
-30	111.3	0.0575	269
-20	67.74	0.0380	443
-10	42.45	0.0254	706
0	27.28	0.0175	1099
10	17.96	0.0123	1670
20	12.09	0.00887	2481
30	8.313	0.00650	3608
40	5.828	0.00485	5147
50	4.161	0.00368	7209
60	3.021	0.00283	9930
70	2.229		13459

The following example derives a displayed temperature using the values in the above table.

Example: Assume the count value after an A/D conversion is 3200. Then, it is between 3608 and 2481 in the table. As a result the temperature range is 20° to 30°C.

- The count value for the minimum value of the temperature range: 2481
- The count value for the maximum value of the temperature range: 3608

Then, the linear approximation coefficient of the temperature range is 0.00887.

As a result, the displayed temperature is derived as follows:

$$\text{Displayed temperature} = (3200 - 2481) \times 0.00887 + 20 \text{ (°C)} = 26.377 \text{ (°C)}$$

Appendix B Error Factors

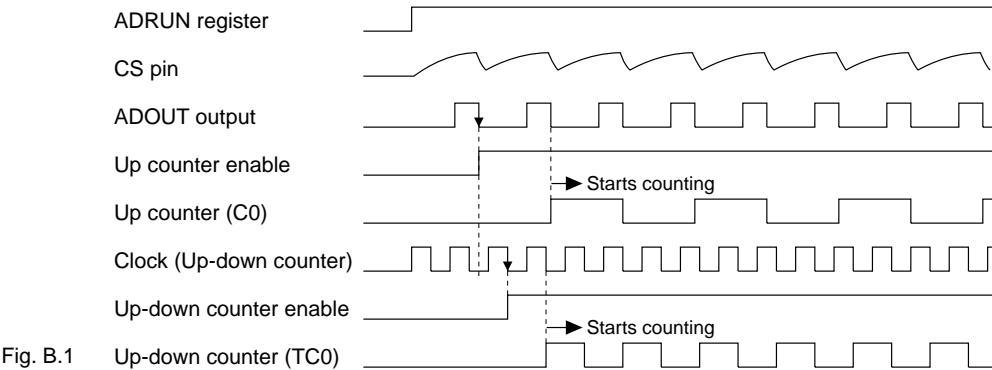
When a temperature is computed using the S1C60N05 A/D converter and the Thermistor, the following error factors should be taken in account:

Thermistor resistance dispersion

The Thermistor manufacturer should guarantee the precision.

A/D converter error factors

Error (circuit) by A/D conversion in R1 (standard resistance) and R2 (Thermistor)
By the CR oscillation at the standard resistor (R1), the up counter and the up-down counter increment the counter with the timing shown below.



After the A/D RUN, the first trailing edge of the CS pin triggers the up counter enable. From the next trailing edge, the up counter starts to count. In addition, the first trailing edge of the clock after the up counter is enabled, the up-down counter is enabled and it starts to count from the next trailing edge. When the up counter value becomes 0, the up counter is disabled. The next trailing edge of the clock disables the up-down counter. If this situation occurs, the error described below will result.

Started:	Min. ≈ 0	} Total up-down counter - 2 counts
	Max. Up-down counter - 1 count	
Stopped:	Min ≈ 0	
	Max. Up-down counter - 1 count	

The same is true in the CR oscillation by Thermistor R2, and a similar error occurs. Exception: because the up-down counter is down-counted the following counting error occurs:

Started:	Min. ≈ 0	} Total up-down counter - 2 counts
	Max. Up-down counter - 1 count	
Stopped:	Min ≈ 0	
	Max. Up-down counter - 1 count	

Therefore, as for the error from the circuit, a maximum of 2 count errors results.

The effect of the maximum 2 count error is given below.

$$\Delta_1\text{MAX} (\%) = \frac{2}{(f_{\text{CLK}}/f_{\text{CR1}}) \times \text{CUP11}} \times 100 \text{ --- (1)}$$

$$\Delta_2\text{MAX} (\%) = \frac{2}{(f_{\text{CLK}}/f_{\text{CR2}}) \times \text{CUPS}} \times 100 \text{ --- (2)}$$

fCLK: Clock frequency (32 kHz/64 kHz)

fCR1: CR oscillation frequency by standard resistor

CUP11: Up counter initial value (times)

$\Delta_1\text{MAX}$: Maximum error (%) at CR oscillation by standard resistor

fCR2: CR oscillation frequency by Thermistor

CUPS: Thermistor count (times)

$\Delta_2\text{MAX}$: Maximum error (%) at CR oscillation by Thermistor

In addition, the number of counts of the up-down counter should be the same. Then the following equation is true:

$$\frac{f_{\text{CLK}}}{f_{\text{CR1}}} \times \text{CUP11} = \frac{f_{\text{CLK}}}{f_{\text{CR2}}} \times \text{CUPS} \text{ --- (3)}$$

Then, from (3), assume the up-down counter counts shifted 2 counts, the following equations are true:

$$\frac{f_{\text{CLK}}}{f_{\text{CR1}}} \times \text{CUP11} = \frac{f_{\text{CLK}}}{f_{\text{CR2}}} \times \text{CUPS} \pm 2$$

$$\frac{f_{\text{CR2}}}{f_{\text{CR1}}} = \frac{\text{CUPS} \pm 2 \times (f_{\text{CR2}}/f_{\text{CLK}})}{\text{CUP11}} \text{ --- (3)'}$$

(1) is the count error at the CR oscillation by the standard resistor.

(2) is the count error at the CR oscillation by Thermistor.

The total error is expressed by the equation (3)' with the ratio of fCR1 and fCR2.

The segment that represents the error in the equation (3)' is $\pm 2 \times (f_{\text{CR2}}/f_{\text{CLK}})$. If the values CUP11 and CUPS are large, this error factor may be ignored.

For how to determine the initial value (CUP11) of the up counter, see the section describing thermometer design steps.

CR oscillation constant (K) error

The constant, K, is determined by the logic level of the internal Schmidt trigger of the IC. However, in S1C60N05, the Schmidt trigger shares the circuit with the standard resistor and Thermistor. As a result, oscillation is canceled and no error occurs.

Error by transistor ON resistance

The transistor ON resistance is directly connected to the standard resistor and Thermistor; this may cause an error.

See the circuit shown next to Figure B.2 below. In this circuit, the capacitor is charged by Tr1, T2 ON and Tr3 OFF. If the voltage at the CS pin changes to a certain level, the capacitor charge is drained by Tr1, Tr2 OFF and Tr3 ON. As a result, the CR oscillation is generated as in Figure B.3.

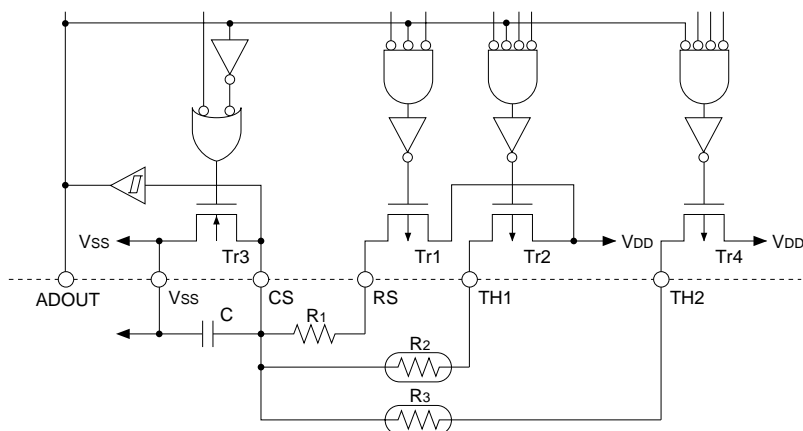


Fig. B.2

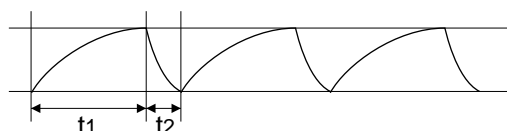


Fig. B.3

At this time, if the ON resistance of Tr1 and Tr2 ON is t_1 and the ON resistance of Tr3 is t_2 , the constance may be effected.

The S1C60N05 transistors are standardized to have a maximum of 100 Ω .

This standard includes dispersion by temperature characteristics, Pch and Nch.

The Evaluation board transistor uses standard ICs and the actual resistance is about 1 k Ω . (This is not guaranteed and should be regarded as just a reference.)

The error by ON resistance of this transistor is expressed by the following equations:

$$\begin{aligned} \Delta 3 (\%) &= \frac{\text{Up counter count} - \text{Actual upcounter count}}{\text{Up counter count}} \times 100 \\ &= \frac{K}{\text{CUP11} - \frac{C(R_1 + R_{Tr})}{f_{CR1}} \times \text{CUP11}} \times 100 = \left\{ 1 - \frac{R_1}{(R_1 + R_{Tr})} \right\} \times 100 \\ \Delta 4 (\%) &= \frac{\text{Up counter count} - \text{Actual upcounter count}}{\text{Up counter count}} \times 100 \\ &= \frac{K}{\text{CUPS} - \frac{C(R_2 + R_{Tr})}{f_{CR2}} \times \text{CUP11}} \times 100 = \left\{ 1 - \frac{R_2}{(R_2 + R_{Tr})} \right\} \times 100 \end{aligned}$$

$\Delta 3$: Error (%) by transistor ON resistance (CR oscillation by standard resistance)

$\Delta 4$: Error (%) by transistor ON resistance (CR oscillation by Thermistor)

CUP11: Up counter initial value (times)

CUPS: Thermistor count value (times)

R_{Tr} : Transistor ON resistance (Ω)

f_{CR1} : Oscillation frequency (Hz) (CR oscillation by standard resistance)

f_{CR2} : Oscillation frequency (Hz) (CR oscillation by Thermistor)

Example: Transistor ON resistance error when Thermistor 103AT measures 60°C

$$\Delta 3 = \left\{ 1 - \frac{10 \times 10^3}{(10 \times 10^3 + 100)} \right\} \times 100 \approx 1\%$$

$$\Delta 4 = \left\{ 1 - \frac{3.217 \times 10^3}{(3.217 \times 10^3 + 100)} \right\} \times 100 \approx 3\%$$

As a result, the following errors occur by directly connecting the transistor ON resistance:

1% at CR oscillation on the standard resistor

3% at CR oscillation on Thermistor

The transistor ON resistance effect is smaller if R1 and R2 are larger. (See Equation $\Delta 3$ and $\Delta 4$.)

In the high temperature range, the R2 value becomes small and $\Delta 4$ becomes large. This causes precision degradation. Compensation is needed to implement a user's required precision.

Error by floating capacity

The floating capacity of the inside of an IC, board, lead of a sensor and others may be an error factor. Floating capacity inside an IC may be several pF and it may be ignored by increasing the capacitor value.

Software error

In the software, it is normal to convert the counter value to an actual temperature by a linear approximation. In this method, an error may be caused by the linear approximation in the temperature measured range.

As shown in Figure B.4 below, if the temperature range measured is 20°C to 30°C, the weight of 1 count differs between 20°C and 29°C.

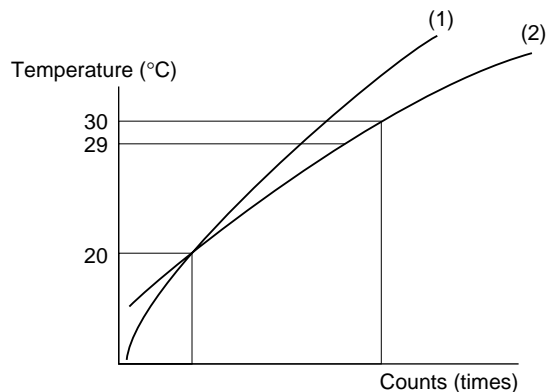


Fig. B.4

On the slope (1), the linear approximation coefficient in this segment for 1 count is large, and the slope (2) has a smaller coefficient.

For example, if this segment (20°C to 30°C) is calculated by the same linear approximation coefficient, and if the 20°C is the reference point, then, at 29°C, the linear approximation coefficient becomes the largest and, at 29°C, the error is maximum.

The error may differ depending on the temperature measured by the software, up counter initial value and Thermistor type.

Appendix C AT Thermistor

High precision thermistor

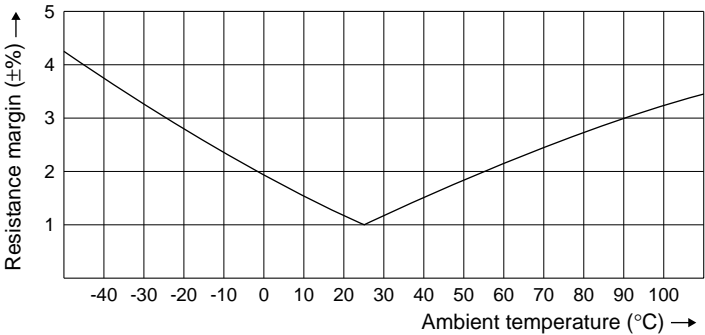
- Features** The AT Thermistor has a high precision thermistor with small resistance and B constant error margin.
- Using the AT Thermistor as a temperature sensor does not require adjustment between a control circuit and the sensor; and the AT Thermistor provides a temperature precision of $\pm 0.3^{\circ}\text{C}$. As a result, a high precision temperature control and temperature display are possible.
- Error margins of resistance and temperature characteristics are very small.
 - Small age-based change and high reliability
 - Low price
 - High durability

Usage Air conditioners, fan heaters, FF heaters, refrigerators, water heaters, boiler/kitchen appliances, copiers, printers, facsimiles, automatic vending machines, agricultural equipment, automobiles (for external temperature, internal temperature, air flow sensor), portable thermometers, medical equipment, thermos-type containers, solar heating system, automatic toilet seats, fire alarms, home automation

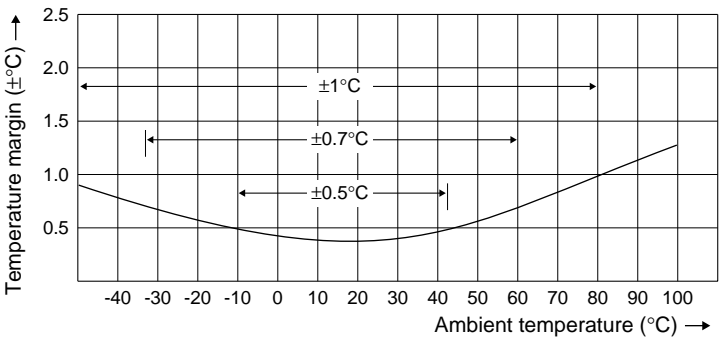
Type number **103 AT - 2**

- External type
- High precision AT Thermistor
- Zero load resistance (25°C) 103: 10 k Ω

Resistance margin graph



Temperature precision graph



Comparison between AT type and others

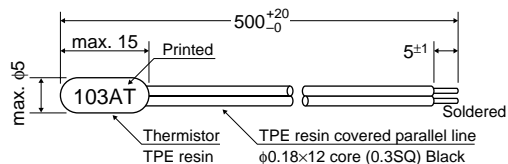
Thermistor	R25 margin	B margin	Temperature margin (25°C)	Temperature control (display) for every 1°C
AT type	±1%	±1%	±0.3°C	Circuit adjustment - not required
Other type	±5%	±3%	±1.3°C	Circuit adjustment - required

Ratings

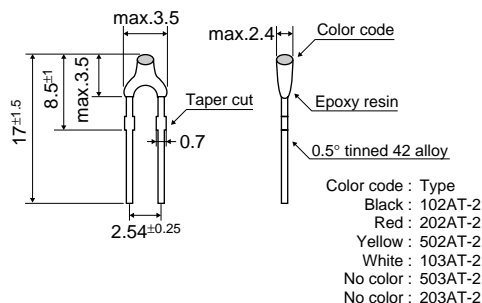
Type	R25	B constant	Thermal radiation constant (mW/°C)	Thermal constant (s)	Maximum power (mW) at 25°C	Temperature range (°C)
102AT-1	1 kΩ ±1%	3100K ±1%	Approx. 3	Approx. 75	15	-50 to 90
202AT-1	2 kΩ ±1%	3182K ±1%	Approx. 3	Approx. 75	15	-50 to 90
502AT-1	5 kΩ ±1%	3324K ±1%	Approx. 3	Approx. 75	15	-50 to 105
103AT-1	10 kΩ ±1%	3435K ±1%	Approx. 3	Approx. 75	15	-50 to 105
102AT-2	1 kΩ ±1%	3100K ±1%	Approx. 2	Approx. 15	10	-50 to 90
202AT-2	2 kΩ ±1%	3182K ±1%	Approx. 2	Approx. 15	10	-50 to 90
502AT-2	5 kΩ ±1%	3324K ±1%	Approx. 2	Approx. 15	10	-50 to 110
103AT-2	10 kΩ ±1%	3435K ±1%	Approx. 2	Approx. 15	10	-50 to 110
203AT-2	20 kΩ ±1%	4013K ±1%	Approx. 2	Approx. 15	10	-50 to 110
503AT-2	50 kΩ ±1%	4060K ±1%	Approx. 2	Approx. 15	10	-50 to 110

External dimension

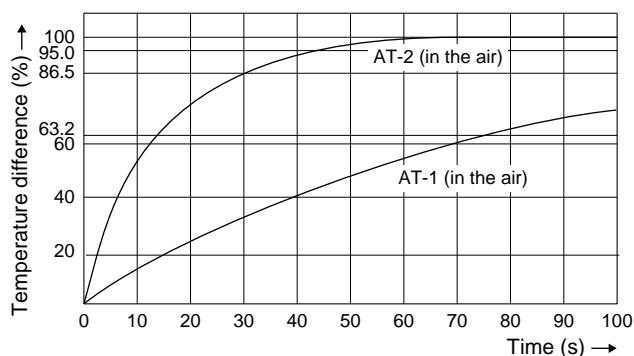
AT-1



AT-2

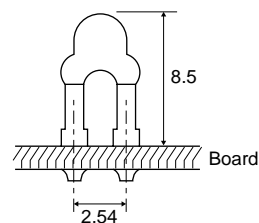


Thermal response



Board soldering method

Proper usage example



Proper soldering conditions:
 260°C, 10 seconds or less

Resistance - Temperature characteristics

-50 to 29°C

30 to 110°C

Temp (°C)	103AT		
	Rmax (kΩ)	Rst (kΩ)	Rmin (kΩ)
-50	344.4	329.2	314.7
-49	324.7	310.7	297.2
-48	306.4	293.3	280.7
-47	289.2	277.0	265.3
-46	273.2	261.8	250.8
-45	258.1	247.5	237.3
-44	244.0	234.1	224.6
-43	230.8	221.6	212.7
-42	218.5	209.8	201.5
-41	206.8	198.7	191.0
-40	195.9	188.4	181.1
-39	185.4	178.3	171.5
-38	175.5	168.9	162.6
-37	166.2	160.1	154.2
-36	157.5	151.8	146.2
-35	149.3	144.0	138.8
-34	141.6	136.6	131.8
-33	134.4	129.7	125.2
-32	127.6	123.2	118.9
-31	121.2	117.1	113.1
-30	115.1	111.3	107.5
-29	109.3	105.7	102.2
-28	103.8	100.4	97.16
-27	98.63	95.47	92.41
-26	93.75	90.80	87.93
-25	89.15	86.39	83.70
-24	84.82	82.22	79.71
-23	80.72	78.29	75.93
-22	76.85	74.58	72.36
-21	73.20	71.07	68.99
-20	69.74	67.74	65.80
-19	66.42	64.54	62.72
-18	63.27	61.52	59.81
-17	60.30	58.66	57.05
-16	57.49	55.95	54.44
-15	54.83	53.39	51.97
-14	52.31	50.96	49.63
-13	49.93	48.66	47.42
-12	47.67	46.48	45.31
-11	45.53	44.41	43.32
-10	43.50	42.45	41.43
-9	41.54	40.56	39.59
-8	39.68	38.76	37.85
-7	37.91	37.05	36.20
-6	36.24	35.43	34.63
-5	34.65	33.89	33.14
-4	33.14	32.43	31.73
-3	31.71	31.04	30.39
-2	30.35	29.72	29.11
-1	29.06	28.47	27.89
0	27.83	27.28	26.74
1	26.64	26.13	25.62
2	25.51	25.03	24.55
3	24.44	23.99	23.54
4	23.42	22.99	22.57
5	22.45	22.05	21.66
6	21.52	21.15	20.78
7	20.64	20.29	19.95
8	19.80	19.48	19.15
9	19.00	18.70	18.40
10	18.24	17.96	17.67
11	17.51	17.24	16.97
12	16.80	16.55	16.31
13	16.13	15.90	15.67
14	15.50	15.28	15.06
15	14.89	14.68	14.48
16	14.31	14.12	13.93
17	13.75	13.57	13.40
18	13.22	13.06	12.89
19	12.72	12.56	12.41
20	12.23	12.09	11.95
21	11.77	11.63	11.50
22	11.32	11.20	11.07
23	10.90	10.78	10.66
24	10.49	10.38	10.27
25	10.10	10.00	9.900
26	9.732	9.632	9.533
27	9.381	9.281	9.181
28	9.044	8.944	8.845
29	8.721	8.622	8.523

Temp (°C)	103AT		
	Rmax (kΩ)	Rst (kΩ)	Rmin (kΩ)
30	8.412	8.313	8.215
31	8.113	8.015	7.917
32	7.826	7.729	7.632
33	7.551	7.455	7.359
34	7.288	7.192	7.097
35	7.036	6.941	6.846
36	6.793	6.699	6.606
37	6.561	6.468	6.375
38	6.338	6.246	6.154
39	6.124	6.033	5.942
40	5.918	5.828	5.739
41	5.719	5.630	5.541
42	5.527	5.439	5.352
43	5.343	5.256	5.170
44	5.166	5.080	4.996
45	4.996	4.912	4.828
46	4.833	4.749	4.667
47	4.676	4.594	4.512
48	4.525	4.444	4.364
49	4.380	4.300	4.221
50	4.240	4.161	4.084
51	4.104	4.026	3.950
52	3.973	3.897	3.822
53	3.847	3.772	3.698
54	3.726	3.652	3.579
55	3.609	3.537	3.465
56	3.497	3.426	3.355
57	3.389	3.319	3.249
58	3.285	3.216	3.148
59	3.184	3.116	3.049
60	3.088	3.021	2.955
61	2.994	2.928	2.863
62	2.903	2.838	2.775
63	2.816	2.752	2.690
64	2.732	2.669	2.608
65	2.650	2.589	2.529
66	2.572	2.512	2.452
67	2.496	2.437	2.379
68	2.423	2.365	2.308
69	2.353	2.296	2.240
70	2.285	2.229	2.174
71	2.219	2.163	2.109
72	2.155	2.101	2.047
73	2.093	2.040	1.987
74	2.034	1.981	1.930
75	1.976	1.924	1.874
76	1.920	1.870	1.820
77	1.866	1.817	1.768
78	1.814	1.766	1.718
79	1.764	1.716	1.669
80	1.716	1.669	1.622
81	1.668	1.622	1.577
82	1.623	1.577	1.533
83	1.578	1.534	1.490
84	1.536	1.492	1.449
85	1.494	1.451	1.409
86	1.454	1.412	1.371
87	1.415	1.374	1.333
88	1.378	1.337	1.297
89	1.341	1.301	1.262
90	1.306	1.266	1.228
91	1.271	1.233	1.195
92	1.238	1.200	1.163
93	1.206	1.169	1.132
94	1.175	1.138	1.102
95	1.144	1.108	1.073
96	1.115	1.080	1.045
97	1.087	1.052	1.018
98	1.059	1.025	0.9918
99	1.032	0.9988	0.9663
100	1.006	0.9735	0.9416
101	0.9812	0.9489	0.9175
102	0.9567	0.9250	0.8942
103	0.9330	0.9018	0.8716
104	0.9100	0.8793	0.8496
105	0.8877	0.8575	0.8284
106	0.8660	0.8364	0.8077
107	0.8456	0.8159	0.7877
108	0.8245	0.7960	0.7683
109	0.8047	0.7767	0.7495

EPSON International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.

- HEADQUARTERS -

1960 E. Grand Avenue
El Segundo, CA 90245, U.S.A.
Phone: +1-310-955-5300 Fax: +1-310-955-5400

- SALES OFFICES -

West

150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone: +1-408-922-0200 Fax: +1-408-922-0238

Central

101 Virginia Street, Suite 290
Crystal Lake, IL 60014, U.S.A.
Phone: +1-815-455-7630 Fax: +1-815-455-7633

Northeast

301 Edgewater Place, Suite 120
Wakefield, MA 01880, U.S.A.
Phone: +1-781-246-3600 Fax: +1-781-246-5443

Southeast

3010 Royal Blvd. South, Suite 170
Alpharetta, GA 30005, U.S.A.
Phone: +1-877-EEA-0020 Fax: +1-770-777-2637

EUROPE

EPSON EUROPE ELECTRONICS GmbH

- HEADQUARTERS -

Riesstrasse 15
80992 Munich, GERMANY
Phone: +49-(0)89-14005-0 Fax: +49-(0)89-14005-110

SALES OFFICE

Altstadtstrasse 176
51379 Leverkusen, GERMANY
Phone: +49-(0)2171-5045-0 Fax: +49-(0)2171-5045-10

UK BRANCH OFFICE

Unit 2.4, Doncastle House, Doncastle Road
Bracknell, Berkshire RG12 8PE, ENGLAND
Phone: +44-(0)1344-381700 Fax: +44-(0)1344-381701

FRENCH BRANCH OFFICE

1 Avenue de l'Atlantique, LP 915 Les Conquerants
Z.A. de Courtaboeuf 2, F-91976 Les Ulis Cedex, FRANCE
Phone: +33-(0)1-64862350 Fax: +33-(0)1-64862355

BARCELONA BRANCH OFFICE

Barcelona Design Center

Edificio Prima Sant Cugat
Avda. Alcalde Barrils num. 64-68
E-08190 Sant Cugat del Vallès, SPAIN
Phone: +34-93-544-2490 Fax: +34-93-544-2491

ASIA

EPSON (CHINA) CO., LTD.

28F, Beijing Silver Tower 2# North RD DongSanHuan
ChaoYang District, Beijing, CHINA
Phone: 64106655 Fax: 64107319

SHANGHAI BRANCH

4F, Bldg., 27, No. 69, Gui Jing Road
Caohejing, Shanghai, CHINA
Phone: 21-6485-5552 Fax: 21-6485-0775

EPSON HONG KONG LTD.

20/F., Harbour Centre, 25 Harbour Road
Wanchai, Hong Kong
Phone: +852-2585-4600 Fax: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON TAIWAN TECHNOLOGY & TRADING LTD.

10F, No. 287, Nanking East Road, Sec. 3
Taipei
Phone: 02-2717-7360 Fax: 02-2712-9164
Telex: 24444 EPSONTB

HSINCHU OFFICE

13F-3, No. 295, Kuang-Fu Road, Sec. 2
HsinChu 300
Phone: 03-573-9900 Fax: 03-573-9169

EPSON SINGAPORE PTE., LTD.

No. 1 Temasek Avenue, #36-00
Millenia Tower, SINGAPORE 039192
Phone: +65-337-7911 Fax: +65-334-2716

SEIKO EPSON CORPORATION KOREA OFFICE

50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: 02-784-6027 Fax: 02-767-3677

SEIKO EPSON CORPORATION

ELECTRONIC DEVICES MARKETING DIVISION

Electronic Device Marketing Department

IC Marketing & Engineering Group

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5816 Fax: +81-(0)42-587-5624

ED International Marketing Department Europe & U.S.A.

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5812 Fax: +81-(0)42-587-5564

ED International Marketing Department Asia

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814 Fax: +81-(0)42-587-5110



In pursuit of “**Saving**” **Technology**, Epson electronic devices.
Our lineup of semiconductors, liquid crystal displays and quartz devices
assists in creating the products of our customers’ dreams.
Epson IS energy savings.

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

■ EPSON Electronic Devices Website

<http://www.epson.co.jp/device/>