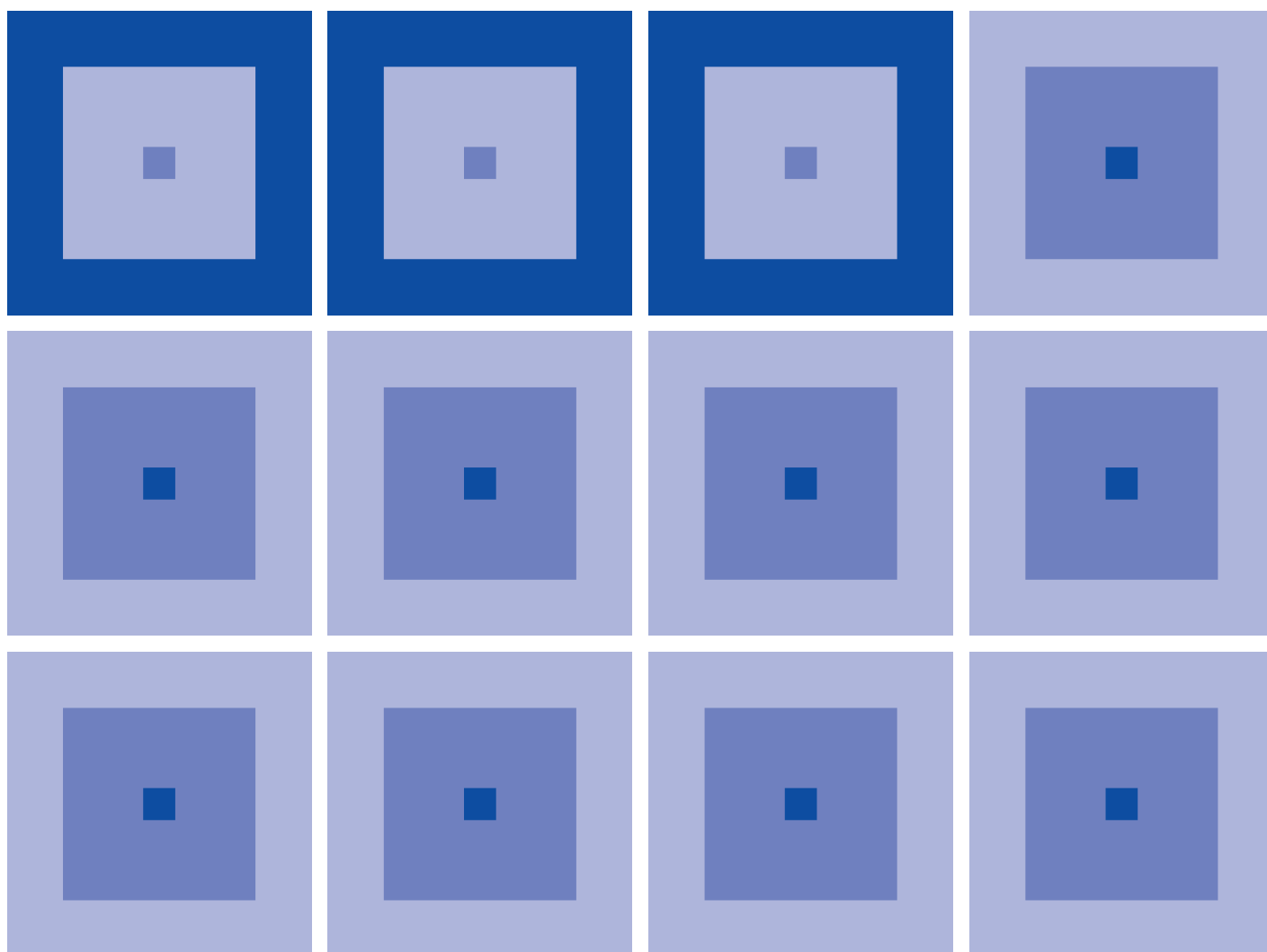


LCD DRIVERS

# S1D16000 Series

## Technical Manual



## NOTICE

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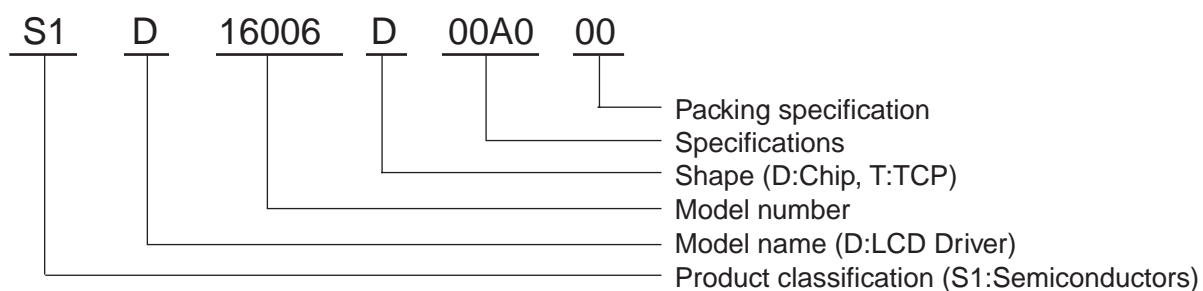
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## The information of the product number change

Starting April 1, 2001 the product number will be changed as listed below. To order from April 1, 2001 please use the new product number. For further information, please contact Epson sales representative.

### Configuration of product number

#### ●DEVICES



### Comparison table between new and previous number

Previous number	New number
SED1606D0A	S1D16006D00A*
SED1606D0B	S1D16006D00B*
SED1606F0A	S1D16006F00A*
SED1606D1A	S1D16006D01A*
SED1606D1B	S1D16006D01B*
SED1640D0B	S1D16400D00B*
SED1651D0A	S1D16501D00A*
SED1670D0A	S1D16700D00A*
SED1670D1A	S1D16700D01A*
SED1670D0B	S1D16700D00B*
SED1670D1B	S1D16700D01B*
SED1672D0A	S1D16702D00A*
SED1672D1A	S1D16702D01A*
SED1672D0B	S1D16702D00B*
SED1672D1B	S1D16702D01B*
SED1672F0A	S1D16702F00A*

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# **Selection Guide**

## S1D16000 (SED1600) series

### ● Segment drivers

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Outputs	Data bus	Package
S1D16006D00A* (SED1606D <sub>0A</sub> )	2.7 to 5.5	8 to 28	1/100 to 1/300	80	4-bit parallel	Al pad chip (for COB)
S1D16006D00B* (SED1606D <sub>0B</sub> )						Au bump chip
S1D16006F00A* (SED1606F <sub>1A</sub> )						QFP5-100pin
S1D16006D01A* (SED1606D <sub>1A</sub> )						Al pad chip (DOFF type)
S1D16006D01B* (SED1606D <sub>1B</sub> )						Au bump chip (DOFF type)
S1D16400D00B* (SED1640D <sub>0B</sub> )	2.7 to 5.5	8 to 28	1/100 to 1/300	80	4-bit parallel	Au bump chip (slim chip)

### ● Common drivers

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Outputs	Package
S1D16501D00A* (SED1651D <sub>0A</sub> )	2.7 to 5.5	8 to 28	1/64 to 1/300	100	Al pad chip (zigzag positioning)
S1D16700D00A* (SED1670D <sub>0A</sub> )	2.7 to 5.5	8 to 28	1/64 to 1/300	100	Al pad chip (INH type)
S1D16700D01A* (SED1670D <sub>1A</sub> )					Al pad chip (DOFF type)
S1D16700D00B* (SED1670D <sub>0B</sub> )					Au bump chip (INH type)
S1D16700D01B* (SED1670D <sub>1B</sub> )					Au bump chip (DOFF type)
S1D16702D00A* (SED1672D <sub>0A</sub> )	2.7 to 5.5	8 to 28	1/64 to 1/300	68	Al pad chip (INH type)
S1D16702D01A* (SED1672D <sub>1A</sub> )					Al pad chip (DOFF type)
S1D16702D00B* (SED1672D <sub>0B</sub> )					Au bump chip (INH type)
S1D16702D01B* (SED1672D <sub>1B</sub> )					Au bump chip (DOFF type)
S1D16702F00A* (SED1672F <sub>0A</sub> )					QFP5-80pin (INH type)

# **S1D16006 Series**

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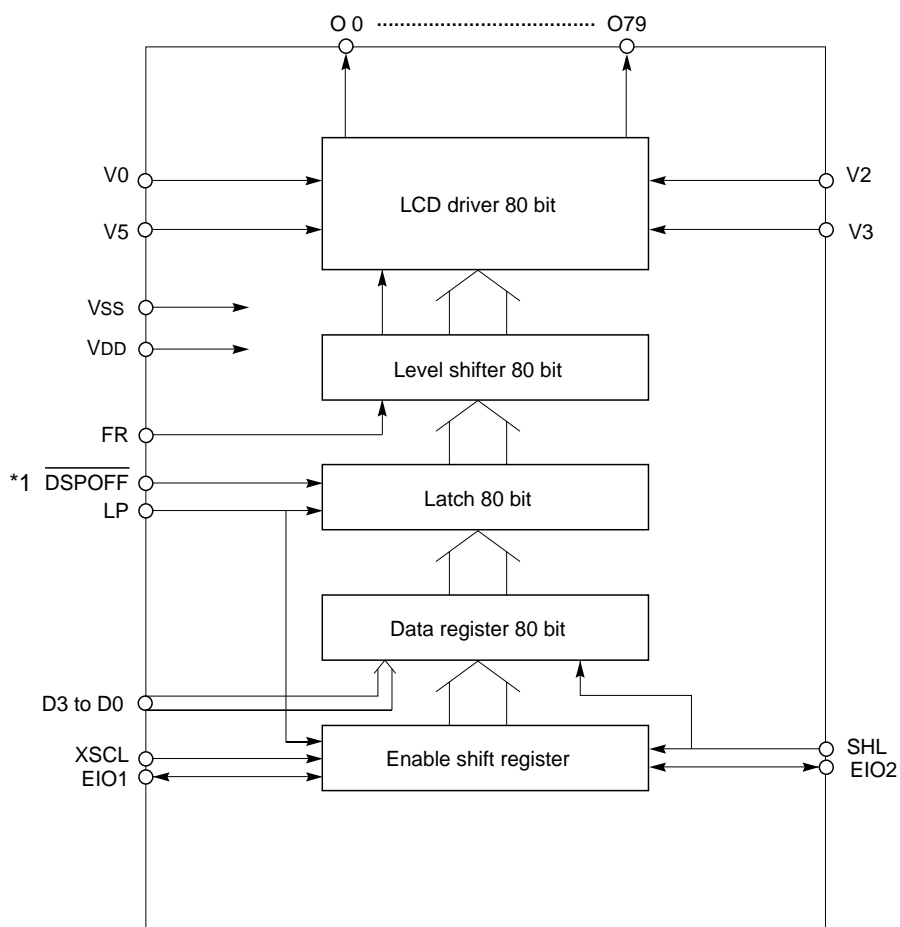
## 1. DESCRIPTION

The S1D16006 Series is an 80 output segment (column) driver which is suitable for driving a very high capacity dot-matrix LCD panels. It is intended to be used in conjunction with the S1D16700/16702 as a pair. The S1D16006 Series is featured in a high quality of picture in LCD display. It employs a high-speed enable chain system which is favorable to a low-power driving. Allowed to be operated with a low voltage in the logic system power supply, it can meet a wide range of applications.

## 2. FEATURES

- Number of LCD drive output segments: 80
- Low current consumption
- Low voltage operation:  $-2.7\text{ V}$  (Max.)
- Wide range of LCD drive voltages:  $-8\text{ V}$  to  $-28\text{ V}$
- High-speed and low-power data transfer enabled by means of a 4-bit bus and chain enable support  
Shift clock frequency:  $6.5\text{ MHz}$  (at  $-2.7\text{ V}$ )  
 $10.0\text{ MHz}$  (at  $-4.5\text{ V}$ )
- Selectable pin output shift direction (S1D16006D01A\*)
- Adjustable offset bias of LCD power to a VDD level
- Logic system power supply :  $-2.7\text{ V}$  to  $-5.5\text{ V}$
- Non-bias display off function
- Chip packaging  
S1D16006D00A\* (AL-pad die form)  
S1D16006D00B\* (Au bump die form)  
S1D16006D01A\* (AL-pad die form)  
S1D16006D01B\* (Au bump die form)  
PKG S1D16006F00A\* (QFP5-100 pin)
- No radial rays countermeasure taken in designing

### 3. BLOCK DIAGRAM



\*1 Dummy terminal NC when S1D16006D00\*\* is used.  
 DSPOFF terminal when S1D16006D01\*\* is used

## 4. PIN DESCRIPTION

Pin name	I/O	Function	Number of pins																																							
O0 ~ O79	O	Segment (column) output for LCD driving The output changes at the LP falling edge.	80																																							
D0 ~ D3	I	Display data input	4																																							
XSCL	I	Display data shift clock input (Falling edge trigger)	1																																							
LP	I	Display data latch pulse input (Falling edge trigger)	1																																							
EIO1, EIO2	I/O	Enable input/output To be set to input or output according to the SHL input level. The output is reset by the LP input. Upon the end of fetching of 80-bit data, the system starts up automatically to HIGH.	2																																							
SHL	I	Shift direction selection and EIO pin I/O control input When data is input to (D3, D2 ... D0 ) pins sequentially in order of (a3, a2, a1, a0), (b3, b2, b1, b0) ... (t3, t2, t1, t0), the relationship between the data and segment output becomes as shown in the table below: <table><tr><th rowspan="2">SHL</th><th colspan="7">O Output</th><th colspan="2">EIO</th></tr><tr><th>79</th><th>78</th><th>77</th><th></th><th>2</th><th>1</th><th>0</th><th>EIO1</th><th>EIO2</th></tr><tr><td>LOW</td><td>a3</td><td>b2</td><td>c1</td><td>...</td><td>t2</td><td>t1</td><td>t0</td><td>Output</td><td>Input</td></tr><tr><td>HIGH</td><td>t0</td><td>t1</td><td>t2</td><td>...</td><td>a1</td><td>a2</td><td>a3</td><td>Input</td><td>Output</td></tr></table> (Note) The relationship between the data and segment output is determined irrespective of the number of shift clock inputs.	SHL	O Output							EIO		79	78	77		2	1	0	EIO1	EIO2	LOW	a3	b2	c1	...	t2	t1	t0	Output	Input	HIGH	t0	t1	t2	...	a1	a2	a3	Input	Output	1
SHL	O Output							EIO																																		
	79	78	77		2	1	0	EIO1	EIO2																																	
LOW	a3	b2	c1	...	t2	t1	t0	Output	Input																																	
HIGH	t0	t1	t2	...	a1	a2	a3	Input	Output																																	
FR	I	LCD drive output AC converted signal input	1																																							
$\overline{\text{DSPOFF}}$	I	Force input of blank V0 level is forcibly set by entering LOW level (available with S1D16006D01** alone).	1																																							
VDD, VSS	Power supply	Logic power supply VDD: 0 V VSS: -2.7 V to -5.5 V	2																																							
V0, V2, V3, V5  *1	Power supply	LCD drive circuit power supply VDD: 0 V V5: -8 V to -28 V VDD ≥ V0 ≥ V2 ≥ 6/9 V5 3/9 V5 ≥ V3 ≥ V5  When used at a same potential, V0 and VDD are used by grounding them close to the IC chip.	4																																							

\*1 Be sure to connect V0 to V5 to their LCD power, respectively.

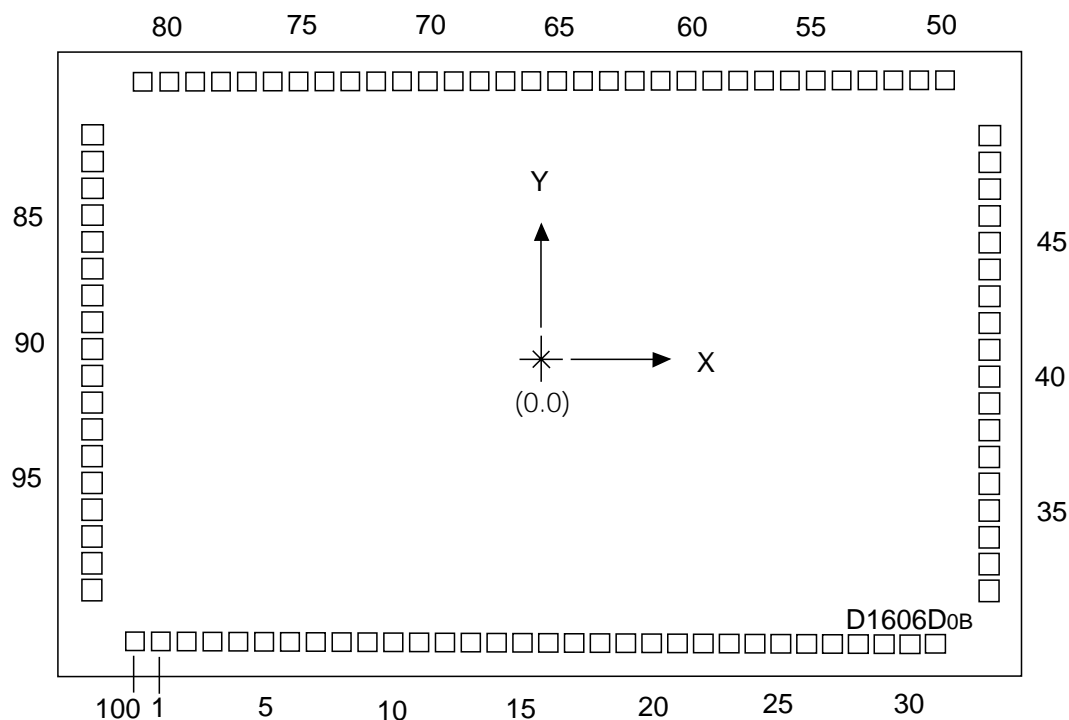
Total: 100

S1D16006D00\*\* (including four NC'4)

S1D16006D01\*\* (including four NC'3)

## 5. PAD

- **Pad Layout**



Chip size: ..... 5.59 mm × 3.50 mm  
Pad pitch: ..... 0.153 mm (Min.)  
Chip thickness: ..... 0.400 mm (AL-pad die form)  
                                0.525 mm (Au-bump die form)

### Au bump specifications [Reference values]

Bump size: 117μm × 109μm ± 20 μm  
Bump height: 17μm to 28μm (Details shall be stipulated in the delivery specification.)

## AL-pad die form

Pad Opening	87×76μm
-------------	---------

## ● Pad center coordinate

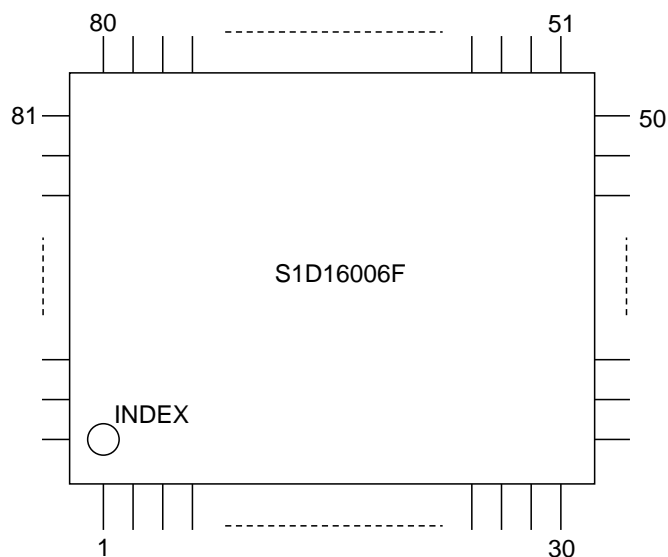
Unit (μm)

PAD		Actual dimensions		PAD		Actual dimensions		PAD		Actual dimensions	
NO.	NAME	X	Y	NO.	NAME	X	Y	NO.	NAME	X	Y
1	O0	-2227	-1578	35	O34	2622	-871	69	O68	-537	1578
2	O1	-2073		36	O35		-713	70	O69	-691	
3	O2	-1920		37	O36		-554	71	O70	-846	
4	O3	-1766		38	O37		-396	72	O71	-998	
5	O4	-1612		39	O38		-238	73	O72	-1152	
6	O5	-1459		40	O39		-79	74	O73	-1305	
7	O6	-1305		41	O40		79	75	O74	-1459	
8	O7	-1152		42	O41		238	76	O75	-1613	
9	O8	-998		43	O42		396	77	O76	-1766	
10	O9	-845		44	O43		554	78	O77	-1920	
11	O10	-691		45	O44		713	79	O78	-2073	
12	O10	-537		46	O45		871	80	O79	-2227	
13	O12	-384		47	O46		1029	81	EIO2	-2381	
14	O13	-230		48	O47		1188	82	D0	-2622	1346
15	O14	-76		49	O48		1346	83	D1		1192
16	O15	77		50	O49	2381	1578	84	D2		1039
17	O16	231		51	O50	2228		85	D3		885
18	O17	384		52	O51	2074		86	Dummy		732
19	O18	538		53	O52	1921		87	Dummy		578
20	O19	692		54	O53	1767		88	Dummy		424
21	O20	845		55	O51	1613		89	*1		271
22	O21	999		56	O55	1460		90	VDD		106
23	O22	1152		57	O56	1306		91	VSS		-58
24	O23	1306		58	O57	1152		92	V0		-224
25	O24	1460		59	O58	999		93	V2		-389
26	O25	1613		60	O59	845		94	V3		-553
27	O26	1767		61	O60	692		95	V5		-718
28	O27	1921		62	O61	538		96	SHL	-2611	-885
29	O28	2074		63	O62	384		97	XSCL		-1039
30	O29	2228		64	O63	231		98	LP		-1192
31	O30	2381		65	O64	77		99	FR		-1346
32	O31	2622	-1346	66	O65	-76		100	EIO1	-2381	-1578
33	O32		-1188	67	O66	-230					
34	O33		-1029	68	O67	-384					

\*1: Pad No.89 is dummy when S1D16006D00\*\* is used.  
It will be  $\overline{\text{DSPOFF}}$  with S1D16006D01\*\*.

## 6. PIN LAYOUT

Package Type: QFP-5 100pin



PIN No.	NAME	PIN No.	NAME	PIN No.	NAME	PIN No.	NAME	PIN No.	NAME
1	O0	21	O20	41	O40	61	O60	81	EIO2
2	O1	22	O21	42	O41	62	O61	82	D0
3	O2	23	O22	43	O42	63	O62	83	D1
4	O3	24	O23	44	O43	64	O63	84	D2
5	O4	25	O24	45	O44	65	O64	85	D3
6	O5	26	O25	46	O45	66	O65	86	NC
7	O6	27	O26	47	O46	67	O66	87	NC
8	O7	28	O27	48	O47	68	O67	88	NC
9	O8	29	O28	49	O48	69	O68	89	*1
10	O9	30	O29	50	O49	70	O69	90	VDD
11	O10	31	O30	51	O50	71	O70	91	VSS
12	O11	32	O31	52	O51	72	O71	92	V0
13	O12	33	O32	53	O52	73	O72	93	V2
14	O13	34	O33	54	O53	74	O73	94	V3
15	O14	35	O34	55	O54	75	O74	95	V5
16	O15	36	O35	56	O55	76	O75	96	SHL
17	O16	37	O36	57	O56	77	O76	97	XSCL
18	O17	38	O37	58	O57	78	O77	98	LP
19	O18	39	O38	59	O58	79	O78	99	FR
20	O19	40	O39	60	O59	80	O79	100	EIO1

\*1: Pad No.89 is dummy when S1D16006D00\*\* is used.  
It will be DSPOFF with S1D16006D01\*\*.

## 7. FUNCTIONAL DESCRIPTION

### Enable shift register

This is a bidirectional shift register with which the shift direction is selected by SHL input. The output of this shift register is used to store the data bus signals to data register.

When the enable signal is in the disable status, the internal clock signal and data bus are fixed to LOW and the system is made into the power save mode.

When using two or more segment drivers, connect the EIO pin of each driver in a cascade arrangement and the EIO pin of the leading driver to VDD.

Since the enable controller circuit automatically detects that the data for 80 bits have been fetched thoroughly and then transfers the enable signal to the controller, it is not necessary to provide the control signal using the control LSI.

### Data register

This is a register used to convert the data bus signal into serial or parallel signal through the enable shift register output. Consequently, the relationship between the serial display data and segment output is determined irrespective of the number of shift clock inputs.

### Latch

This latch is used to fetch the content of data register at the LP falling edge trigger and to send its output to the level shifter.

### Level shifter

This is a level interface circuit used to convert the signal voltage level from the logic system level to LCD drive level.

### LCD driver

This driver outputs the LCD drive voltage.

The relationship among the data bus signal, AC converted signal FR and segment output voltage is as shown in the table below:

(S1D16006D00\*\*)

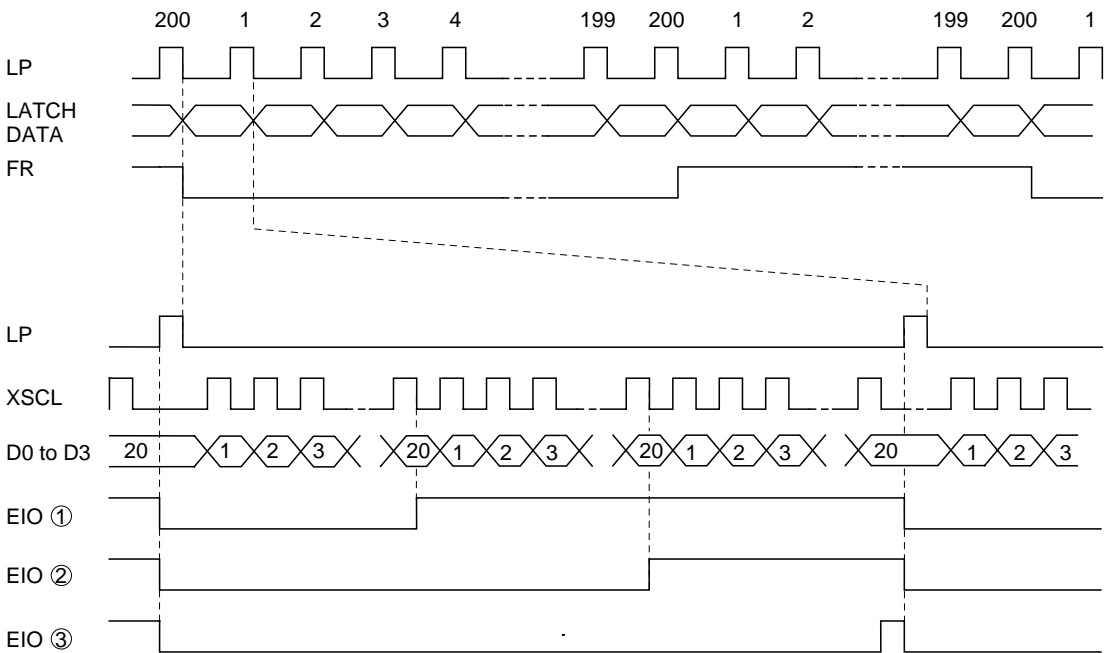
Data bus signal	FR	O output voltage
HIGH	HIGH	V <sub>0</sub>
	LOW	V <sub>5</sub>
LOW	HIGH	V <sub>2</sub>
	LOW	V <sub>3</sub>

(S1D16006D01\*\*)

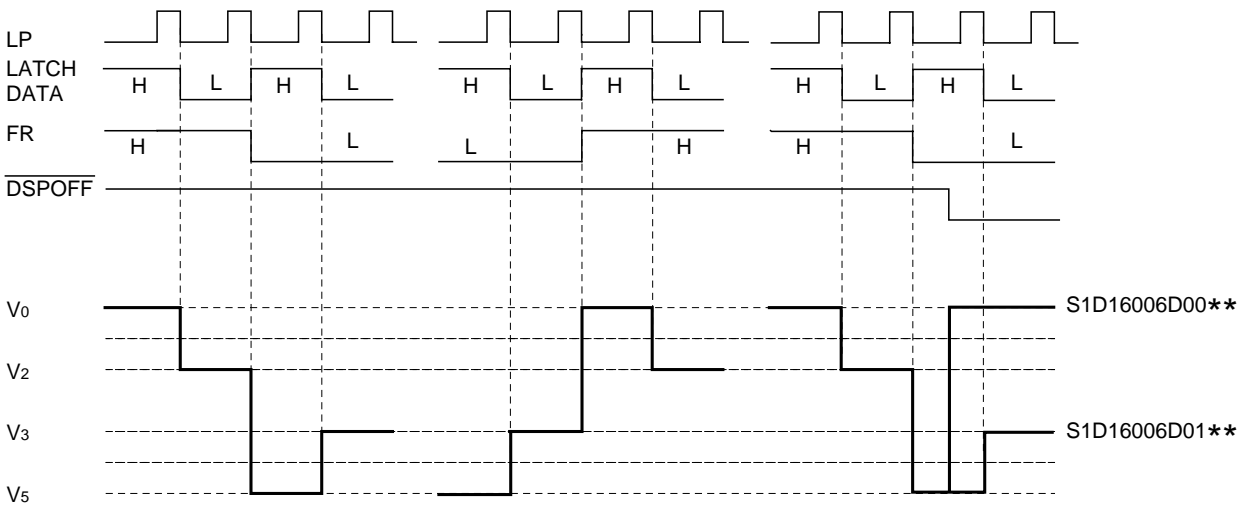
$\overline{\text{DSPOFF}}$	Data bus signal	FR	O output voltage
HIGH	HIGH	HIGH	V <sub>0</sub>
		LOW	V <sub>5</sub>
HIGH	LOW	HIGH	V <sub>2</sub>
		LOW	V <sub>3</sub>
LOW	—	—	V <sub>0</sub>

# 8. TIMING CHART

When the duty is 1/200 (Reference Example)



① to ③ stand for a cascade No. of driver.



When S1D16006D01\*\* is used:  
The driver output is forcibly switched to  
V0 output upon switching of DSPOFF



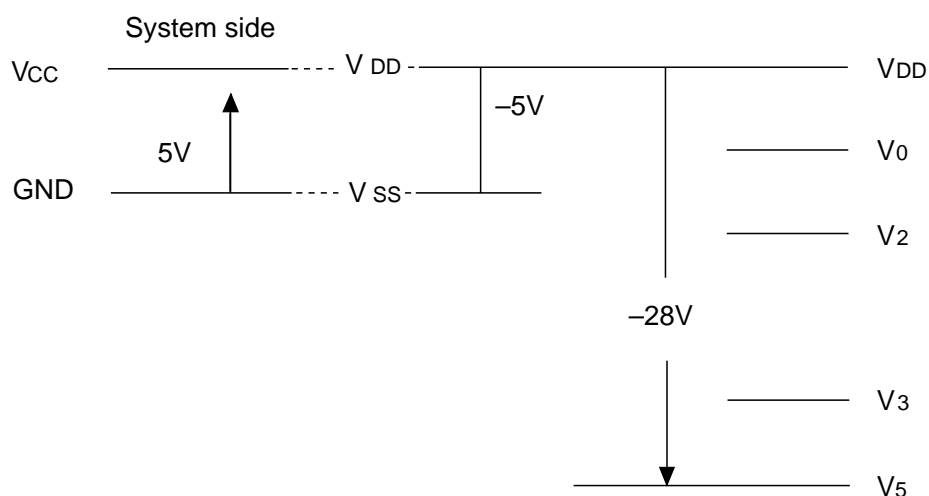
## 9. ABSOLUTE MAXIMUM RATINGS

V<sub>DD</sub>=0V

Parameter	Symbol	Rating	Unit
Power voltage (1)	V <sub>SS</sub>	-7.0 to +0.3	V
Power voltage (2)	V <sub>5</sub>	-30.0 to +0.3	V
Power voltage (3)	V <sub>0</sub> , V <sub>2</sub> , V <sub>3</sub>	V <sub>5</sub> -0.3 to V <sub>DD</sub> +0.3	V
Input voltage	V <sub>I</sub>	V <sub>SS</sub> -0.3 to V <sub>DD</sub> +0.3	V
Output voltage	V <sub>O</sub>	V <sub>SS</sub> -0.3 to V <sub>DD</sub> +0.3	V
EIO output current	I <sub>O</sub>	20	mA
Operating temperature	T <sub>opr</sub>	-40 to + 85	°C
Storing temperature 1	T <sub>stg 1</sub>	-65 to +150	°C

Notes:

1. All the above voltage is based on V<sub>DD</sub> = 0V.
2. The storage temperature 1 stipulates the temperature by unit of a chip.
3. The voltage of V<sub>0</sub>, V<sub>2</sub> and V<sub>3</sub> must always satisfy the condition of V<sub>DD</sub> ≥ V<sub>0</sub> ≥ V<sub>2</sub> ≥ V<sub>3</sub> ≥ V<sub>5</sub>.



4. Floating of the logic system power during while the LCD drive system power is applied, or exceeding V<sub>SS</sub> = -2.6 V can cause permanent damage to the LSI. Functional operation under these conditions is not implied.

Care should be taken to the power supply sequence especially in the system power ON or OFF.

## 10. ELECTRICAL CHARACTERISTICS

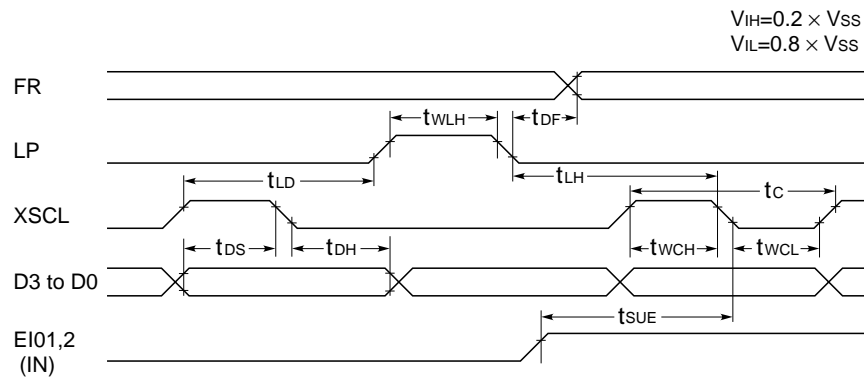
### DC characteristics

Unless otherwise specified,  $V_{DD} = V_0 = 0V$ ,  $V_{SS} = -5.0V \pm 10\%$  and  $T_a = -40$  to  $85^\circ C$ .

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Supply voltage (1)	$V_{SS}$	—	-5.5	-5.0	-2.7	V	$V_{SS}$
Recommended operating voltage	$V_5$	$V_{SS} = -2.7$ to $-5.5V$	-28.0	—	-12.0	V	$V_5$
Operation enable voltage	$V_5$	Function	—	—	-8.0	V	$V_5$
Supply voltage (2)	$V_0$	Recommended value	$V_{DD} - 2.5$	—	$V_{DD}$	V	$V_0$
Supply voltage (3)	$V_2$	Recommended value	$3/9V_5$	—	—	V	$V_2$
Supply voltage (4)	$V_3$	Recommended value	$V_5$	—	$6/9V_5$	V	$V_3$
HIGH input voltage	$V_{IH}$	$V_{SS} = -2.7$ to $-5.5V$	$0.2V_{SS}$	—	—	V	EIO1, EIO2, FR, D0 to D3, XSCL, SHL, LP
LOW input voltage	$V_{IL}$		—	—	$0.8V_{SS}$	V	
HIGH output voltage	$V_{OH}$	$V_{SS} = -2.7$ to $-5.5V$	$I_{OH} = -0.6mA$	—	—	V	EIO1, EIO2
LOW output voltage	$V_{OL}$		$I_{OL} = 0.6mA$	—	$V_{SS} + 0.4$	V	
Input leakage current	$I_{LI}$	$V_{SS} \leq V_{IN} \leq V_{DD}$	—	—	2.0	$\mu A$	D0 to D3, LP, FR XSCL, SHL
Input/output leakage current	$I_{L/O}$	$V_{SS} \leq V_{IN} \leq V_{DD}$	—	—	5.0	$\mu A$	EIO1, EIO2
Static current	$I_{SS}$	$V_5 = -28.0$ to $-14.0V$ $V_{IH} = V_{DD}$ , $V_{IL} = V_{SS}$	—	—	25	$\mu A$	$V_{SS}$
Output resistance	$R_{SEG}$	$\Delta V_{ON} = 0.5V$ $V_5 = -20.0V$ $V_3 = 13/15 \cdot V_5$ $V_2 = 2/15 \cdot V_5$ $V_0 = V_{DD}$ $T_a = 25^\circ C$	—	1.2	1.6	$k\Omega$	O0 to O79
Average operating current consumption (1)	$I_{SS}$	$V_{SS} = -5.0V$ , $V_{IH} = V_{DD}$ $V_{IL} = V_{SS}$ , $f_{XSCL} = 2.69MHz$ $f_{LP} = 16.8KHz$ , $f_{FR} = 70Hz$ Input data: Dice display at no load	—	0.10	0.2	mA	$V_{SS}$
		$V_{SS} = -3.0V$ Other conditions are the same as $V_{SS} = -5V$	—	0.07	0.15		
Average operating current consumption (2)	$I_5$	$V_{SS} = -5.0V$ , $V_0 = 0.0V$ , $V_2 = -9.3V$ $V_3 = -18.6V$ , $V_5 = -28.0V$ Other conditions are the same as in the item of $I_{SS}$ .	—	0.05	0.08	mA	$V_5$
Input pin capacitance	$C_i$	Freq. = 1MHz $T_a = 25^\circ C$	—	—	8	pF	D0 to D3, LP, FR XSCL, SHL
Input/output pin capacitance	$C_{I/O}$	By unit of a chip	—	—	15	pF	EIO1, EIO2

## AC Characteristics

## Input timing characteristics

 $V_{SS}=-5.0V \pm 0.5V$ ,  $T_a=-40$  to  $85^\circ\text{C}$ 

Parameter	Symbol	Condition	Min.	Max.	Unit
XSCL period	$t_c$	—	100	—	ns
XSCL HIGH pulsewidth	$t_{WCH}$	—	30	—	ns
XSCL LOW pulsewidth	$t_{WCL}$	—	30	—	ns
Data setup time	$t_{DS}$	—	20	—	ns
Data hold time	$t_{DH}$	—	10	—	ns
XSCL-rise to LP-rise time	$t_{LD}$	—	0	—	ns
LP-fall to XSCL-fall time	$t_{LH}$	—	40	—	ns
LP HIGH pulsewidth	$t_{WLH}$	*3	40	—	ns
Allowable FR delay time	$t_{DF}$	—	−900	+900	ns
EIO setup time	$t_{SUE}$	—	35	—	ns

 $V_{SS}=-4.5V$  to  $-2.7V$ ,  $T_a=-40$  to  $85^\circ\text{C}$ 

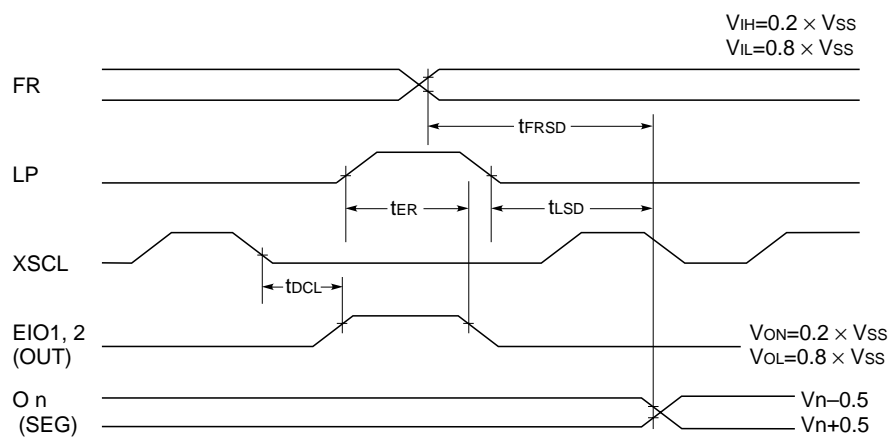
Parameter	Symbol	Condition	Min.	Max.	Unit
XSCL period	$t_c$	$V_{SS}=-2.7V$ *1	153	—	ns
		$V_{SS}=-3.0V$ *2	133	—	
XSCL HIGH pulsewidth	$t_{WCH}$	—	50	—	ns
XSCL LOW pulsewidth	$t_{WCL}$	—	50	—	ns
Data setup time	$t_{DS}$	—	30	—	ns
Data hold time	$t_{DH}$	—	15	—	ns
XSCL-rise to LP-rise time	$t_{LD}$	—	0	—	ns
LP-fall to XSCL-fall time	$t_{LH}$	$V_{SS}=-2.7V$	75	—	ns
		$V_{SS}=-3.0V$	65	—	
LP HIGH pulsewidth	$t_{WLH}$	$V_{SS}=-2.7V$ *3	75	—	ns
		$V_{SS}=-3.0V$ *3	65	—	
Allowable FR delay time	$t_{DF}$	—	−900	+900	ns
EIO setup time	$t_{SUE}$	$V_{SS}=-2.7V$	60	—	ns
		$V_{SS}=-3.0V$	51	—	

\*1 Equivalent to 6.5 MHz

\*2 Equivalent to 7.5 MHz

\*3  $t_{WLH}$  stipulates the time when LP is HIGH and XSCL is LOW.\*4  $t_r$  and  $t_f$  of input signal are stipulated by unit of 20 ns.\*5 At a high-speed operation,  $t_r$  and  $t_f = \{t_c - (t_{DCL} + t_{SUE})\}/2$

## Output timing characteristics


 $V_{DD}=-5.0 \pm 0.5V$ ,  $V_5=-12.0$  to  $-28.0V$ 

Paramant	Symbol	Condition	Min.	Max.	Unit
EIO reset time	$t_{ER}$	$CL=15pF$ (EIO)	—	90	ns
EIO output delay time	$t_{DCL}$		—	55	ns
LP to SEG output delay time	$t_{LSD}$	$CL=100pF$ (On)	—	200	ns
FR to SEG output delay time	$t_{FRSD}$		—	400	ns

 $V_{DD}=-4.5V$  to  $2.7V$ ,  $V_5=-12.0$  to  $-28.0V$ 

Paramant	Symbol	Condition	Min.	Max.	Unit
EIO reset time	$t_{ER}$	$CL=15pF$ (EIO)	—	150	ns
EIO output delay time	$t_{DCL}$	$V_{SS}=-2.7V$	—	88	ns
		$V_{SS}=-3.0V$	—	77	ns
LP to SEG output delay time	$t_{LSD}$	$CL=100pF$ (On)	—	400	ns
FR to SEG output delay time	$t_{FRSD}$		—	800	ns

\*1  $t_r$  and  $t_f$  of input signal are stipulated by unit of 20 ns.

\*2 At a high-speed operation,  $t_r$  and  $t_f = \{t_C - (t_{DCL} + t_{SUE})\}/2$

## 11. LCD DRIVE POWER

### Each voltage level forming method

To obtain each voltage level for LCD driving, it is optimum to divide the resistance of potential between  $V_5$  and  $V_{DD}$  to drive the LCD using the voltage follower with an operational amplifier. In taking into consideration of such a case using the operational amplifier, the maximum potential level  $V_0$  for LCD driving has been made a separate pin from  $V_{DD}$ .

When the potential of  $V_0$  lowers than that of  $V_{DD}$  and the potential difference between the two becomes larger, however, the capacity of LCD drive output driver lowers. To avoid it, use the system with the potential difference of 0 V to 2.5 V between  $V_0$  and  $V_{DD}$ .

When no operational amplifier is used, connect  $V_0$  and  $V_{DD}$  close to the IC chip.

When a series resistance exists in the power supply line of  $V_5$  and  $V_{DD}$ , a voltage drop of  $V_5$  and  $V_{DD}$  occurs at the LSI power supply pin, the relationship with the LCD's intermediate potential ( $V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_5$ ) cannot be met, this causing the LSI to be broken down in some cases. When a protection resistor is inserted, it is necessary to stabilize the voltage by capacitance.

### Note in power ON/OFF

Since this LSI is high in the voltage of LCD driving system, when a high voltage is applied to the LCD driving system with the logic system power supply kept floating or above  $V_{SS} = -2.6$  V, and when the LCD driving signal is output before the applied voltage to the LCD driving system is stabilized, an overcurrent flows and LSI breaks down in some cases.

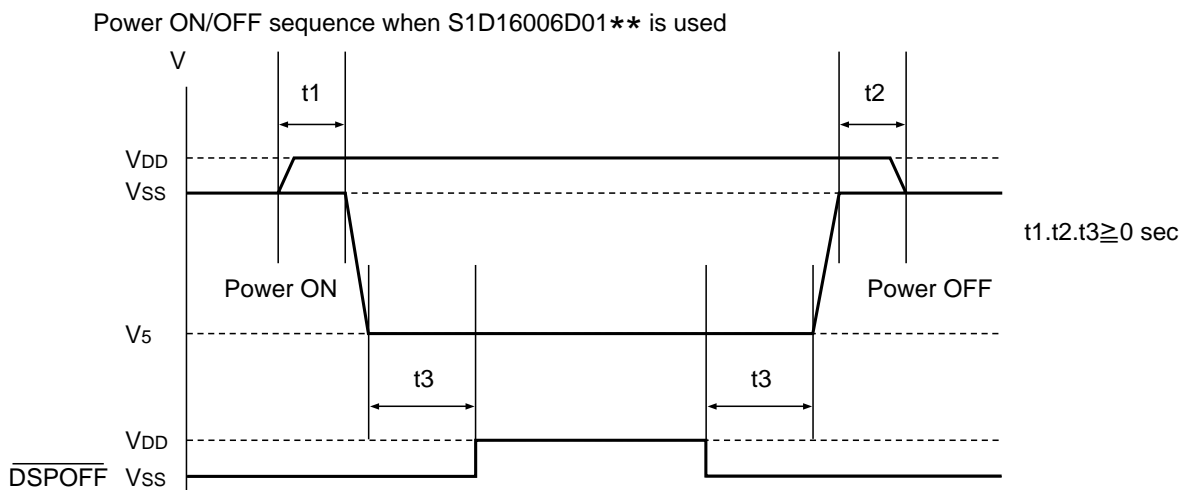
### Be sure to follow the power ON/OFF sequence as shown below:

At power ON ... Logic system ON → LCD driving system ON or simultaneous ON of the both  
At power OFF .. LCD driving system OFF → Logic system OFF or simultaneous OFF of the both

For a countermeasure to such overcurrent, it is effective to put a high-speed melting fuse or protection resistor in series with the LCD power unit.

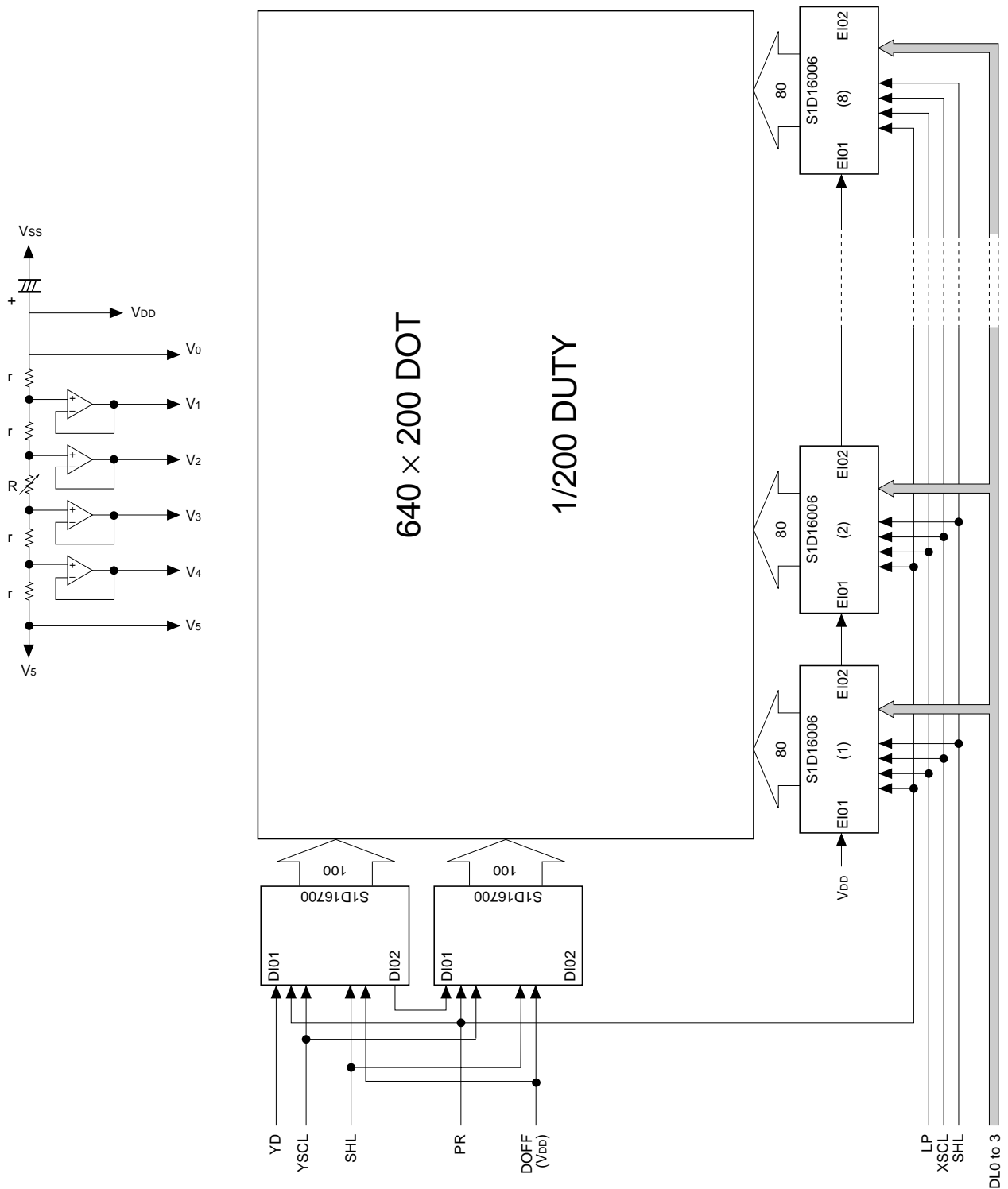
It is then required to select the optimum value in the protection resistance according to the capacitance of LC cell.

Until the LCD driver voltage stabilizes. It is recommended to set the LCD driver output potential to  $V_0$  using the display off function (DSPOFF).



# 12. TYPICAL CIRCUIT DIAGRAM

## Configuration Drawing of Large Screen LCD



**S1D16400**

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10. REGARDING THE LCD DRIVING POWER .....	2-12
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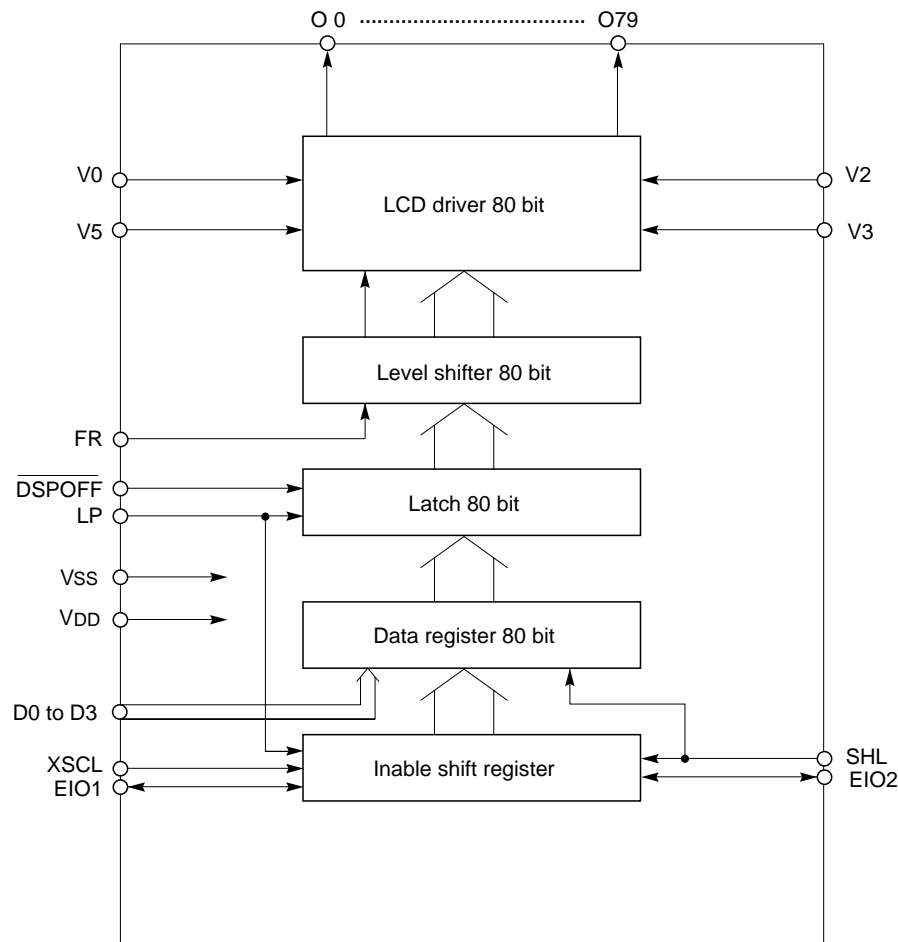
## **1. DESCRIPTION**

The S1D16400 is an 80 output segment (column) driver for use in combination with an S1D16700/16702. It is provided with high-vision measure of the LCD display and adopts high speed inable chain system for low power operation and slim chip shape suitable for minimizing of the LCD panel. Also, low voltage operation of the logic power source suits a wide range of applications.

## **2. FEATURES**

- LCD driver output number : 80
- Ultra-slim chip
- Low current consumption
- Low voltage operation :  $-2.7\text{V}$  Max.
- Wide range of liquid crystal drive voltage :  $-8$  to  $-28\text{V}$
- High speed and low power data transfer is possible by adoption of the 4 bit bus inable chain system.  
Shift clock frequency
  - 6.5MHz (at  $-2.7\text{V}$ )
  - 7.5MHz (at  $-3.0\text{V}$ )
- Non-bias display off function
- Pin selection of the output shift direction is available.
- Offset bias regulation of the liquid crystal power is possible depending on the VDD level.
- Logic system power source :  $-2.7\text{V}$  to  $-5.5\text{V}$
- Product shapes
  - Chip : S1D16400D00B\* (Au bump article)

### 3. BLOCK DIAGRAM



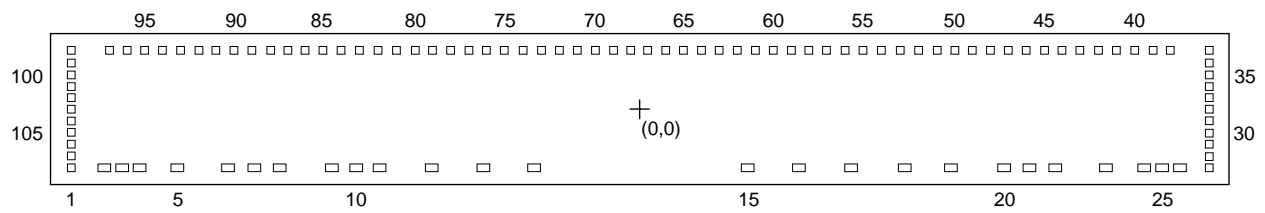
## 4. FUNCTIONS OF THE TERMINALS

Terminal names	I/O	Functions	Numbers of terminals																																							
O0 ~ O79	O	LCD driving segment (column) output. The output level varies by the trailing edge of the LP.	80																																							
D0 ~ D3	I	Display data input	4																																							
XSCL	I	Shift clock input of display data (trailing edge trigger)	1																																							
LP	I	Latch pulse input of display data (trailing edge trigger)	1																																							
EIO1, EIO2	I/O	Inable input and output. Set to input or output depending on the SHL input level. The output is reset by the LP input and, after receiving 80 bit data, it automatically rises to HIGH.	2																																							
SHL	I	Shifting direction choice and input/output controlling input to the EIO terminal. When data are input to (D3, D2 ...D0) terminals in the order of (a,b,c,d,e,f,g,h).....(w,x,y,z), relations between data and segment outputs are as follows: <table border="1"><tr><th rowspan="2">SHL</th><th colspan="7">O Output</th><th colspan="2">EIO</th></tr><tr><th>79</th><th>78</th><th>77</th><th></th><th>2</th><th>1</th><th>0</th><th>EIO1</th><th>EIO2</th></tr><tr><td>LOW</td><td>a</td><td>b</td><td>c</td><td>...</td><td>x</td><td>y</td><td>z</td><td>Output</td><td>Input</td></tr><tr><td>HIGH</td><td>z</td><td>y</td><td>x</td><td>...</td><td>c</td><td>b</td><td>a</td><td>Input</td><td>OUtput</td></tr></table> (Note) Relations between data and segment outputs are determined independent from the shift clock number.	SHL	O Output							EIO		79	78	77		2	1	0	EIO1	EIO2	LOW	a	b	c	...	x	y	z	Output	Input	HIGH	z	y	x	...	c	b	a	Input	OUtput	1
SHL	O Output							EIO																																		
	79	78	77		2	1	0	EIO1	EIO2																																	
LOW	a	b	c	...	x	y	z	Output	Input																																	
HIGH	z	y	x	...	c	b	a	Input	OUtput																																	
FR	I	Input of the alternating signal of the LCD drive output.	1																																							
VDD, VSS	Power source	Power supply for the logics    VDD : 0V 																																								

\*1 Be sure to connect pairs of V0 - V5 to respective LCD power sources.

Total 107  
(including NC5)

# 5. PAD LAYOUT



Chip size ..... 11.59mm x 1.40mm

Pad pitch ..... 105µm (Min.)

Chip thickness ..... 625µm ± 25µm

## Au bump specification (S1D16400D00B<sub>1</sub>) reference values

Bump size	A	160µm × 80µm ± 4µm	(Pad No. 2 ~ 26)
Bump size	B	86µm × 91µm ± 4µm	(Pad No. 1, 27, 37 and 98)
Bump size	C	86µm × 68µm ± 4µm	(Pad No. 28 ~ 36 and 99 ~ 107)
Bump size	D	82µm × 74µm ± 4µm	(Pad No. 38 ~ 97)
Bump height	A ~ D	22.5 ± 5.5µm	(Pad No. 1 ~ 107)

## 6. PAD CENTER COORDINATES

PAD NO.	PAD NAME	X-axis of coordinates	Y-axis of coordinates	PAD NO.	PAD NAME	X-axis of coordinates	Y-axis of coordinates	PAD NO.	PAD NAME	X-axis of coordinates	Y-axis of coordinates
2	V0	-5345	-541	38	O10	5269	553	74	O46	-1161	553
3	V2	-5164		39	O11	5090		75	O47	-1340	
4	V3	-4984		40	O12	4912		76	O48	-1518	
5	V5	-4594		41	O13	4733		77	O49	-1697	
6	Vss	-4091		42	O14	4554		78	O50	-1875	
7	Dummy	-3839		43	O15	4376		79	O51	-2054	
8	SHL	-3587		44	O16	4197		80	O52	-2233	
9	Dummy	-3065		45	O17	4019		81	O53	-2411	
10	Dummy	-2828		46	O18	3840		82	O54	-2590	
11	VDD	-2590		47	O19	3661		83	O55	-2768	
12	DSPOFF	-2086		48	O20	3483		84	O56	-2947	
13	FR	-1583		49	O21	3304		85	O57	-3126	
14	LP	-1079		50	O22	3126		86	O58	-3304	
15	XSCL	1079		51	O23	2947		87	O59	-3483	
16	D0	1583		52	O24	2768		88	O60	-3661	
17	D1	2086		53	O25	2590		89	O61	-3840	
18	D2	2590		54	O26	2411		90	O62	-4019	
19	Dummy	3065		55	O27	2233		91	O63	-4197	
20	D3	3587		56	O28	2054		92	O64	-4376	
21	Dummy	3839		57	O29	1875		93	O65	-4554	
22	Vss	4091		58	O30	1697		94	O66	-4733	
23	V5	4594		59	O31	1518		95	O67	-4912	
24	V3	4984		60	O32	1340		96	O68	-5090	
25	V2	5164		61	O33	1161		97	O69	-5269	
26	V0	5345	▼	62	O34	982		98	O70	-5644	546
27	EIO1	5644	-544	63	O35	804		99	O71		418
28	O0		-426	64	O36	625		100	O72		313
29	O1		-320	65	O37	447		101	O73		207
30	O2		-215	66	O38	268		102	O74		102
31	O3		-109	67	O39	89		103	O75		-4
32	O4		-4	68	O40	-89		104	O76		-109
33	O5		102	69	O41	-268		105	O77		-215
34	O6		207	70	O42	-447		106	O78		-320
35	O7		313	71	O43	-625		107	O79		-426
36	O8		418	72	O44	-804		1	EIO2	▼	-544
37	O9	▼	546	73	O45	-982	▼				

## 7. FUNCTION DESCRIPTIONS

### Inable shift register

The inable shift register is a bidirectional shift register wherewith the shift direction is determined by the SHL inputs and outputs of such shift register are used to store data bus signals to the data register. When inable signals are in the disable state, the internal clock signal and data bus are fixed to LOW to become the power save mode.

When using multiple units of the segment driver, EIO terminals of each driver should be connected by the cascade connection and the EIO terminals of the top end driver should be connected to “VDD”. (Refer to the example of the connection) Since the inable control circuit automatically detects when all the 80 bit data are taken in and automatically transfers the inable signal, control signals from a controlling LSI are not needed.

### Data register

This is a register for serial and parallel conversion of data bus signals by means of the inable shift register output. Consequently, the relations between the serial display data and segment outputs are determined independent from the shift clock input number.

### Latch

It takes in the contents of the data register by means of the trailing edge trigger of the LP to transmit the output to the level shifter.

### Level shifter

This is a level interface circuit to convert the voltage level of signals from logic level to LCD driving level.

### LCD driver

It outputs the LCD drive voltage.

Relations among data bus signals, alternating signals FR and the segment output voltage are given below.

$\overline{\text{DSPOFF}}$	Data bus signals	FR	O Output Voltage
HIGH	HIGH	HIGH	V <sub>0</sub>
		LOW	V <sub>5</sub>
	LOW	HIGH	V <sub>2</sub>
		LOW	V <sub>3</sub>
LOW	—	—	V <sub>0</sub>

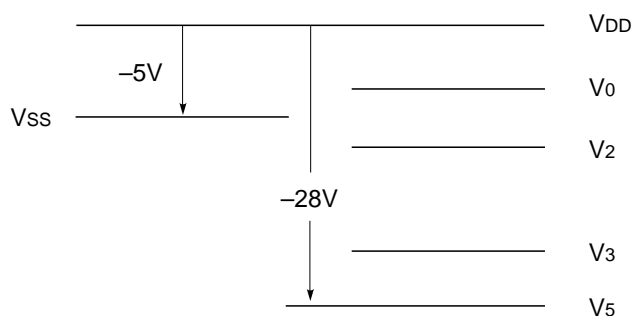
## 8. ABSOLUTE MAXIMUM RATING

Items	Symbols	Ratings	Unit
Power voltage (1)	V <sub>SS</sub>	-7.0 ~ +0.3	V
Power voltage (2)	V <sub>5</sub>	-30.0 ~ +0.3	V
Power voltage (3)	V <sub>0</sub> , V <sub>2</sub> , V <sub>3</sub>	V <sub>5</sub> -0.3 ~ V <sub>DD</sub> +0.3	V
Input voltage	V <sub>I</sub>	V <sub>SS</sub> -0.3 ~ V <sub>DD</sub> +0.3	V
Output voltage	V <sub>O</sub>	V <sub>SS</sub> -0.3 ~ V <sub>DD</sub> +0.3	V
EIO output current	I <sub>O1</sub>	20	mA
Working temperature	T <sub>opr</sub>	-40 ~ +85	°C
Storing temperature 1	T <sub>stg 1</sub>	-65 ~ +150	°C
Storing temperature 2	T <sub>stg 2</sub>	-55 ~ +100	°C

Note 1) All the above voltage is based on V<sub>DD</sub> = 0V.

Note 2) The storing temperature 1 specifies that of chips proper and the storing temperature 2 specifies that of TAB packages.

Note 3) Voltage of V<sub>0</sub>, V<sub>2</sub> and V<sub>3</sub> should always be maintained under a condition of  $V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_5$ .



Note 4) When logic power becomes floating state or if V<sub>SS</sub> = -2.6 or beyond while the LCD driver power source is being applied, the LSI may be permanently damaged and avoid such circumstances. Pay extra attention to the power sequence at times of turning on and turning off the power supply.

## 9. ELECTRICAL CHARACTERISTICS

### DC characteristics

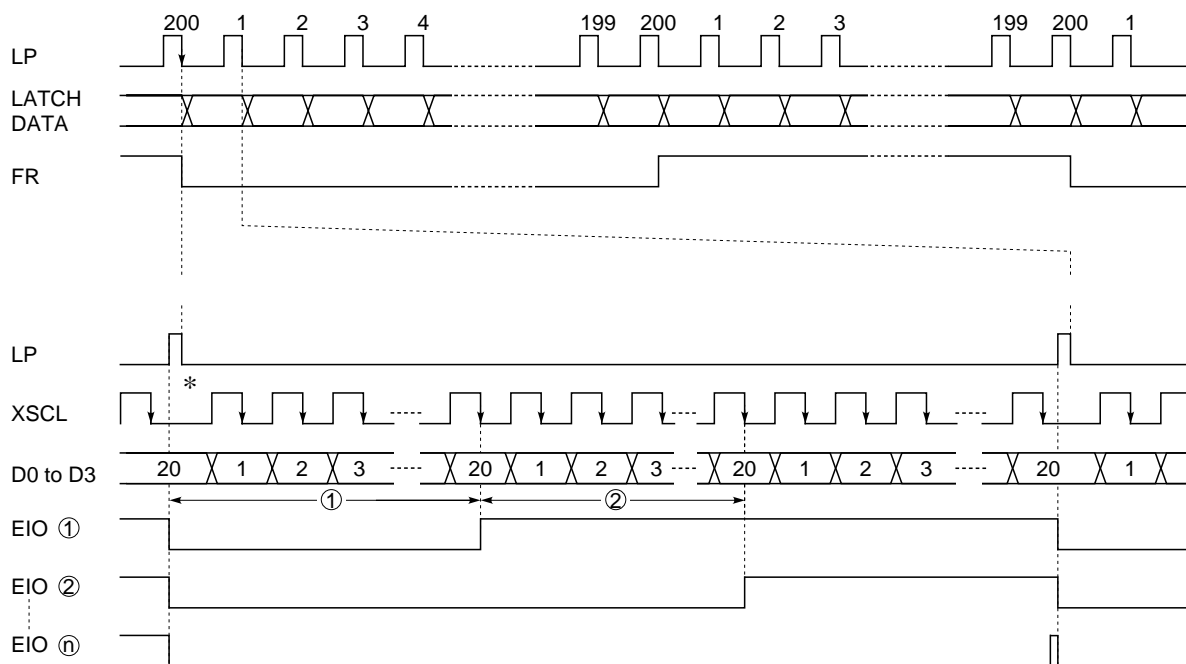
Unless otherwise designated,  $V_{DD} = V_0 = 0V$ ,  $V_{SS} = -5.0V \pm 10\%$  and  $T_a = -40$  to  $85^\circ C$ .

Items	Symbols	Conditions		Applicable terminals	Min.	Typ.	Max.	Unit
Power voltage (1)	V <sub>SS</sub>			V <sub>SS</sub>	−5.5	−5.0	−2.7	V
Recommended operating voltage	V <sub>5</sub>	V <sub>SS</sub> =−2.7 ~ −5.5V		V <sub>5</sub>	−28.0		−12.0	V
Operatable voltage	V <sub>5</sub>	Function		V <sub>5</sub>			-8.0	V
Power voltage (2)	V <sub>0</sub>	Recommended value		V <sub>0</sub>	V <sub>DD</sub> −2.5		V <sub>DD</sub>	V
Power voltage (3)	V <sub>2</sub>	Recommended value		V <sub>2</sub>	3/9V <sub>5</sub>			V
Power voltage (4)	V <sub>3</sub>	Recommended value		V <sub>3</sub>	V <sub>5</sub>		6/9V <sub>5</sub>	V
High level input voltage	V <sub>IH</sub>	V <sub>SS</sub> =−2.7 ~ −5.5V		EIO1, EIO2, FR, D0 ~ D3, XSCL, SHL, LP, DSPOFF	0.2V <sub>SS</sub>			V
Low level input voltage	V <sub>IL</sub>						0.8V <sub>SS</sub>	V
High level output	V <sub>OH</sub>	V <sub>SS</sub> =−2.7 ~ −5.5V	I <sub>OH</sub> =−0.6mA	EIO1, EIO2	V <sub>DD</sub> −0.4			V
Low level output voltage	V <sub>OL</sub>		I <sub>OL</sub> =0.6mA				V <sub>SS</sub> +0.4	V
Input leak current	I <sub>LI</sub>	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>		D0 ~ D3, LP, FR XSCL, SHL, DSPOFF			2.0	μA
Input and output leak current	I <sub>LI/O</sub>	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>		EIO1, EIO2			5.0	μA
Rest current	I <sub>SS</sub>	V <sub>5</sub> =−28.0 ~ −14.0V V <sub>IH</sub> =V <sub>DD</sub> , V <sub>IL</sub> =V <sub>SS</sub>		V <sub>SS</sub>			25	μA
Output resistance	R <sub>SEG</sub>	ΔV <sub>ON</sub> =0.5V V <sub>5</sub> =−20.0V V <sub>3</sub> =13/15•V <sub>5</sub> V <sub>2</sub> =2/15•V <sub>5</sub> V <sub>0</sub> =V <sub>DD</sub>		0 0 ~ 0 79		1.5	2.5	kΩ
Average operating current consumption (1)	I <sub>SS</sub>	V <sub>SS</sub> =−5.0V, V <sub>IH</sub> =V <sub>DD</sub> V <sub>IL</sub> =V <sub>SS</sub> , f <sub>XSCL</sub> =2.69MHz f <sub>LP</sub> =16.8KHz, f <sub>FR</sub> =70Hz Input data: Diced display no-load		V <sub>SS</sub>		0.10	0.2	mA
		V <sub>SS</sub> =−3.0V Other conditions are the same as with V <sub>SS</sub> =−5V				0.07	0.15	
Average operating current consumption (2)	I <sub>5</sub>	V <sub>SS</sub> =−5.0V, V <sub>0</sub> =0.0V, V <sub>2</sub> =−9.3V, V <sub>3</sub> =−18.6V, V <sub>5</sub> =−28.0V Other conditions are the same as with the item I <sub>SS</sub> .		V <sub>5</sub>		0.02	0.05	mA
Input terminal capacity	C <sub>I</sub>	Freq.=1MHz Ta=25°C Chips proper		D0 ~ D3, LP, FR, XSCL, SHL, DSPOFF			8	pF
Input and output terminal capacity	C <sub>I/O</sub>			EIO1, EIO2			15	pF



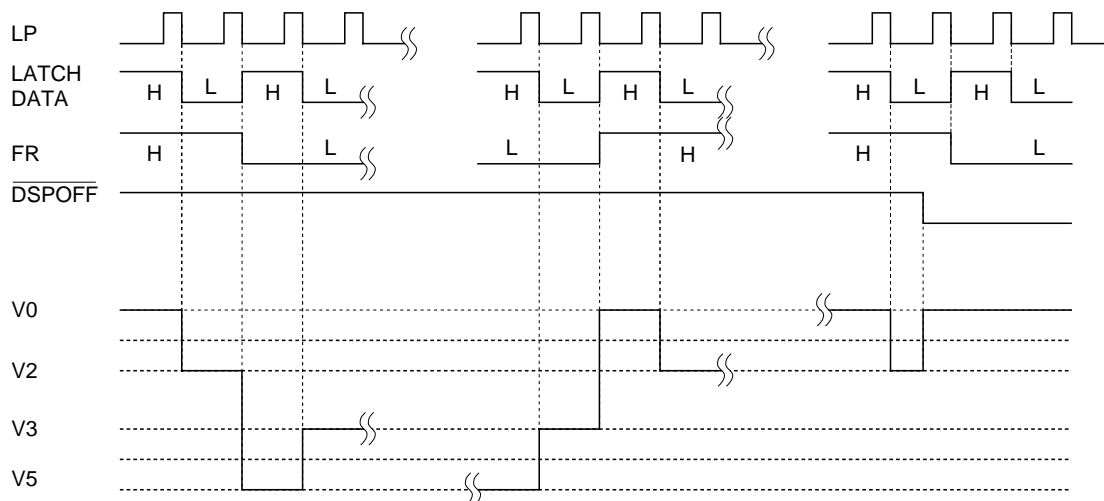
## Timing Diagram

### In case of 1/200 duty (an example)



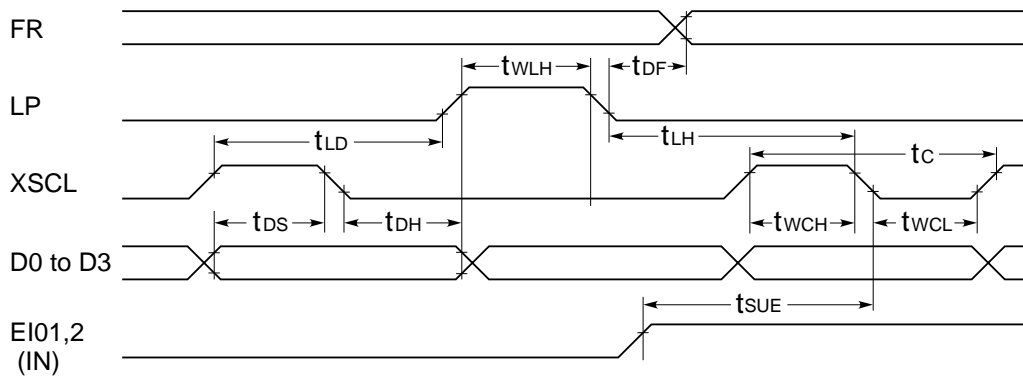
① ~ ③ indicate the cascade numbers of drivers.

\* In case of high speed data transfer, it is necessary to secure a longer XSCS cycle in the timing of the LP pulse insertion in order to maintain the specified value of LP → XSCS (t<sub>LH</sub>).



## AC Characteristics

## Input timing characteristics


 $V_{SS} = -5.0V \pm 0.5V$ ,  $T_a = -40 \sim 85^\circ\text{C}$ 

Items	Symbols	Conditions	Min.	Max.	Unit
XSCL cycle	$t_c$		100		ns
XSCL HIGH level pulse duration	$t_{WCH}$		30		ns
XSCL LOW level pulse duration	$t_{WCL}$		30		ns
Data setup time	$t_{DS}$		30		ns
Data hold time	$t_{DH}$		20		ns
XSCL → LP rise time	$t_{LD}$		0		ns
LP → XSCL fall time	$t_{LH}$		40		ns
LP HIGH level pulse duration	$t_{WLH}$	*3	40		ns
FR delay permissible time	$t_{DF}$		-900	+900	ns
EIO setup time	$t_{SUE}$		35		ns

 $V_{SS} = -4.5V \sim -2.7V$ ,  $T_a = -40 \sim 85^\circ\text{C}$ 

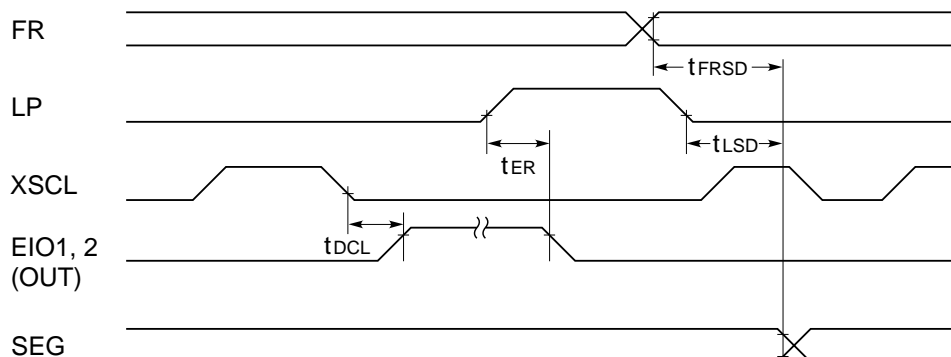
Items	Symbols	Conditions	Min.	Max.	Unit
XSCL cycle	$t_c$	$V_{SS} = -2.7V$ *1	153		ns
		$V_{SS} = -3.0V$ *2	133		
XSCL HIGH level pulse duration	$t_{WCH}$		50		ns
XSCL LOW level pulse duration	$t_{WCL}$		50		ns
Data setup time	$t_{DS}$		50		ns
Data hold time	$t_{DH}$		30		ns
XSCL → LP rise time	$t_{LD}$		0		ns
LP → XSCL fall time	$t_{LH}$	$V_{SS} = -2.7V$	75		ns
		$V_{SS} = -3.0V$	65		
LP HIGH level pulse duration	$t_{WLH}$	$V_{SS} = -2.7V$ *3	75		ns
		$V_{SS} = -3.0V$ *3	65		
FR delay permissible time	$t_{DF}$		-900	+900	ns
EIO setup time	$t_{SUE}$	$V_{SS} = -2.7V$	50		ns
		$V_{SS} = -3.0V$	40		

\*1 6.5MHz equivalence

\*2 7.5MHz equivalence

\*3  $t_{WLH}$  specifies the time when LP is HIGH and, at the same time, XSCL is LOW.

## Output timing characteristics


 $V_{DD} = -5.0 \pm 0.5V$ ,  $V_5 = -12.0 \sim -28.0V$ 

Items	Symbols	Conditions	Min.	Max.	Unit
EIO reset time	$t_{ER}$	CL=15pF (EIO)		90	ns
EIO output delay time	$t_{DCL}$			55	ns
LP → SEG output delay time	$t_{LSD}$	CL=100pF (0n)		200	ns
FR → SEG output delay time	$t_{FRSD}$			400	ns

 $V_{DD} = -4.5V \sim 2.7V$ ,  $V_5 = -12.0 \sim -28.0V$ 

Items	Symbols	Conditions	Min.	Max.	Unit
EIO reset time	$t_{ER}$	CL=15pF (EIO)		150	ns
EIO output delay time	$t_{DCL}$	$V_{SS} = -2.7V$		95	ns
		$V_{SS} = -3.0V$		85	ns
LP → SEG output delay time	$t_{LSD}$	CL=100pF (0n)		400	ns
FR → SEG output delay time	$t_{FRSD}$			800	ns

## 10. REGARDING THE LCD DRIVING POWER

### Methods to obtain necessary voltage levels

In order to obtain necessary voltage levels for driving of the LCD, it should be the best to divide the potential between V5 VDD resistively to drive by means of the voltage follower by the operation amplifier. In consideration of the case of using the operation amplifier, the maximum potential level V0 and VDD should be separated to independent terminals.

Nevertheless, if V0 potential drops below the VDD potential increasing the potential difference, the capacity of the LCD driver decreases and, therefore, it is suggested that the potential difference between V0 ~ VDD be maintained within 0V ~ 2.5V. When the operation amplifier is not used, V0 and VDD should be connected.

As shown in the example of the connection, when using the resistive divider, set the resistance as low as the power capacity of the system allows.

When a series resistance exist in the power line of V5 (VDD), voltage drop of V5 (VDD) at the LSI current end occurs by I5 at times of signal changes and it becomes unable to maintain the relations of the LCD with intermediate potentials ( $VDD \geq V0 \geq V2 \geq V3 \geq V5$ ) leading to breakage of the LSI. When installing protective resistors, it is necessary to stabilize the voltage by their capacity.

### Cautions when turning the power on and off

Since the LCD drive system voltage with this LSI is comparatively high, when high voltage is applied to the LCD drive system leaving the logic power floating or leaving VSS = -2.6V or over or if LCD drive signals are output before the applied voltage to the LCD drive system is stabilized, excess current may flow to break the LSI. It therefore is suggested to bring the potential of the LCD drive output to the V0 level until the LCD drive system voltage gets stabilized using the display-off function (DSPOFF).

### When turning the power on or off, follow the sequence below.

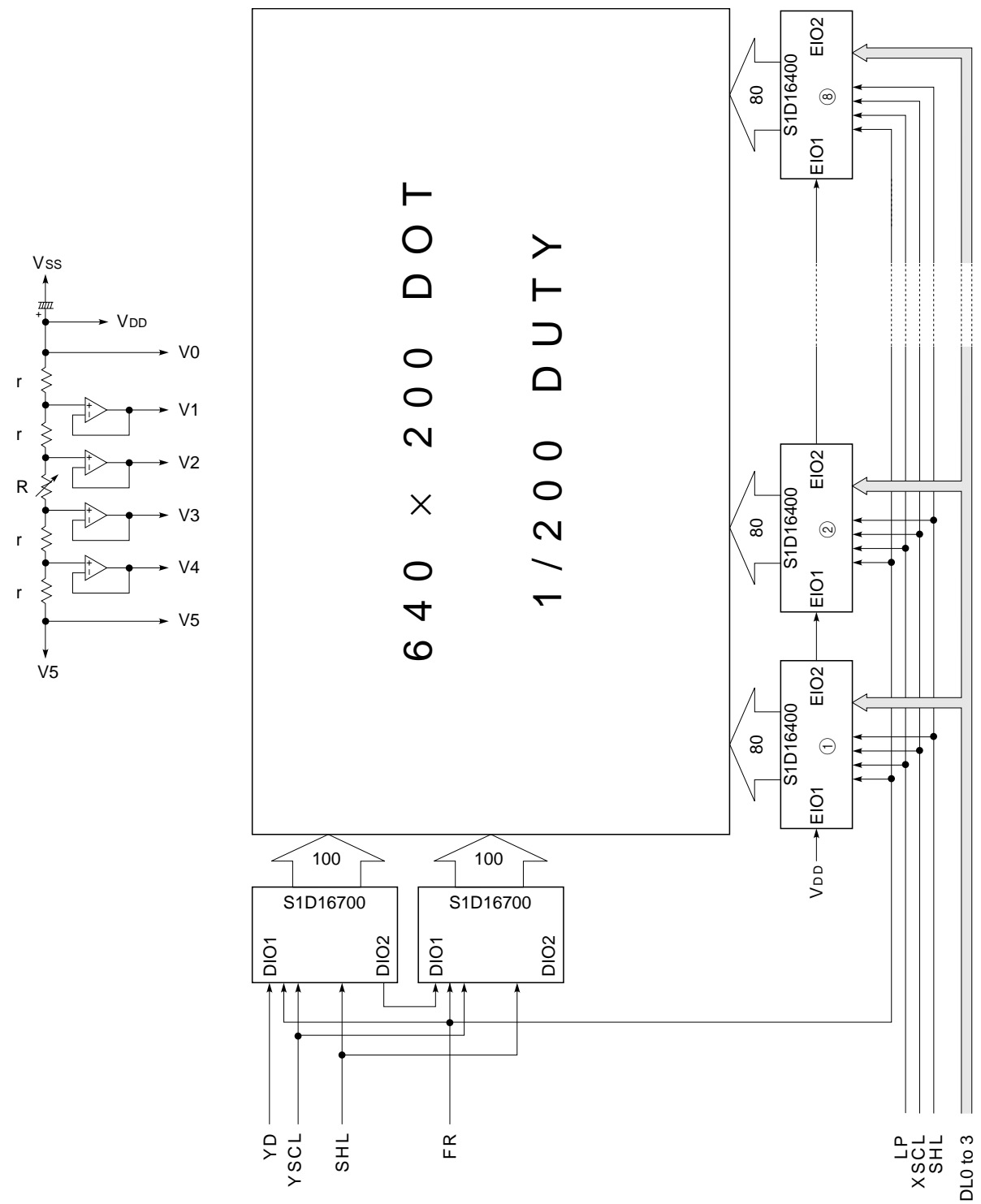
When turning on the power.....Logic systems ON → LCD drive system ON  
(or turn them on simultaneously).

When turning off the power.....LCD drive system OFF → Logic system OFF  
(or turn them off simultaneously).

Insert quick melting fuse in series to the LCD power source for prevention of an excess current flow. It is necessary to choose the optimum value for the protective resistance matching the capacity of the liquid crystal cells.

# 11. AN EXAMPLE OF CONNECTION

Block diagram of a large sized LCD



**S1D16501**

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## **1. DESCRIPTION**

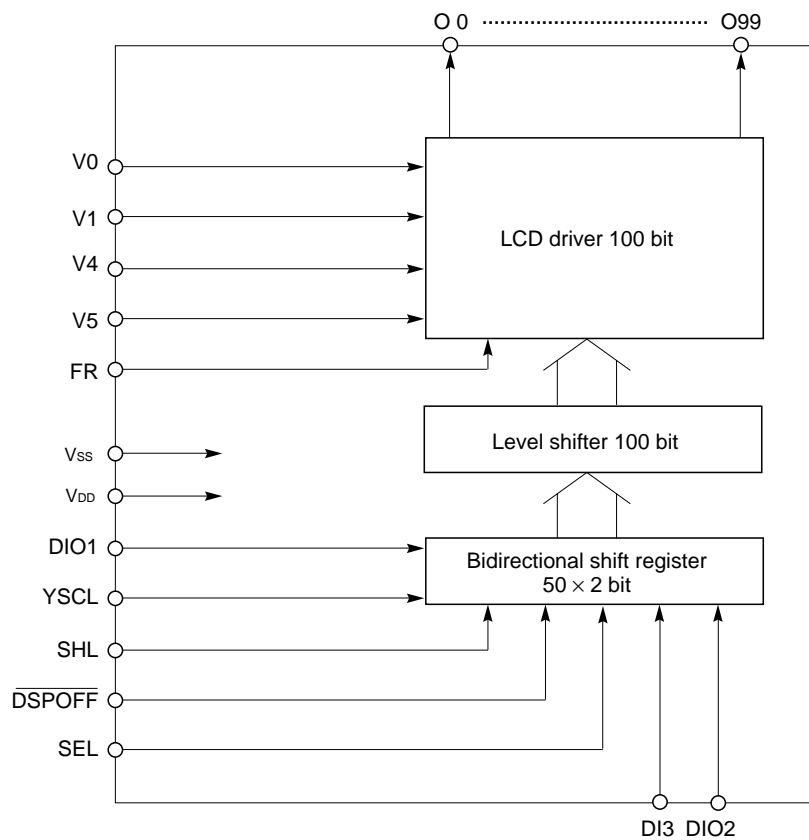
The S1D16501 is a 100 output low-power resistance common (row) driver which is suitable for driving a very high capacity dotmatrix LCD panels. It is intended to be used in conjunction with the S1D16408 as a pair. Since the S1D16501 is so designed to drive LCD's over a wide range of voltages, and also the maximum potential  $V_0$  of its LCD driving bias voltages is isolated from VDD to allow the LCD driving bias voltages to be externally generated optionally with a high accuracy, it can cope with a wide range of LCD panels. Owing to its pad layout which can minimize its PC boards mounting space in addition to its selectable bidirectional driver output sequence and as many as 100 LCD output segments of high pressure resistance and low output impedance, it is possible to obtain the highest driver working efficiency for the 1/200 duty panel.

## **2. FEATURES**

- Number of LCD drive output segments: 100
- Super slim chip configuration
- Common output ON resistance:  $750\Omega$  (Typ.)
- Display capacity ... Possible to display  $640 \times 480$  dots.
- Selectable pin output shift direction
- No bias display OFF function
- Adjustable offset bias of LCD power to VDD level
- Wide range of LCD drive voltages:  $-8\text{ V}$  to  $-28\text{ V}$  (Absolute maximum rated voltage:  $-30\text{ V}$ )
- Logic system power supply:  $-2.7\text{ V}$  to  $-5.5\text{ V}$
- Chip packaging S1D16501D00A\* (AL-pad die form)
- No radial rays countermeasure taken in designing



### 3. BLOCK DIAGRAM



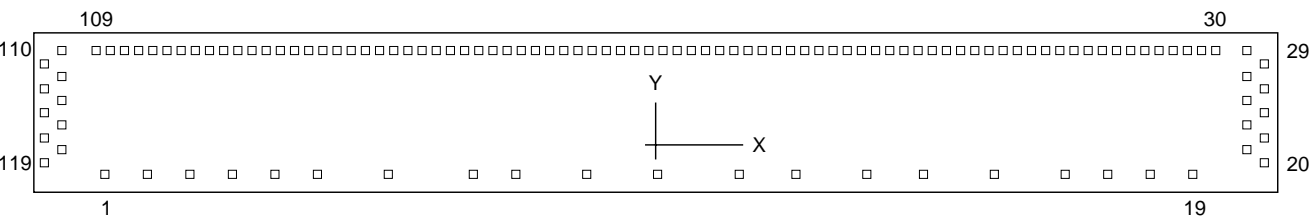
## 4. PIN DESCRIPTION

Pin name	I/O	Function	Number of pins															
O0 to O99	O	LCD drive common (row) output The output changes at the YSCL falling edge.	80															
DIO1 DIO2	I/O	50 × 2 bits bidirectional shift register serial data input/output To be set to input or output according to the SHL input The output changes at the YSCL falling edge.	2															
DI3	I	This is the input pin of scanning pulse in the 50 × 2 bits configuration. When SEL = LOW, the DI3 pin to Vss or GND.	1															
SEL	I	Selection input of bidirectional shift register operating mode HIGH ... 50 × 2 (DI3 input) LOW ... 100	1															
YSCL	I	Serial data shift clock input The scanning data is shifted at the falling edge.	1															
SHL	I	Shift direction selection and DIO pin I/O control input <table border="1"><tr><td>SHL</td><td colspan="2">O output shift direction</td><td>DIO1</td><td>DIO2</td></tr><tr><td>LOW</td><td>0 → 49</td><td>50 → 99</td><td>Input</td><td>Output</td></tr><tr><td>HIGH</td><td>99 → 50</td><td>49 → 0</td><td>Ourput</td><td>Input</td></tr></table> When SEL = HIGH, the DI3 input is set to O50 (SHL = LOW) or O49 (SHL = HIGH). When SEL = LOW, the D13 input is ignored and the DIO inputs are shifted continuously.	SHL	O output shift direction		DIO1	DIO2	LOW	0 → 49	50 → 99	Input	Output	HIGH	99 → 50	49 → 0	Ourput	Input	1
SHL	O output shift direction		DIO1	DIO2														
LOW	0 → 49	50 → 99	Input	Output														
HIGH	99 → 50	49 → 0	Ourput	Input														
$\overline{\text{DSPOFF}}$	I	LCD display blanking control input When LOW is input, the content of shift register is cleared and all common outputs become the V <sub>0</sub> level instantaneously.	1															
FR	I	LCD drive output converted signal input	1															
V <sub>DD</sub> , V <sub>SS</sub>	Power supply	Logic power supply      V <sub>DD</sub> : 0 V (GND)    V <sub>SS</sub> : -2.7 V to -5.5 V	3															
V <sub>0</sub> , V <sub>1</sub> , V <sub>4</sub> V <sub>5</sub>	Power supply	LCD drive power supply    V <sub>5</sub> : -8 V to -28 V V <sub>DD</sub> ≥ V <sub>0</sub> ≥ V <sub>1</sub> ≥ V <sub>4</sub> ≥ V <sub>5</sub>	8															

Respectively  
Total: 119

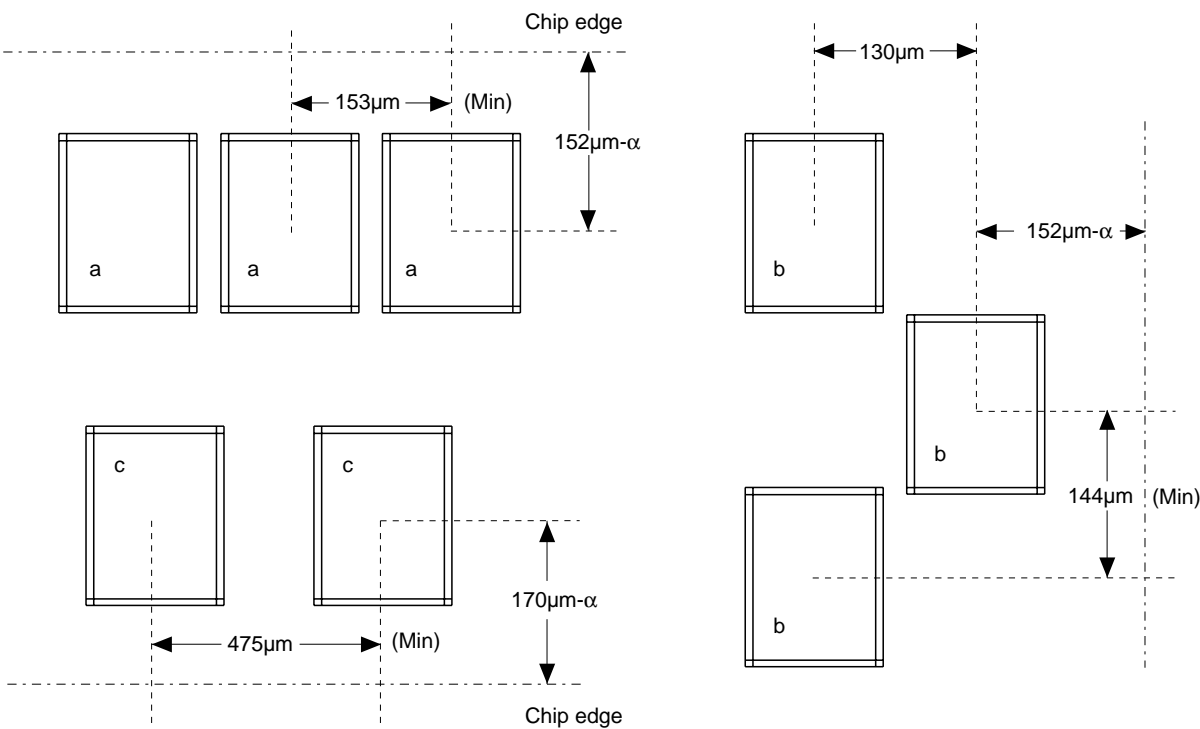
# 5. PAD

## • Pad layout



Chip size: ..... 13.43 mm × 1.76 mm  
 Chip thickness: ..... 400 μm (Typ.)

## AL pad specifications (S1D16501D00A\*)



Pad	a	Opening (X, Y)	110 × 110μm	PAD No 30 to 109
Pad	b	Opening (X, Y)	110 × 110μm	PAD No 20 to 29, 110 to 119
Pad	c	Opening (X, Y)	110 × 110μm	PAD No 1 to 19

## ● Pad center coordinates

Unit (μm)

PAD		Actual dimensions		PAD		Actual dimensions		PAD		Actual dimensions	
NO.	NAME	X	Y	NO.	NAME	X	Y	NO.	NAME	X	Y
1	DIO2	-5985	-709	43	O23	4078	727	85	O65	-2385	727
2	V0	-5510		44	O24	3924		86	O66	-2539	
3	V1	-5035		45	O25	3771		87	O67	-2693	
4	V4	-4560		46	O26	3617		88	O68	-2847	
5	V5	-4038		47	O27	3463		89	O69	-3001	
6	Vss	-3164		48	O28	3309		90	O70	-3155	
7	SEL	-2280		49	O29	3155		91	O71	-3309	
8	SHL	-1767		50	O30	3001		92	O72	-3463	
9	DI3	-1064		51	O31	2847		93	O73	-3617	
10	YSCL	-181		52	O32	2693		94	O74	-3771	
11	VDD	770		53	O33	2539		95	O78	-3924	
12	DSPOFF	1283		54	O34	2385		96	O76	-4078	
13	FR	2176		55	O35	2232		97	O77	-4232	
14	Vss	2879		56	O36	2078		98	O78	-4386	
15	V5	3753		57	O37	1924		99	O79	-4540	
16	V4	4560		58	O38	1770		100	O80	-4694	
17	V1	5035		59	O39	1616		101	O81	-4848	
18	V0	5510		60	O40	1462		102	O82	-5002	
19	DIO1	5985		61	O41	1308		103	O83	-5156	
20	O0	6560	-610	62	O42	1154		104	O84	-5310	
21	O1	6430	-466	63	O43	1000		105	O85	-5463	
22	O2	6560	-321	64	O44	846		106	O86	-5617	
23	O3	6430	-177	65	O45	693		107	O87	-5771	
24	O4	6560	-32	66	O46	539		108	O88	-5925	
25	O5	6430	112	67	O47	385		109	O89	-6079	
26	O6	6560	257	68	O48	231		110	O90	-6430	690
27	O7	6430	401	69	O49	77		111	O91	-6560	545
28	O8	6560	545	70	O50	-77		112	O92	-6430	401
29	O9	6430	690	71	O51	-231		113	O93	-6560	257
30	O10	6079	727	72	O52	-385		114	O94	-6430	112
31	O11	5925		73	O53	-539		115	O95	-6560	-32
32	O12	5771		74	O54	-693		116	O96	-6430	-177
33	O13	5617		75	O55	-846		117	O97	-6560	-321
34	O14	5463		76	O55	-1000		118	O98	-6430	-466
35	O15	5310		77	O57	-1154		119	O99	-6560	-610
36	O16	5156		78	O58	-1308					
37	O17	5002		79	O59	-1462					
38	O18	4848		80	O60	-1616					
39	O19	4694		81	O61	-1770					
40	O20	4540		82	O62	-1924					
41	O21	4386		83	O63	-2078					
42	O22	4232		84	O64	-2232					

## 6. FUNCTIONAL DESCRIPTION

### Shift register

This is a bidirectional shift register to transfer common data.

Being a  $50 \times 2$  bits configuration, this register can select  $50 \times 2$  bits or 100 bits according to the status of SEL. When the  $50 \times 2$  bits configuration is selected, the input of the 50-bit shift register becomes D13.

### Level shifter

This is a level interface circuit used to convert the signal voltage level from the logic system level to LCD drive level.

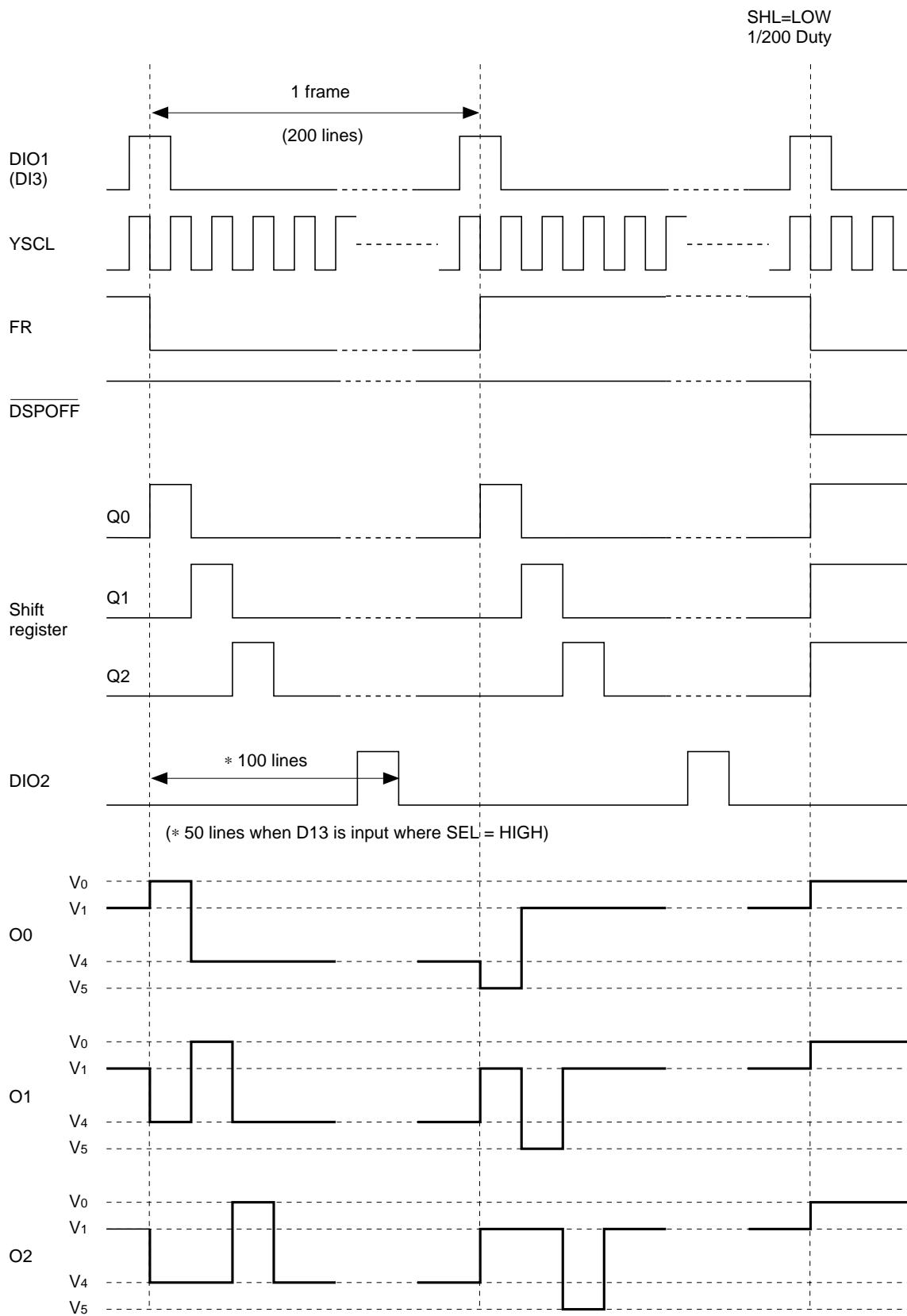
### LCD driver

This driver outputs the LCD drive voltage.

The relationship among the display blanking signal  $\overline{\text{DSPOFF}}$ , contents of shift register, AC converted signal FR and On output voltage is as shown in the table below:

$\overline{\text{DSPOFF}}$	Content of shift register	FR	O output voltage	
HIGH	HIGH	HIGH	V5	(Select level)
		LOW	V0	
	LOW	HIGH	V1	(Non-select level)
		LOW	V4	
LOW	—	—	V0	—

## 7. TIMING CHART



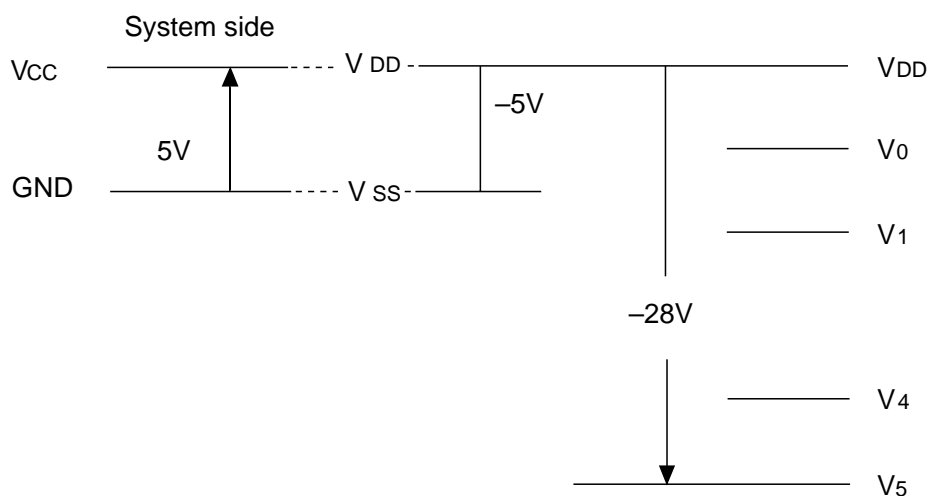
## 8. ABSOLUTE MAXIMUM RATINGS

V<sub>DD</sub>=0V

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V <sub>SS</sub>	−7.0 to +0.3	V
Supply voltage (2)	V <sub>5</sub>	−30.0 to +0.3	V
Supply voltage (3)	V <sub>0</sub> , V <sub>1</sub> , V <sub>4</sub>	V <sub>5</sub> −0.3 to +0.3	V
Input voltage	V <sub>I</sub>	V <sub>SS</sub> −0.3 to +0.3	V
Output voltage	V <sub>O</sub>	V <sub>SS</sub> −0.3 to +0.3	V
Output current (1)	I <sub>O</sub>	20	mA
Output current (2)	I <sub>OCOM</sub>	20	mA
Operating temperature	T <sub>opr</sub>	−40 to + 85	°C
Storing temperature 1	T <sub>stg 1</sub>	−65 to +150	°C

Notes\*

1. The voltage of V<sub>0</sub>, V<sub>1</sub>, V<sub>4</sub> and V<sub>5</sub> must always satisfy the condition of V<sub>DD</sub> ≥ V<sub>0</sub> ≥ V<sub>1</sub> ≥ V<sub>4</sub> ≥ V<sub>5</sub>.



2. Floating of the logic system power during while the LCD drive system power is applied, or exceeding V<sub>SS</sub> = −2.6 V or less can cause permanent damage to the LSI. Functional operation under these conditions is not implied.

Care should be taken to the power supply sequence especially in the system power ON or OFF.

## 9. ELECTRICAL CHARACTERISTICS

### DC characteristics

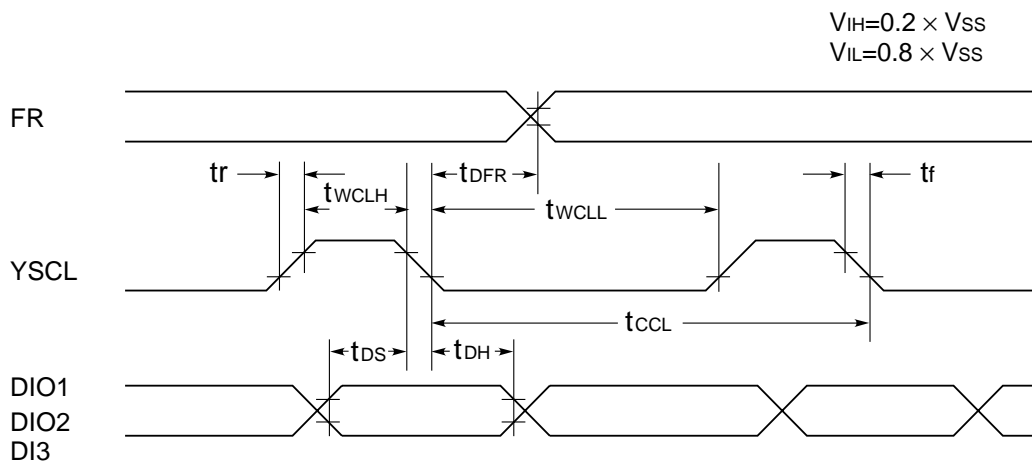
Unless otherwise specified,  $V_{DD} = V_0 = 0V$ ,  $V_{SS} = -5.5V \sim -2.7V$ ,  $T_a = -40$  to  $85^\circ C$ .

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Supply voltage (1)	$V_{SS}$	—	-5.5	-5.0	-2.7	V	$V_{SS}$
Recommended operating voltage	$V_5$	—	-28.0	—	-12.0	V	$V_5$
Operation enable voltage	$V_5$	Functional operation	—	—	-8.0	V	$V_5$
Supply voltage (2)	$V_0$	—	2.5	—	0	V	$V_0$
Supply voltage (3)	$V_1$	—	$2/9 \cdot V_5$	—	$V_{DD}$	V	$V_1$
Supply voltage (4)	$V_4$	—	$V_5$	—	$7/9 \cdot V_5$	V	$V_4$
HIGH input voltage	$V_{IH}$	—	$0.2 \cdot V_{SS}$	—	—	V	DIO1, DIO2, FR, YSCL, SHL, DI3 DSPOFF, SEL
LOW input voltage	$V_{IL}$	—	—	—	$0.8 \cdot V_{SS}$	V	
HIGH output voltage	$V_{OH}$	$I_{OH} = -0.3mA$	$V_{DD} - 0.4$	—	—	V	DIO1, DIO2
LOW output voltage	$V_{OL}$	$I_{OL} = 0.3mA$	—	—	$V_{SS} + 0.4$	V	
Input leakage current	$I_{LI}$	$V_{SS} \leq V_{IN} \leq 0V$	—	—	2.0	$\mu A$	YSCL, SHL, DI3 DSPOFF, FR, SEL
Input/output leakage current	$I_{LI/O}$	$V_{SS} \leq V_{IN} \leq 0V$	—	—	5.0	$\mu A$	DIO1, DIO2
Static current	$I_{DDS}$	$V_5 = -12.0 \sim -28.0V$ $V_{IH} = V_{DD}$ , $V_{IL} = V_{SS}$	—	—	25	$\mu A$	$V_{DD}$
Output resistance	$R_{COM}$	$\Delta V_{ON} = 0.5V$ $V_0 = V_{DD}$ , $V_1 = -1.5V$ $V_4 = -18.5V$ $V_5 = -20.0V$	—	0.75	1.0	$k\Omega$	O0~O99
Average operating current consumption (1)	$I_{SS1}$	$V_{SS} = -5.0V$ , $V_{IH} = V_{DD}$ $V_{IL} = V_{SS}$ , $f_{YSCL} = 12KHz$ Frame frequency = 60Hz Input data: 1/200 $T_a = 25^\circ C$ ?	—	7	15	$\mu A$	$V_{SS}$
		$V_{SS} = -3.0V$ Other conditions are the same as $V_{SS} = -5.0V$	—	5	10		
Average operating current consumption (2)	$I_{SS2}$	$V_{SS} = -5.0V$ , $V_0 = 0V$ , $V_1 = 1.5V$ , $V_4 = 18.5V$ , $V_{EE} = V_5 = -20.0V$ Other conditions are the same as in the item of ISS 1.	—	7	15	$\mu A$	$V_5$
Input pin capacitance	$C_i$	$T_a = 25^\circ C$	—	—	8	pF	YSCL, SHL, DSPOFF, FR, DI3, SEL
Input/output pin capacitance	$C_{I/O}$		—	—	15	pF	DIO1, DIO2



# AC Characteristics

## Input timing characteristics



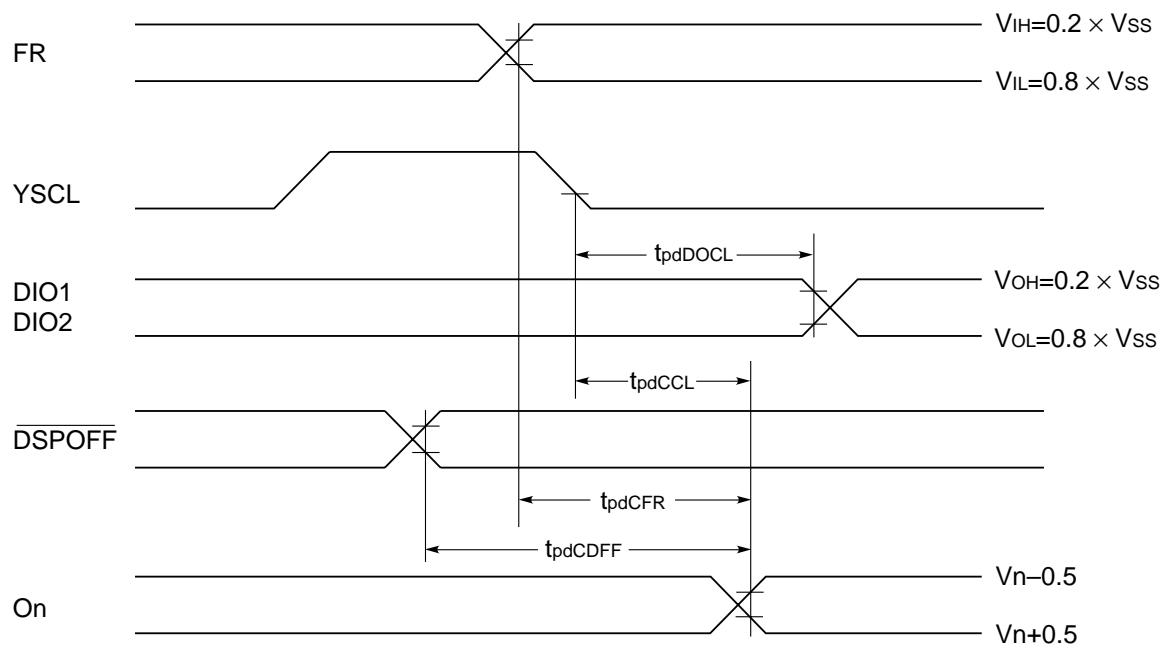
$V_{SS}=-5.0V \pm 0.5V$ ,  $T_a=-40$  to  $85^{\circ}C$

Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	$t_r$	—	—	50	ns
Input signal fall time	$t_f$	—	—	50	ns
YSCL period	$t_{CCL}$	—	500	—	ns
YSCL HIGH pulsewidth	$t_{WCLH}$	—	70	—	ns
YSCL LOW pulsewidth	$t_{WCLL}$	—	330	—	ns
Data setup time	$t_{DS}$	—	100	—	ns
Data hold time	$t_{DH}$	—	10	—	ns
Allowable FR delay time	$t_{DFFR}$	—	-300	300	ns

$V_{SS}=-5.0V \pm 0.5V$ ,  $T_a=-40$  to  $85^{\circ}C$

Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	$t_r$	—	—	50	ns
Input signal fall time	$t_f$	—	—	50	ns
YSCL period	$t_{CCL}$	—	1000	—	ns
YSCL HIGH pulsewidth	$t_{WCLH}$	—	160	—	ns
YSCL LOW pulsewidth	$t_{WCLL}$	—	330	—	ns
Data setup time	$t_{DS}$	—	200	—	ns
Data hold time	$t_{DH}$	—	10	—	ns
Allowable FR delay time	$t_{DFFR}$	—	-500	500	ns

## Output timing characteristics



$V_{SS}=-5.0 \pm 10\%$ ,  $T_a=-40$  to  $+85^\circ\text{C}$

Parament	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	$t_{pdDOCL}$	$CL=15\text{pF}$	—	350	ns
(YSCL - fall to On output) delay time	$t_{pdCCL}$	$V_5=-12.0$ to $-28.0\text{V}$	—	1.0	$\mu\text{s}$
( $\overline{\text{DSPOFF}}$ to On output) delay time	$t_{pdCDOFF}$				
(FR to On Output) delay time	$t_{pdCFR}$	$CL=100\text{pF}$	—	1.0	$\mu\text{s}$

$V_{SS}=-4.5$ – $2.7\text{V}$ ,  $T_a=-40$  to  $+85^\circ\text{C}$

Parament	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	$t_{pdDOCL}$	$CL=15\text{pF}$	—	400	ns
(YSCL - fall to On output) delay time	$t_{pdCCL}$	$V_5=-12.0$ to $-28.0\text{V}$	—	2.0	$\mu\text{s}$
( $\overline{\text{DSPOFF}}$ to On output) delay time	$t_{pdCDOFF}$				
(FR to On Output) delay time	$t_{pdCFR}$	$CL=100\text{pF}$	—	2.0	$\mu\text{s}$

## 10. LCD DRIVE POWER

### Each voltage level forming method

To obtain each voltage level for LCD driving, it is optimum to divide the resistance of potential between VDDH and GND to drive the LCD using the voltage follower with an operational amplifier.

In taking into consideration of such a case using the operational amplifier, the maximum potential level V0 for LCD driving has been made a separate pin from VDD.

When no operational amplifier is used in V0, set  $V_0 = V_{DD}$ .

When a resistive divider is used, set it to a resistance value as low as possible in the system power capacity.

When a series resistance exists in the power supply line of VDD, a voltage drop of VDD occurs at the LSI power supply pin, the relationship with the LCD's intermediate potential ( $V_{DD} \geq V_0 \geq V_1 \geq V_4 \geq V_5$ ) cannot be met, this causing the LSI to be broken down in some cases. When a protection resistor is inserted, it is necessary to stabilize the voltage by capacitance.

### Note in power ON/OFF

Since this LSI is high in the voltage of LCD driving system, when a high voltage is applied to the LCD driving system with the logic system power supply kept floating or above  $V_{SS} = -2.5\text{ V}$ , an overcurrent flows and LSI breaks down in some cases.

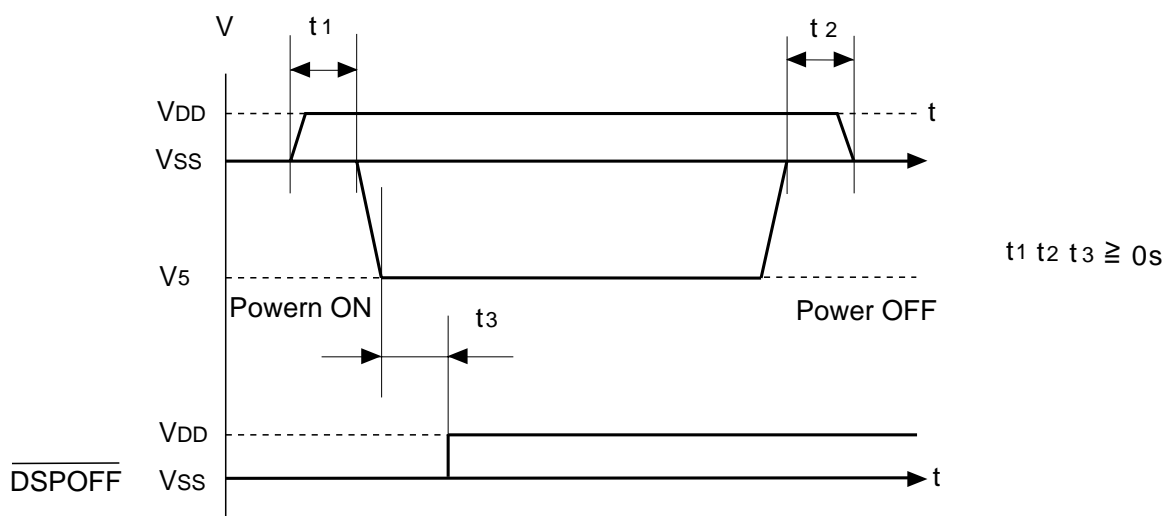
To avoid this, it is recommended to suppress the potential of LCD drive output to V0 level using the display off function (DSPOFF) until the LCD driving system voltage is stabilized.

### Be sure to follow the power ON/OFF sequence as shown below:

At power ON ... Logic system ON → LCD driving system ON or simultaneous ON of the both  
At power OFF ... LCD driving system OFF → Logic system OFF or simultaneous OFF of the both

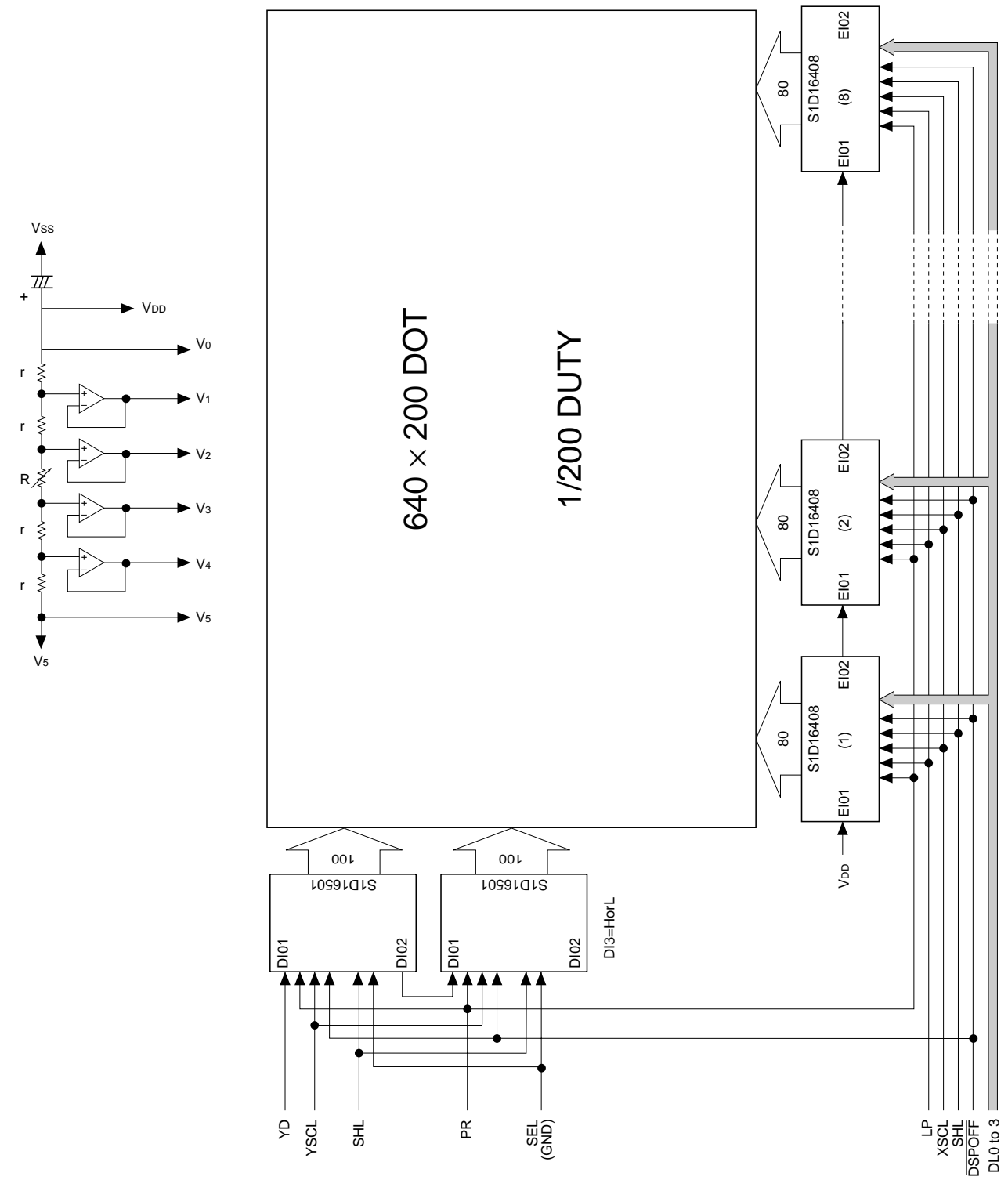
For a countermeasure to such overcurrent, it is effective to put a high-speed melting fuse or protection resistor in series with the LCD power unit.

It is then required to select the optimum value in the protection resistance according to the capacitance of LC cell.



# 11. TYPICAL CIRCUIT DIAGRAM

## Configuration Drawing of Large Screen LCD



**S1D16700**

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11. CONNECT EXAMPLE .....	4-13

## 1. DESCRIPTION

The S1D16700 is a 100 output low-power resistance common (row) driver which is suitable for driving a very high capacity dotmatrix LCD panels upto a duty ratio of 1/300. It is intended to be used in conjunction with the S1D16400 or S1D16006 as a pair.

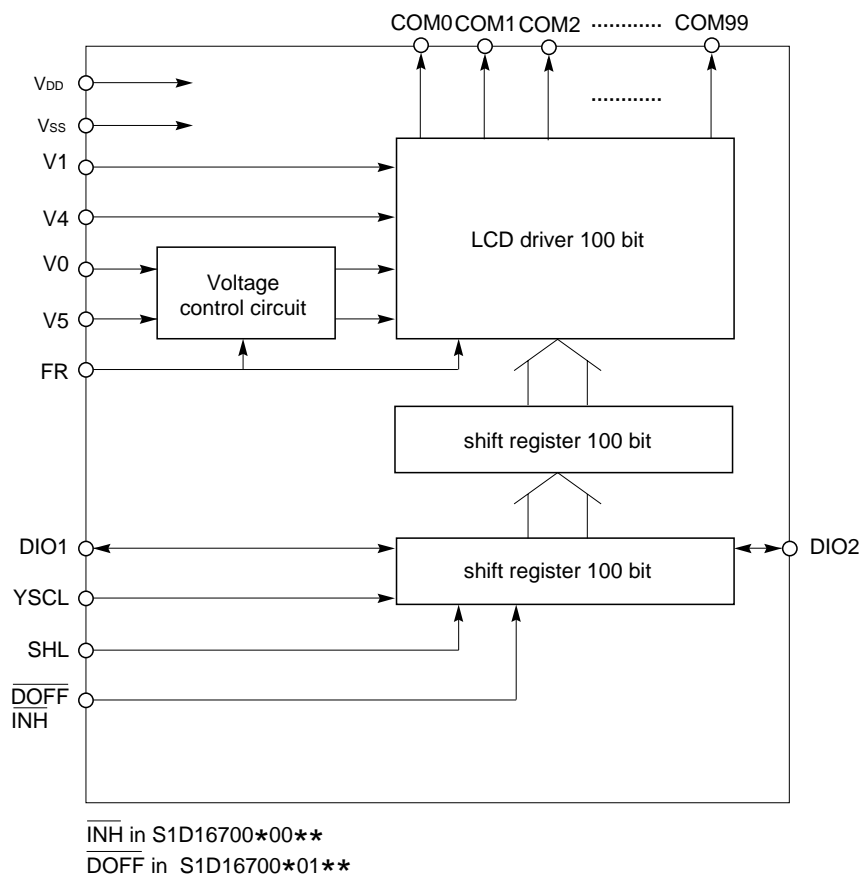
Since the S1D16700 is so designed to drive LCDs over a wide range of voltages, and also the maximum potential  $V_0$  of its LCD drive bias voltages is isolated from  $V_{DD}$  to allow the LCD driving bias voltages to be externally generated optionally with a high accuracy, it can cope with a wide range of LCD panels.

Owing to its pad layout which can minimize its PC boards mounting space in addition to its selectable bidirectional driver output sequence and as many as 100 LCD output segments of high pressure resistance and low output impedance, it is possible to obtain the highest driver working efficiency for the 1/200 duty panel. And the S1D16700\*01\*\* can display 65 x 132 panel when used as a common driver of RAM built-in driver, S1D15301.

## 2. FEATURES

- Number of LCD drive output segments: 100
- Common output ON resistance: 700  $\Omega$  (Typ.)
- Display duty ratio: 1/64 to 1/300 (Reference)
- Display capacity: Possible to display 640  $\times$  480 dots when used in combination with S1D 16400D or S1D16006D.
- Selectable pin output shift direction
- No-bias display OFF function (S1D16700\*01\*\*)
- Instantaneous display blanking enabled by inhibit function (S1D16700\*00\*\*)
- Adjustable offset bias of LCD power to  $V_{DD}$  level
- Wide range of LCD drive voltages: -7 V to -28 V (Absolute maximum rated voltage: -30 V)
- Logic system power supply: -2.7 V to -5.5 V
- Shipping pattern
  - S1D16700D00A\* (Al pad chip)
  - S1D16700D01A\* (Al pad chip)
  - S1D16700D00B\* (Au bump chip)
  - S1D16700D01B\* (Au bump chip)
  - S1D16700T00A\* (TCP)
  - S1D16700T01A\* (TCP)
- No radial rays countermeasure taken in designing

### 3. BLOCK DIAGRAM





## 4. PIN DESCRIPTION

Pin name	I/O	Function	Number of pins															
COM0 to COM099	O	LCD drive common (row) output The output changes at the YS CL falling edge.	100															
DIO1, DIO2	I/O	100-bit shift register serial data input/output To be set to input or output according to the SHL input The output changes at the YSCL falling edge.	2															
YSCL	I	Serial data shift clock input The scanning data is shifted at the falling edge.	1															
SHL	I	Shift direction selection and DIO pin I/O control input <table border="1"><thead><tr><th>SHL</th><th colspan="2">COM output shift direction</th><th>DIO1</th><th>DIO2</th></tr></thead><tbody><tr><td>LOW</td><td>0</td><td>→ 99</td><td>Input</td><td>Output</td></tr><tr><td>HIGH</td><td>99</td><td>→ 0</td><td>Ourput</td><td>Input</td></tr></tbody></table>	SHL	COM output shift direction		DIO1	DIO2	LOW	0	→ 99	Input	Output	HIGH	99	→ 0	Ourput	Input	1
SHL	COM output shift direction		DIO1	DIO2														
LOW	0	→ 99	Input	Output														
HIGH	99	→ 0	Ourput	Input														
$\overline{\text{DOFF}}$	I	LCD display blanking control input When LOW is input, the content of shift register is cleared and all common outputs become the $V_0$ level instantaneously (S1D16700D01B★).	1															
$(\overline{\text{INH}})$	I	LCD drive display blanking control input When LOW is input, the content of shift register is cleared and all common outputs become the non-select level instantaneously. Common output = $V_4$ (when FR = LOW) Common output = $V_1$ (when FR = HIGH) (S1D16700D00B★)	(1)															
FR	I	LCD drive output AC converted signal input	1															
$V_{\text{DD}}$ , $V_{\text{SS}}$	Power supply	Logic power supply $V_{\text{DD}}$ : 0 V (GND) $V_{\text{SS}}$ : -5.0 V	2															
$V_0$ , $V_1$ , $V_4$ , $V_5$	Power supply	LCD drive power supply $V_5$ : -7 V to -28 V $V_{\text{DD}} \geq V_0 \geq V_1 > V_4 \geq V_5$	4															

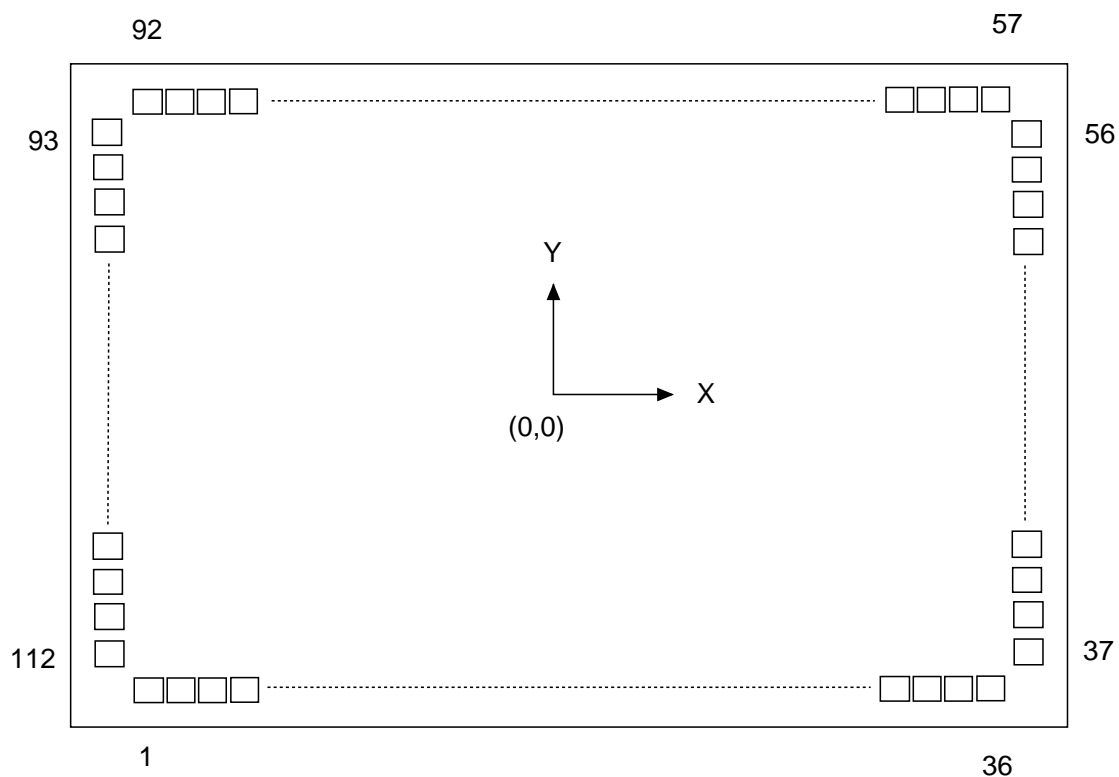
INH for S1D16700★00★★

Total: 112

 $\overline{\text{DOFF}}$  for S1D16700★01★★

## 5. PAD

### • Pad layout



Chip size ..... 5.49mm × 3.03mm

Chip thickness ..... 525μm (Au-bump die from)  
400μm (Al-Pad die from)

#### 1) Au bump specification reference values

Bump specific : High Quality Au bump

Bump size : 90μm × 90μm

Bump height : 17μm ~ 28μm

#### 2) AL Pad specification reference values

Pad Opening : 100μm × 100μm

## ● Pad center coordinates

PAD		Actual dimensions	
NO.	NAME	X	Y
1	COM5	-2187	-1357
2	6	-2058	
3	7	-1929	
4	8	-1799	
5	9	-1670	
6	10	-1541	
7	11	-1412	
8	12	-1283	
9	13	-1153	
10	14	-1024	
11	15	-895	
12	16	-766	
13	17	-637	
14	18	-507	
15	19	-378	
16	20	-249	
17	21	-120	
18	22	10	
19	23	139	
20	24	268	
21	25	397	
22	26	526	
23	27	656	
24	28	785	
25	29	914	
26	30	1043	
27	31	1172	
28	32	1302	
29	33	1431	
30	34	1560	
31	35	1689	
32	36	1818	
33	37	1948	
34	38	2077	
35	39	2206	
36	40	2335	-1357
37	41	2584	-1231
38	42	2584	-1094
39	43	2584	-969
40	44	2584	-840

PAD		Actual dimensions	
NO.	NAME	X	Y
41	COM45	2584	-711
42	46		-581
43	47		-452
44	48		-323
45	49		-194
46	50		-65
47	51		65
48	52		194
49	53		323
50	54		452
51	55		581
52	56		711
53	57		840
54	58		969
55	59		1098
56	60	2584	1231
57	61	2298	1357
58	62	2168	
59	63	2039	
60	64	1910	
61	65	1781	
62	66	1652	
63	67	1522	
64	68	1393	
65	69	1264	
66	70	1135	
67	71	1006	
68	72	876	
69	73	747	
70	74	618	
71	75	489	
72	76	360	
73	77	230	
74	78	101	
75	79	-28	
76	80	-157	
77	81	-286	
78	82	-416	
79	83	-545	
80	84	-674	1357

PAD		Actual dimensions	
NO.	NAME	X	Y
81	COM85	-803	1357
82	86	-932	
83	87	-1062	
84	88	-1191	
85	89	-1320	
89	90	-1449	
87	91	-1578	
88	92	-1708	
89	93	-1837	
90	94	-1966	
91	95	-2095	
92	96	-2224	1357
93	97	-2473	1334
94	98		1201
95	99		1071
96	DIO2		941
97	$\overline{\text{DOFF}}$		715
(97)	(INH)		
98	FR		585
99	YSCL		455
100	SHL		325
101	V <sub>DD</sub>		185
102	V <sub>SS</sub>		46
103	V <sub>0</sub>		-112
104	V <sub>1</sub>		-252
105	V <sub>4</sub>		-391
106	V <sub>5</sub>		-531
107	DIO1		-671
108	COM0		-810
109	1		-941
110	2		-1071
111	3		-1201
112	4	-2473	-1334

PAD No. 97:  $\overline{\text{INH}}$  for S1D16700\*00\*\*  
 $\overline{\text{DOFF}}$  for S1D16700\*01\*\*

## 6. FUNCTIONAL DESCRIPTION

### Shift register

This is a bidirectional shift register to transfer common data.

### Level shifter

This is a level interface circuit used to convert the signal voltage level from the logic system level to LCD drive level.

### LCD driver circuit

This driver outputs the LCD drive voltage.

The relationship among the display blanking signal DOFF, contents of shift register, AC converted signal FR and common output voltage is as shown in the table below:

(S1D16700\*01\*\*)

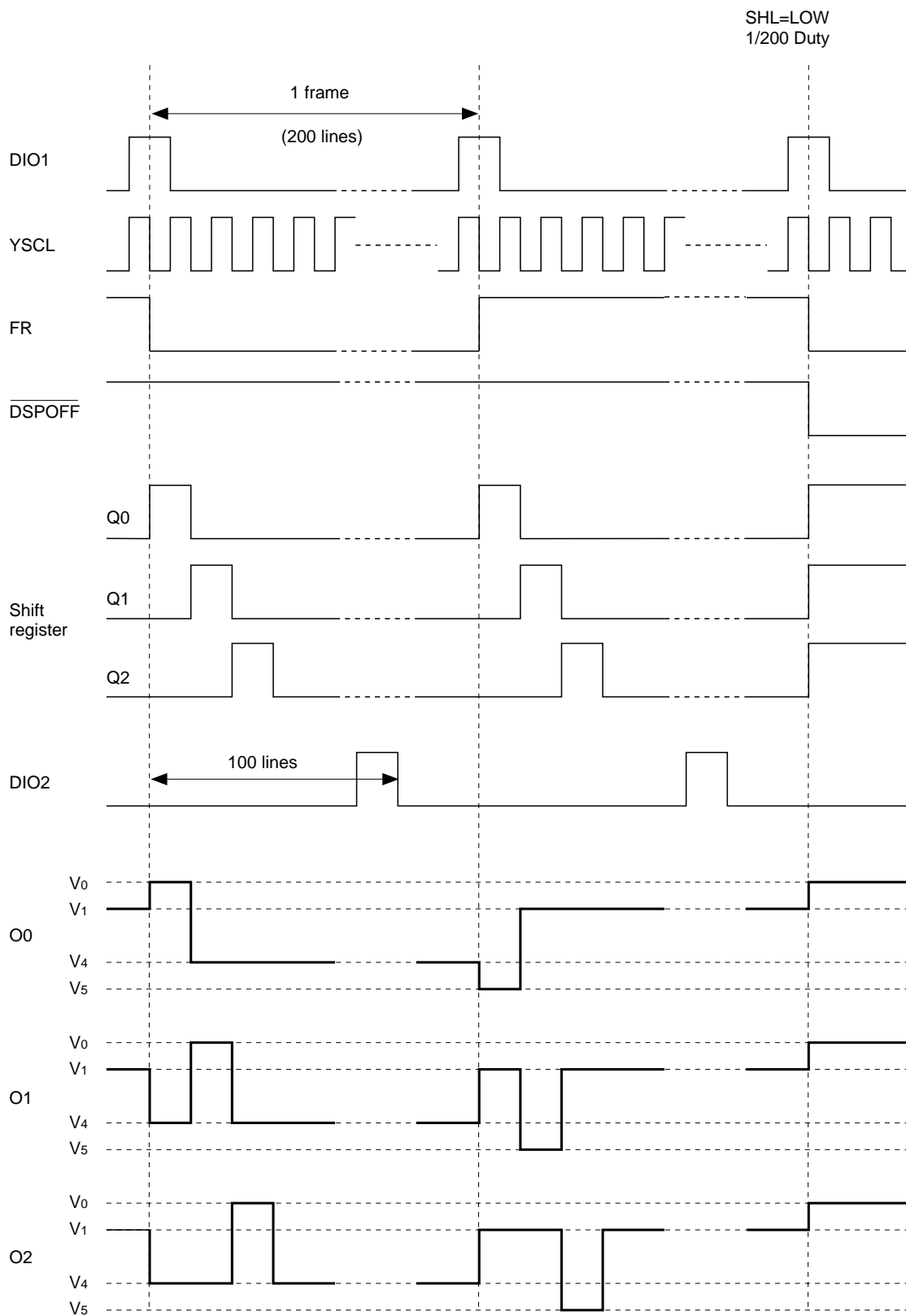
DOFF	Contents of shift register	FR	COM output voltage	
HIGH	HIGH	HIGH	V <sub>5</sub>	(Select level)
		LOW	V <sub>0</sub>	
	LOW	HIGH	V <sub>1</sub>	(Non-select level)
		LOW	V <sub>4</sub>	
LOW	Fixed to LOW	–	V <sub>0</sub>	–

The relationship among the display blanking signal INH, contents of the shift register, AC converted signal FR and COM output voltage is as shown in the table below:

(S1D16700\*00\*\*)

INH	Contents of shift register	FR	COM output voltage	
HIGH	HIGH	HIGH	V <sub>5</sub>	(Select level)
		LOW	V <sub>0</sub>	
	LOW	HIGH	V <sub>1</sub>	(Non-select level)
		LOW	V <sub>4</sub>	
LOW	Fixed to LOW	HIGH	V <sub>1</sub>	(Non-select level)
		LOW	V <sub>4</sub>	

## 7. TIMING CHART (S1D16700D01B\*)



The V1 or V4 non-select level is output corresponding to the FR in S1D16700D00B\* or  $\overline{\text{INH}}=\text{LOW}$ , respectively.

## 8. ABSOLUTE MAXIMUM RATINGS

V<sub>DD</sub>=0V

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V <sub>SS</sub>	−7.0 to +0.3	V
Supply voltage (2)	V <sub>5</sub>	−30.0 to +0.3	V
Supply voltage (3)	V <sub>0</sub> , V <sub>1</sub> , V <sub>4</sub>	V <sub>5</sub> −0.3 to +0.3	V
Input voltage	V <sub>I</sub>	V <sub>SS</sub> −0.3 to +0.3	V
Output voltage	V <sub>O</sub>	V <sub>SS</sub> −0.3 to +0.3	V
Output current (1)	I <sub>O</sub>	20	mA
Output current (2)	I <sub>OCOM</sub>	20	mA
Operating temperature	T <sub>opr</sub>	−40 to + 85	°C
Storing temperature 1	T <sub>stg</sub>	−65 to +150	°C

Notes:

1. The voltage of V<sub>0</sub>, V<sub>1</sub> and V<sub>4</sub> must always satisfy the condition of V<sub>DD</sub> ≥ V<sub>0</sub> ≥ V<sub>1</sub> ≥ V<sub>4</sub> ≥ V<sub>5</sub>.
2. Floating of the logic system power during while the LCD drive system power is applied, or exceeding V<sub>SS</sub> = −2.6 V or more can cause permanent damage to the LSI. Functional operation under these conditions is not implied.

Care should be taken to the power supply sequence especially in the system power ON or OFF.

## 9. ELECTRICAL CHARACTERISTICS

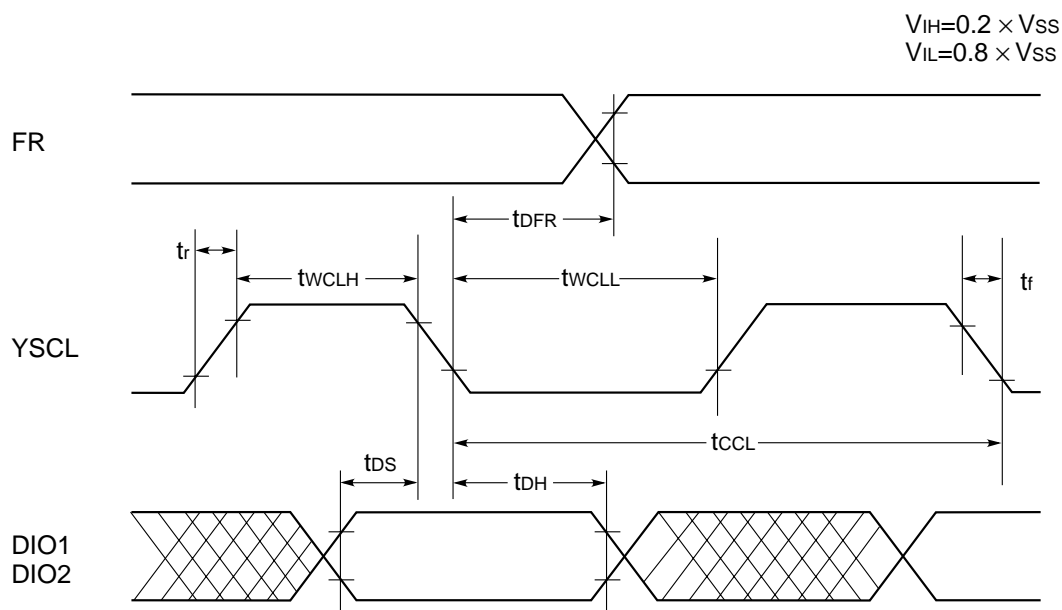
### DC characteristics

Unless otherwise specified,  $V_{DD} = V_0 = 0V$ ,  $V_{SS} = -5.0V \pm 10\%$ ,  $T_a = -40$  to  $85^\circ C$ .

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Supply voltage (1)	$V_{SS}$	—	-5.5	-5.0	-2.7	V	$V_{SS}$
Recommended operating voltage	$V_5$	—	-28.0	—	-7.0	V	$V_5$
Operation enable voltage	$V_5$	Functional operation	—	—	-7.0	V	$V_5$
Supply voltage (2)	$V_0$	Recommended value	-2.5	—	0	V	$V_0$
Supply voltage (3)	$V_1$	Recommended value	$2/9 \cdot V_5$	—	$V_{DD}$	V	$V_1$
Supply voltage (4)	$V_4$	Recommended value	$V_5$	—	$7/9 \cdot V_5$	V	$V_4$
HIGH input voltage (1)	$V_{IH}$	$V_{SS} = -2.7V$ to $-5.5V$	$0.2V_{SS}$	—	0	V	DIO1, DIO2, YSCL, SHL, FR
LOW input voltage (1)	$V_{IL}$		$V_{SS}$	—	$0.8V_{SS}$	V	
HIGH input voltage (2)	$V_{IHT}$	$V_{SS} = -2.7V$ to $-5.5V$	$0.2V_{SS}$	—	0	V	$\overline{DOFF}$ , $\overline{INH}$
LOW input voltage (2)	$V_{ILT}$		$V_{SS}$	—	$0.85V_{SS}$	V	
HIGH output voltage	$V_{OH}$	$I_{OH} = -0.3mA$ $I_{OH} = -0.2mA$ ( $V_{SS} = -2.7$ to $-4.5V$ )	-0.4	—	0	V	DIO1, DIO2
LOW output voltage	$V_{OL}$	$I_{OL} = +0.3mA$ $I_{OL} = +0.2mA$ ( $V_{SS} = -2.7$ to $-4.5V$ )	$V_{SS}$	—	$V_{SS} + 0.4$	V	
Input leakage current	$I_{LI}$	$V_{SS} \leq V_{IN} \leq 0V$	—	—	2.0	$\mu A$	YSCL, SHL, $\overline{DOFF}$ , $\overline{INH}$ , FR
Input/output leakage current	$I_{L/O}$	$V_{SS} \leq V_{IN} \leq 0V$	—	—	5.0	$\mu A$	DIO1, DIO2
Static current	$I_{DDS}$	$V_5 = -7.0$ to $-28.0V$ $V_{IH} = V_{DD}$ , $V_{IL} = V_{SS}$	—	—	25	$\mu A$	$V_{DD}$
Output resistance	$R_{COM}$	$\Delta V_{ON} = 0.5V$ $V_5 = -20.0V$ When the $V_1$ , $V_4$ , $V_0$ or $V_5$ level is output	—	0.70	1.40	$k\Omega$	COM0~COM99
Average operating current consumption (1)	$I_{SS1}$	$V_{SS} = -5.0V$ , $V_{IH} = V_{DD}$ , $V_{IL} = V_{SS}$ , $f_{YSCL} = 12KHz$ , Frame frequency = 60Hz Input data; "H" at no load every 1/200 duty Other conditions are the same as $V_{SS} = -3.0V$	—	7	15	$\mu A$	$V_{SS}$
			—	5	10		
Average operating current consumption (2)	$I_{SS2}$	$V_{SS} = -5.0V$ , $V_1 = -2.0V$ , $V_4 = -18.0V$ , $V_5 = -20.0V$ Other conditions are the same as in the item of $I_{SS1}$ .	—	7	15	$\mu A$	$V_5$
Input pin capacitance	$C_i$	$T_a = 25^\circ C$	—	—	8	pF	YSCL, SHL, $\overline{DOFF}$ , $\overline{INH}$ , FR
Input/output pin capacitance	$C_{I/O}$		—	—	15	pF	DIO1, DIO2

## AC Characteristics

## Input timing characteristics



Unless otherwise specified  $V_{SS}=-5.0V \pm 10\%$ ,  $T_a=-40$  to  $85^\circ\text{C}$

Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	$t_r$	—	—	50	ns
Input signal fall time	$t_f$	—	—	50	ns
YSCL period	$t_{cCL}$	—	500	—	ns
YSCL HIGH pulsewidth	$t_{wCLH}$	—	70	—	ns
YSCL LOW pulsewidth	$t_{wCLL}$	—	330	—	ns
Data setup time	$t_{DS}$	—	100	—	ns
Data hold time	$t_{DH}$	—	10	—	ns
Allowable FR delay time	$t_{DFR}$	—	-500	500	ns

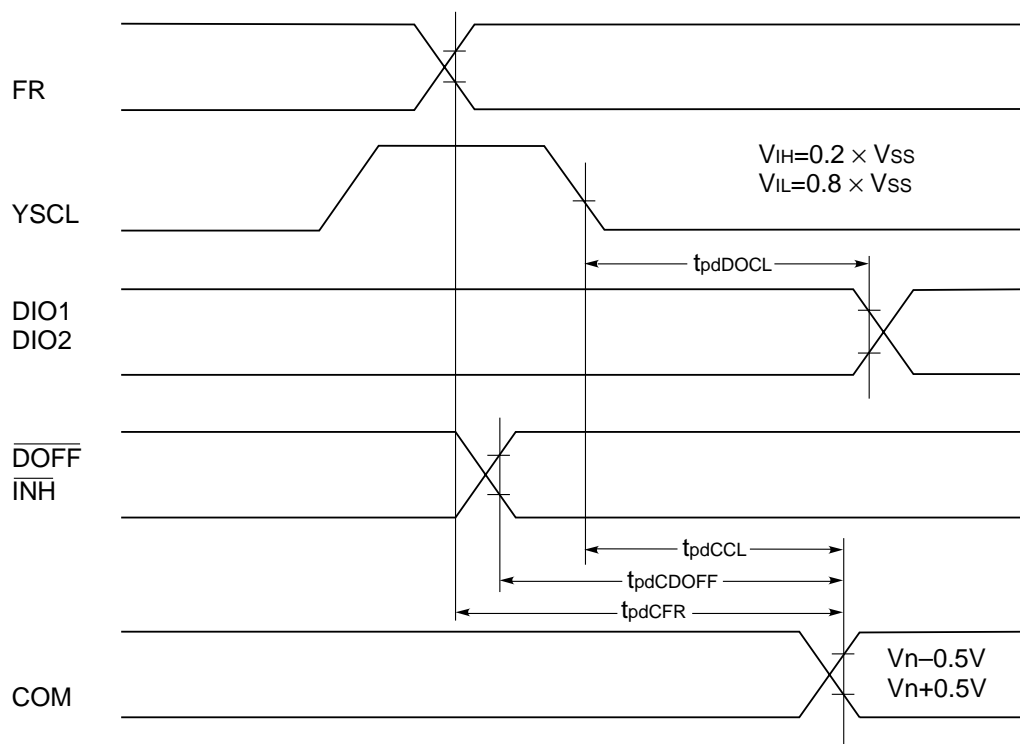
Unless otherwise specified  $V_{SS}=-2.7V$  to  $-4.5V$ ,  $T_a=-40$  to  $85^\circ\text{C}$

Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	$t_r$	—	—	50	ns
Input signal fall time	$t_f$	—	—	50	ns
YSCL period	$t_{cCL}$	—	1000	—	ns
YSCL HIGH pulsewidth	$t_{wCLH}$	—	160	—	ns
YSCL LOW pulsewidth	$t_{wCLL}$	—	330	—	ns
Data setup time	$t_{DS}$	—	200	—	ns
Data hold time	$t_{DH}$	—	10	—	ns
Allowable FR delay time	$t_{DFR}$	—	-500	500	ns

The standard applicable to  $t_{cCL}$ ,  $t_{wCLH}$ ,  $t_{wCLL}$  and  $t_{DS}$  when  $V_{SS} = -2.4V$  shall be 1.3 times of that applies when  $V_{SS} = -2.7V$  to  $-4.5V$ .



## Output timing characteristics



Unless otherwise specified  $V_{ss}=-5.0V \pm 10\%$ ,  $T_a=-40$  to  $85^\circ C$

Parament	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	$t_{pdDOCL}$	$CL=15pF$	30	300	ns
(YSCL - fall to COM output) delay time	$t_{pdCCL}$	$V_5=-7.0$ to $-28.0V$ $CL=100pF$	—	3.0	$\mu s$
(DOFF to COM output) delay time	$t_{pdCDOFF}$				
(INH to COM output) delay time	$t_{pdCINH}$				
(FR to COM output) delay time	$t_{pdCFR}$		—	3.0	$\mu s$

Unless otherwise specified  $V_{ss}=-2.7V$  to  $-4.5V$ ,  $T_a=-40$  to  $85^\circ C$

Parament	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	$t_{pdDOCL}$	$CL=15pF$	60	600	ns
(YSCL - fall to COM output) delay time	$t_{pdCCL}$	$V_5=-7.0$ to $-28.0V$ $CL=100pF$	—	3.0	$\mu s$
(DOFF to COM output) delay time	$t_{pdCDOFF}$				
(INH to COM output) delay time	$t_{pdCINH}$				
(FR to COM output) delay time	$t_{pdCFR}$		—	3.0	$\mu s$

The standard applicable at  $V_{ss} = -2.4V$  shall be the same as that employed when  $V_{ss} = -2.7V$  to  $-4.5V$ .

## 10. LCD DRIVE POWER

### Each voltage level forming method

To obtain each voltage level for LCD driving, it is the most simple to divide the resistance of potential as shown in the connection example. On the other hand, to obtain a high quality display, it is necessary to raise the accuracy and constancy of each voltage level and to set the divided resistance value as low as possible in the range of system power capacity.

Especially when a low-power LCD driving is required, set the divided resistance to a higher value and drive the LCD with a voltage follower by means of operational amplifier instead. In taking into consideration of a case where the operational amplifier is employed, the maximum potential level  $V_0$  for LCD driving has been isolated from the VDD pin.

When the potential of  $V_0$  lowers than that of VDD and the potential difference between the two becomes larger, however, the capacity of LCD drive output driver lowers. To avoid it, use the system with the potential difference of 0 V to 2.5 V between  $V_0$  and VDD.

When no operational amplifier is used, connect  $V_0$  and VDD pins.

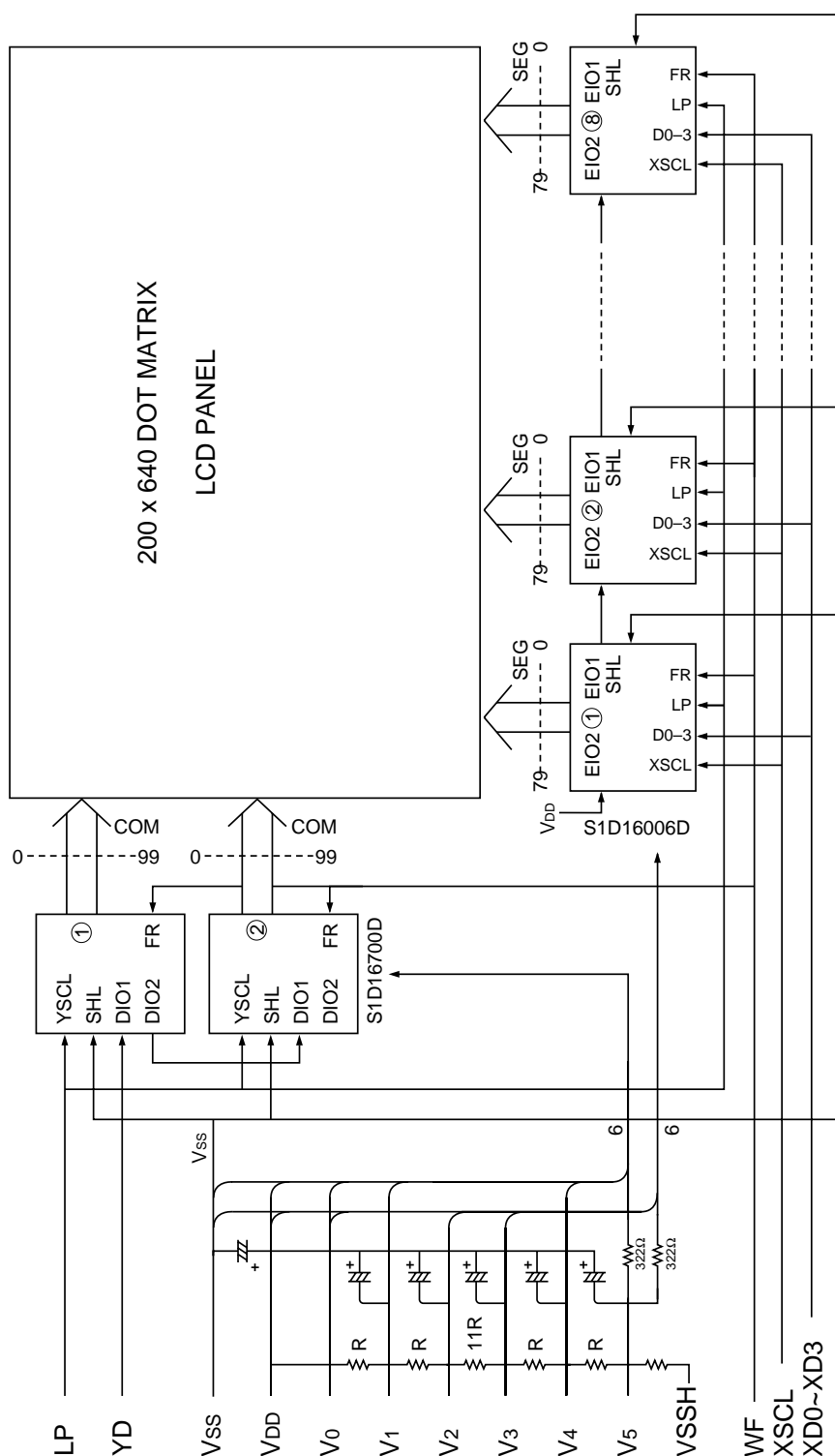
### Note in power ON/OFF

Since this LSI is high in the voltage of LCD driving system, when a high voltage is applied to the LCD driving system with the logic system power supply kept floating, an overcurrent flows and LSI breaks down in some cases.

### Be sure to follow the power ON/OFF sequence as shown below:

At power ON ... Logic system ON → LCD driving system ON or simultaneous ON of the both  
At power OFF ... LCD driving system OFF → Logic system OFF or simultaneous OFF of the both

## 11. CONNECT EXAMPLE



Note \*1 It must be provided as the protective resistor against overcurrent. Also, the bypass capacitor (0.01  $\mu$ F) for noise suppression must be provided near to Vss and V5 terminals on each LSI.

**S1D16702**

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## 1. DESCRIPTION

The S1D16702 is a 68 output low-power resistance common (row) driver which is suitable for driving a very high capacity dotmatrix LCD panels up to a duty ratio of 1/300. It is intended to be used in conjunction with the S1D16006 as a pair.

Since the S1D16006 is so designed to drive LCD's over a wide range of voltages, and also the maximum potential  $V_0$  of its LCD drive bias voltages is isolated from  $V_{DD}$  to allow the LCD driving bias voltages to be externally generated optionally with a high accuracy, it can cope with a wide range of LCD panels.

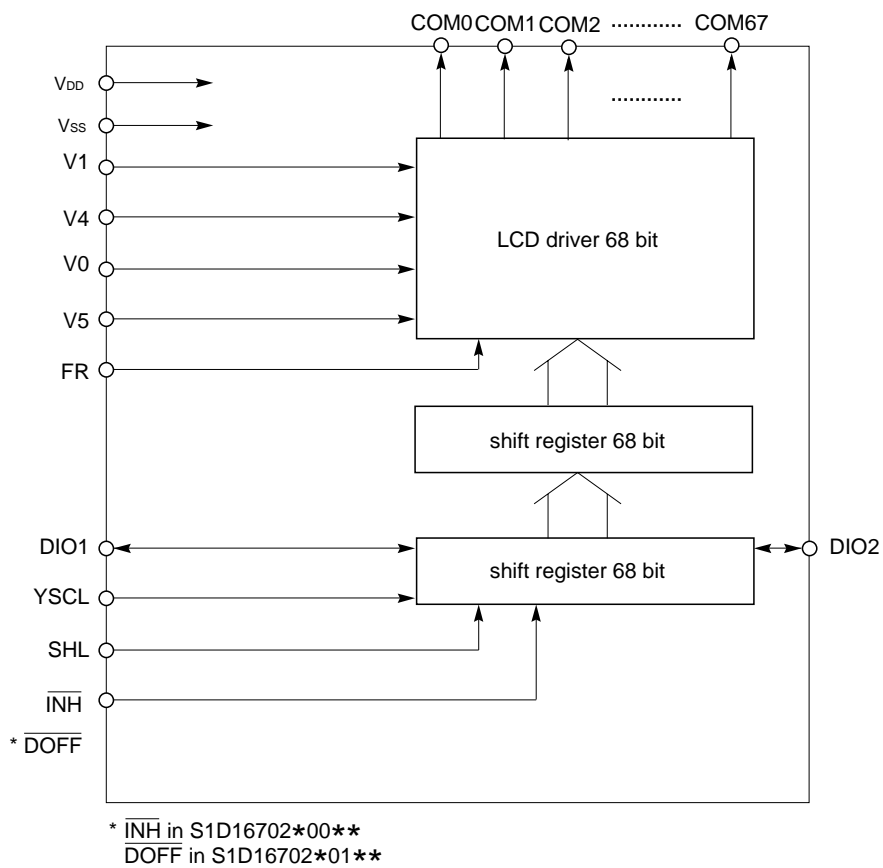
The S1D16702 is featured in its simple pad layout which is easy in mounting PC boards in addition to its selectable bidirectional driver output sequence. It also has 68 LCD output segments of high pressure resistance and low output impedance.

It can display the  $65 \times 132$  panel when used as the expansion driver of S1D15301 being built in RAM (S1D16702\*01\*\*).

## 2. FEATURES

- Number of LCD drive output segments: 68
- Common output ON resistance:  $700\ \Omega$  (Typ.)
- Display duty ratio: 1/64 to 1/300 (Reference)
- Display capacity: Possible to display  $640 \times 480$  dots when used in combination with S1D16006.
- Selectable pin output shift direction
- Instantaneous display blanking enabled by inhibit function (S1D16702\*00\*\*)
- Non-bias display off function (S1D16702\*01\*\*)
- Adjustable offset bias of LCD power to  $V_{DD}$  level
- Wide range of LCD drive voltages:  $-7\text{ V}$  to  $-28\text{ V}$  (Absolute maximum rated voltage:  $-30\text{ V}$ )
- Logic system power supply:  $-2.7\text{ V}$  to  $-5.5\text{ V}$
- Shipping pattern
  - S1D16702D00A\* (Al pad chip)
  - S1D16702D01A\* (Al pad chip)
  - S1D16702F00A\* (80-pin QFP5)
- No radial rays countermeasure taken in designing
- Non-bias display off function

### 3. BLOCK DIAGRAM



## 4. PIN DESCRIPTION

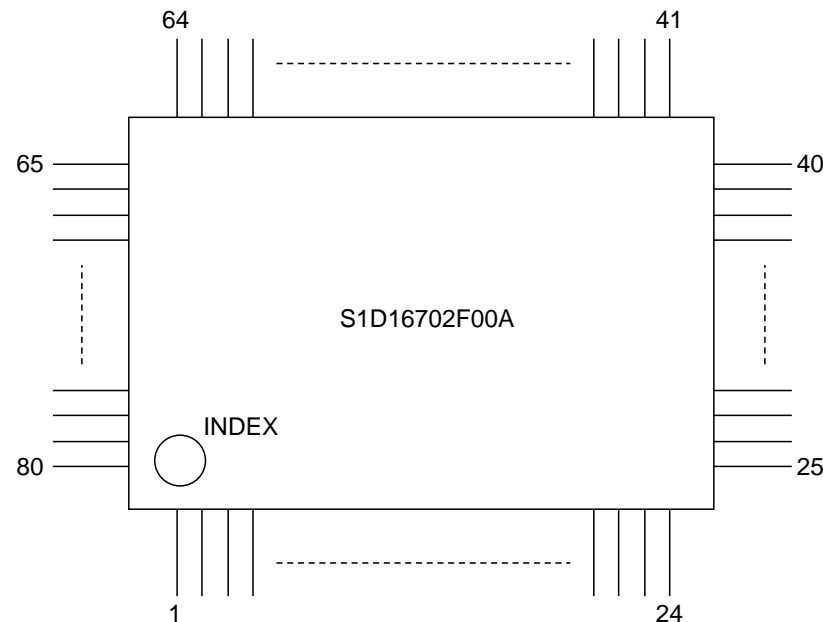
Pin name	I/O	Function	Number of pins																	
COM0 to COM67	O	LCD drive common (row) output The output changes at the YSCL falling edge.	68																	
DIO1, DIO2	I/O	100-bit shift register serial data input/output To be set to input or output according to the SHL input The output changes at the YSCL falling edge.	2																	
YSCL	I	Serial data shift clock input The scanning data is shifted at the falling edge.	1																	
SHL	I	Display data latch pulse input (Falling edge trigger) Shift direction selection and DIO pin I/O control input <table><tr><td>SHL</td><td colspan="2">COM output shift direction</td><td>DIO1</td><td>DIO2</td></tr><tr><td>LOW</td><td>0</td><td>→</td><td>67</td><td>Input</td><td>Output</td></tr><tr><td>HIGH</td><td>67</td><td>→</td><td>0</td><td>Ourput</td><td>Input</td></tr></table>	SHL	COM output shift direction		DIO1	DIO2	LOW	0	→	67	Input	Output	HIGH	67	→	0	Ourput	Input	1
SHL	COM output shift direction		DIO1	DIO2																
LOW	0	→	67	Input	Output															
HIGH	67	→	0	Ourput	Input															
$\overline{\text{DOFF}}$	I	LCD display blanking control input when LOW is input, the content of shift register is cleared and all common outputs become the non-select level instantaneously. (S1D16702*01**)	1																	
$\overline{\text{INH}}$	I	LCD display blanking control input When LOW is input, the content of shift register is cleared and all common outputs become the non-select level instantaneously. Common output = V <sub>4</sub> (when FR = LOW) Common output = V <sub>1</sub> (when FR = HIGH) (S1D16702*00**)	(1)																	
FR	I	LCD drive output AC converted signal input	1																	
V <sub>DD</sub> , V <sub>SS</sub>	Power supply	Logic power supply      V <sub>DD</sub> : 0 V (GND)    V <sub>SS</sub> : -5.0 V	2																	
V <sub>0</sub> , V <sub>1</sub> , V <sub>4</sub> , V <sub>5</sub>	Power supply	LCD drive power supply    V <sub>5</sub> : -7 V to -28 V V <sub>DD</sub> ≥ V <sub>0</sub> ≥ V <sub>1</sub> > V <sub>4</sub> ≥ V <sub>5</sub>	4																	

$\overline{\text{INH}}$  in S1D16702\*00\*\*  
 $\overline{\text{DOFF}}$  in S1D16702\*01\*\*



# 5. PIN LAYOUT

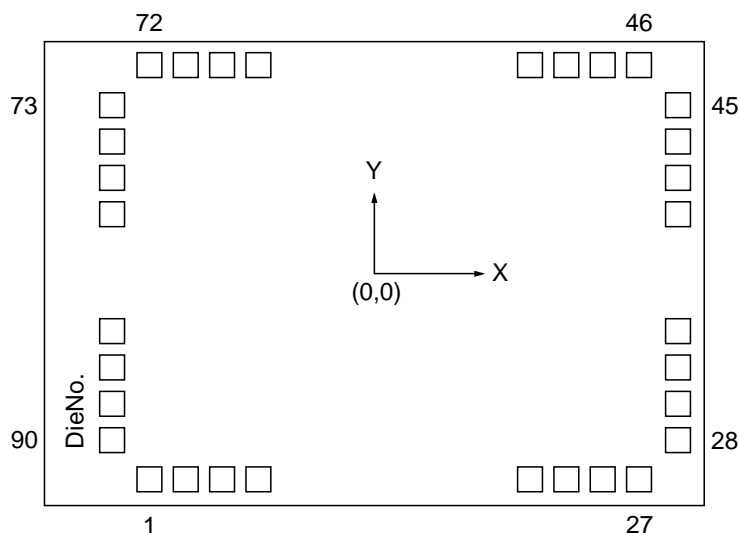
Package type: QFP-5 80pin



PIN No.	Pin Name	PIN No.	Pin Name	PIN No.	Pin Name	PIN No.	Pin Name
1	COM 3	21	COM 23	41	COM 43	61	COM 63
2	COM 4	22	COM 24	42	COM 44	62	COM 64
3	COM 5	23	COM 25	43	COM 45	63	COM 65
4	COM 6	24	COM 26	44	COM 46	64	COM 66
5	COM 7	25	COM 27	45	COM 47	65	COM 67
6	COM 8	26	COM 28	46	COM 48	66	DIO2
7	COM 9	27	COM 29	47	COM 49	67	INH
8	COM 10	28	COM 30	48	COM 50	68	FR
9	COM 11	29	COM 31	49	COM 51	69	YSCL
10	COM 12	30	COM 32	50	COM 52	70	SHL
11	COM 13	31	COM 33	51	COM 53	71	VDD
12	COM 14	32	COM 34	52	COM 54	72	VSS
13	COM 15	33	COM 35	53	COM 55	73	V0
14	COM 16	34	COM 36	54	COM 56	74	V1
15	COM 17	35	COM 37	55	COM 57	75	V4
16	COM 18	36	COM 38	56	COM 58	76	V5
17	COM 19	37	COM 39	57	COM 59	77	DIO1
18	COM 20	38	COM 40	58	COM 60	78	COM 0
19	COM 21	39	COM 41	59	COM 61	79	COM 1
20	COM 22	40	COM 42	60	COM 62	80	COM 2

## 6. PAD

### • Pad layout



Chip size:  $4.27 \times 3.03$  mm

Chip thickness: 400  $\mu\text{m}$  (for AL pad product) and 525  $\mu\text{m}$  (for BUMP product).

AL pad product: Pad opening is  $100 \times 100$   $\mu\text{m}$ .

BUMP product: Vertical Au bump.

Bump size is  $90 \times 90$   $\mu\text{m}$ .

Bump height is 17 to 25  $\mu\text{m}$ .

### • Pad center coordinates

PAD NO.	PIN NAME	X	Y	PAD NO.	PIN NAME	X	Y	PAD NO.	PIN NAME	X	Y
1	DM	-1579	-1357	31	COM 29	1976	-711	61	COM 56	-195	1357
2	COM 3	-1449		32	COM 30		-581	62	COM 57	-324	
3	COM 4	-1320		33	COM 31		-452	63	COM 58	-453	
4	COM 5	-1191		34	COM 32		-323	64	COM 59	-583	
5	COM 6	-1062		35	COM 33		-194	65	COM 60	-712	
6	COM 7	-933		36	COM 34		-65	66	COM 61	-841	
7	COM 8	-803		37	COM 35		65	67	COM 62	-970	
8	COM 9	-674		38	COM 36		194	68	COM 63	-1099	
9	COM 10	-545		39	COM 37		323	69	COM 64	-1229	
10	COM 11	-416		40	COM 38		452	70	COM 65	-1358	
11	COM 12	-287		41	COM 39		581	71	COM 66	-1487	
12	COM 13	-154		42	COM 40		711	72	DM	-1616	1357
13	COM 14	-28		43	COM 41		840	73	DM	-1865	1201
14	COM 15	101		44	COM 42		969	74	COM 67		1071
15	COM 16	230		45	DM	1976	1098	75	DIO2		941
16	COM 17	359		46	DM	1743	1357	76	*1 INH		715
17	COM 18	489		47	DM	1614		77	FR		585
18	COM 19	618		48	COM 43	1485		78	YSCL		455
19	COM 20	747		49	COM 44	1355		79	SHL		325
20	COM 21	876		50	COM 45	1226		80	V <sub>DD</sub>		195
21	COM 22	1005		51	COM 46	1097		81	V <sub>SS</sub>		55
22	COM 23	1135		52	COM 47	968		82	V <sub>0</sub>		-112
23	COM 24	1264		53	COM 48	839		83	V <sub>1</sub>		-252
24	COM 25	1393		54	COM 49	709		84	V <sub>4</sub>		-391
25	COM 26	1522		55	COM 50	580		85	V <sub>5</sub>		-531
26	DM	1651		56	COM 51	451		86	DIO1		-671
27	DM	1781	-1357	57	COM 52	322		87	COM 0		-810
28	DM	1976	-1098	58	COM 53	193		88	COM 1		-941
29	COM 27	1976	-969	59	COM 54	63		89	COM 2		-1071
30	COM 28	1976	-840	60	COM 55	-66	1357	90	DM	-1865	-1201

\*1 PAD No. 76: INH for S1D16702\*00\*\*  
DOFF for S1D16702\*01\*\*

## 7. FUNCTIONAL DESCRIPTION

### Shift register

This is a bidirectional shift register to transfer common data.

### Level shifter

This is a level interface circuit used to convert the signal voltage level from the logic system level to LCD drive level.

### LCD driver circuit

This driver outputs the LCD drive voltage.

The relationship among the display blanking signal  $\overline{\text{INH}}$ , contents of shift register, AC converted signal FR and common output voltage is as shown in the table below:

(S1D16702\*00\*\*)

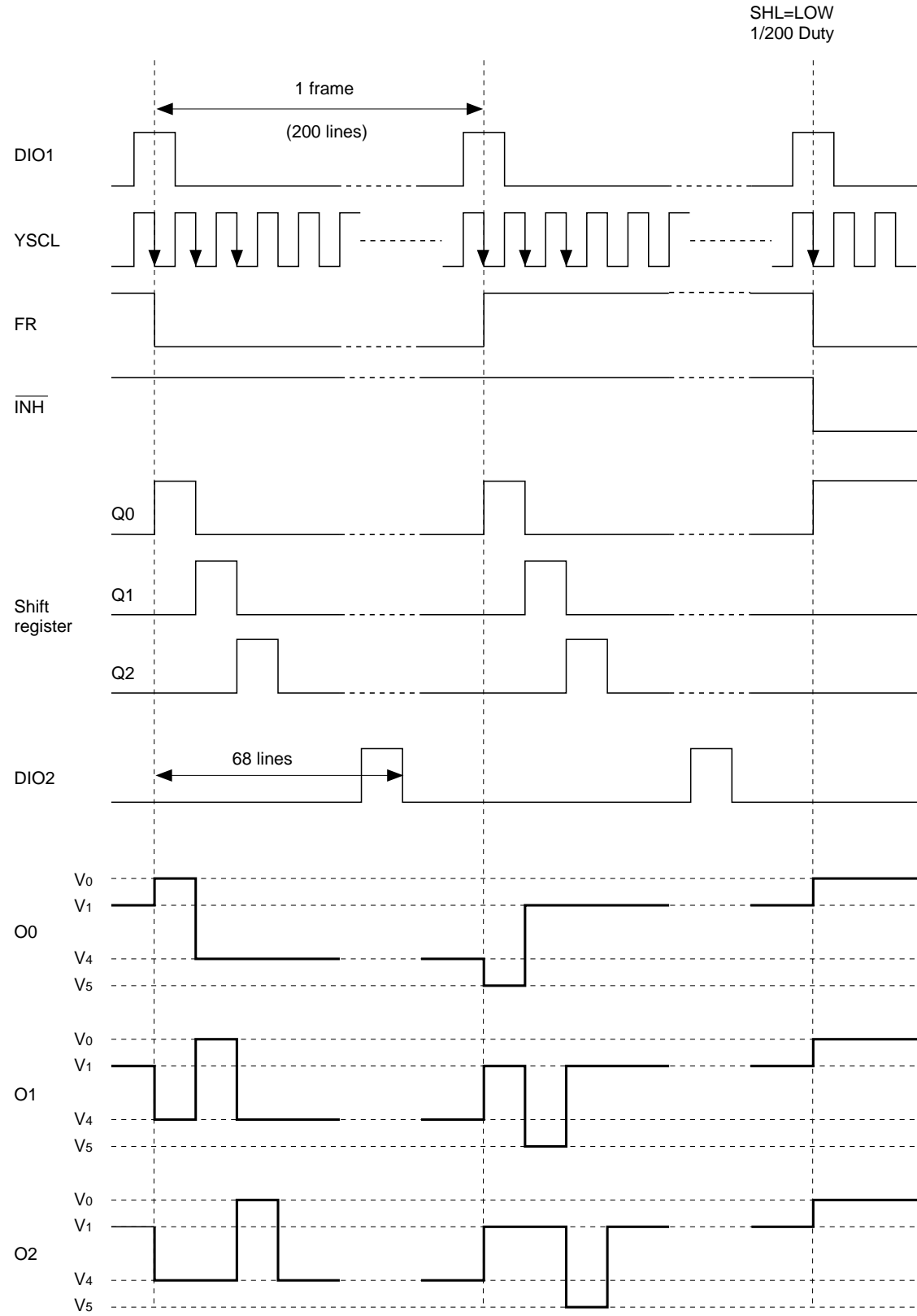
INH	Contents of shift register	FR	COM output voltage	
HIGH	HIGH	HIGH	V <sub>5</sub>	(Select level)
		LOW	V <sub>0</sub>	
	LOW	HIGH	V <sub>1</sub>	(Non-select level)
		LOW	V <sub>4</sub>	
LOW	Fixed to LOW	HIGH	V <sub>1</sub>	(Non-select level)
		LOW	V <sub>4</sub>	

The relationship among the display blanking signal  $\overline{\text{INH}}$ , contents of shift register, AC converted signal FR and common output voltage is as shown in the table below.

(S1D16702\*01\*\*)

$\overline{\text{DOFF}}$	Contents of shift register	FR	COM output voltage	
HIGH	HIGH	HIGH	V <sub>5</sub>	(Select level)
		LOW	V <sub>0</sub>	
	LOW	HIGH	V <sub>1</sub>	(Non-select level)
		LOW	V <sub>4</sub>	
LOW	Fixed to LOW	—	V <sub>0</sub>	(Non-select level)

# 8. TIMING CHART



## 9. ABSOLUTE MAXIMUM RATINGS

V<sub>DD</sub>=0V

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V <sub>SS</sub>	−7.0 to +0.3	V
Supply voltage (2)	V <sub>5</sub>	−30.0 to +0.3	V
Supply voltage (3)	V <sub>0</sub> , V <sub>1</sub> , V <sub>4</sub>	V <sub>5</sub> −0.3 to +0.3	V
Input voltage	V <sub>I</sub>	V <sub>SS</sub> −0.3 to +0.3	V
Output voltage	V <sub>O</sub>	V <sub>SS</sub> −0.3 to +0.3	V
Output current (1)	I <sub>O</sub>	20	mA
Output current (2)	I <sub>OCOM</sub>	20	mA
Operating temperature	T <sub>opr</sub>	−40 to + 85	°C
Storing temperature	T <sub>stg</sub>	−65 to +150	°C
Soldering temperature and time	T <sub>sol</sub>	260°C · 10sec	—

### Notes:

1. The voltage of V<sub>0</sub>, V<sub>1</sub> and V<sub>4</sub> must always satisfy the condition of V<sub>DD</sub> ≥ V<sub>0</sub> ≥ V<sub>1</sub> ≥ V<sub>4</sub> ≥ V<sub>5</sub>.
2. Floating of the logic system power during while the LCD drive system power is applied, or exceeding V<sub>SS</sub> = −2.6 V or more can cause permanent damage to the LSI. Functional operation under these conditions is not implied.  
Care should be taken to the power supply sequence especially in the system power ON or OFF.
3. All the above voltage is based on V<sub>DD</sub> = 0 V.

## 10. ELECTRICAL CHARACTERISTICS

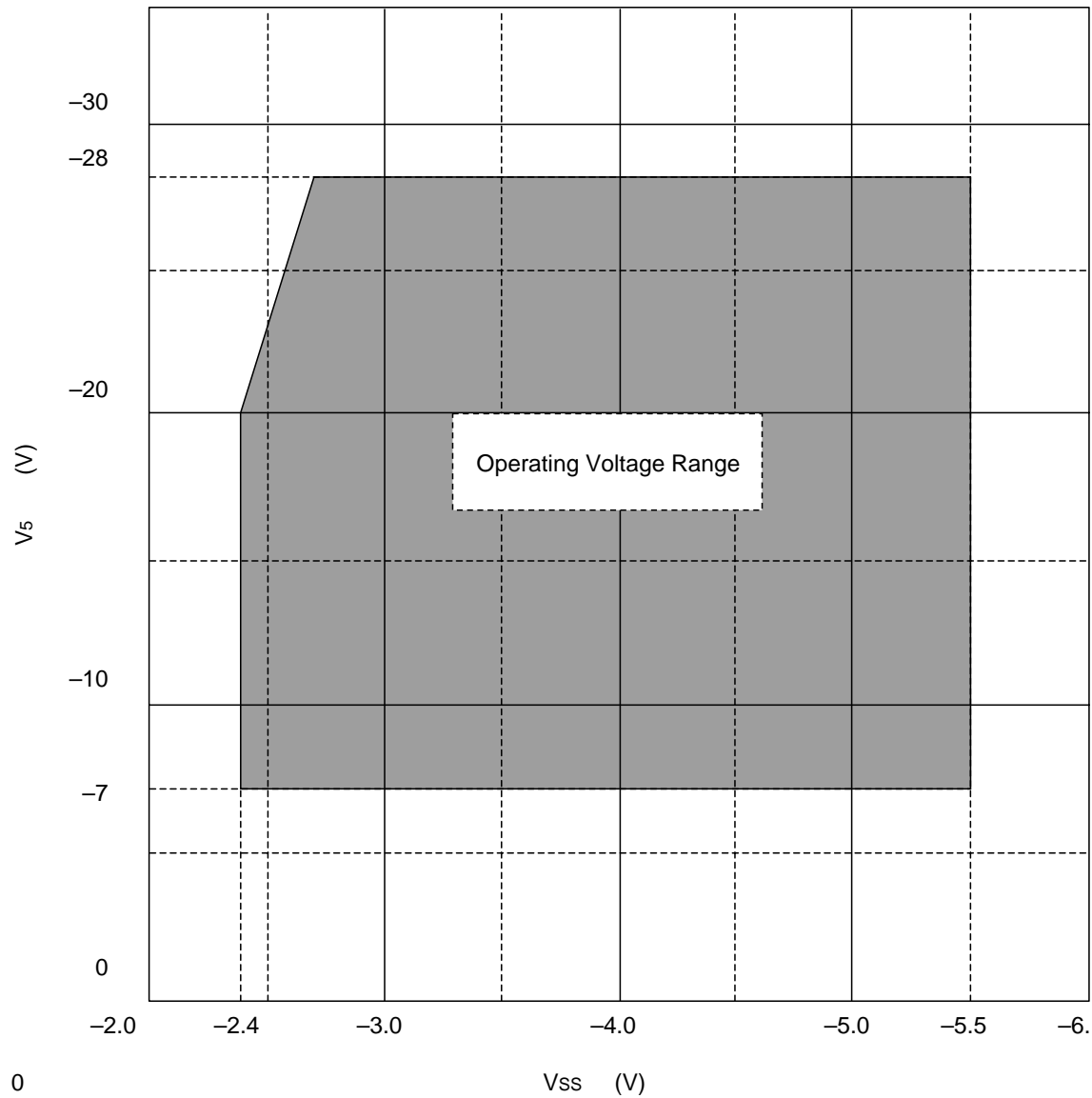
### DC characteristics

Unless otherwise specified,  $V_{DD} = V_0 = 0V$ ,  $V_{SS} = -5.0V \pm 10\%$ ,  $T_a = -40$  to  $85^\circ C$ .

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Supply voltage (1)	$V_{SS}$	—	-5.5	-5.0	-2.7	V	$V_{SS}$
Recommended operating voltage	$V_5$	—	-28.0	—	-7.0	V	$V_5$
Operation enable voltage	$V_5$	Functional operation	—	—	-7.0	V	$V_5$
Supply voltage (2)	$V_0$	Recommended value	-2.5	—	0	V	$V_0$
Supply voltage (3)	$V_1$	Recommended value	$2/9 \cdot V_5$	—	$V_{DD}$	V	$V_1$
Supply voltage (4)	$V_4$	Recommended value	$V_5$	—	$7/9 \cdot V_5$	V	$V_4$
HIGH input voltage (1)	$V_{IH}$	$V_{SS} = -2.7V$ to $-5.5V$	$0.2V_{SS}$	—	0	V	DIO1, DIO2, YSCL, SHL, FR
LOW input voltage (1)	$V_{IL}$		$V_{SS}$	—	$0.8V_{SS}$	V	
HIGH input voltage (2)	$V_{IHT}$	$V_{SS} = -2.7V$ to $-5.5V$	$0.2V_{SS}$	—	0	V	$\overline{INH}$
LOW input voltage (2)	$V_{ILT}$		$V_{SS}$	—	$0.85V_{SS}$	V	
HIGH output voltage	$V_{OH}$	$I_{OH} = -0.3mA$ $I_{OH} = -0.2mA$ ( $V_{SS} = -2.7$ to $-4.5V$ )	-0.4	—	0	V	DIO1, DIO2
LOW output voltage	$V_{OL}$	$I_{OL} = +0.3mA$ $I_{OL} = +0.2mA$ ( $V_{SS} = -2.7$ to $-4.5V$ )	$V_{SS}$	—	$V_{SS} + 0.4$	V	
Input leakage current	$I_{LI}$	$V_{SS} \leq V_{IN} \leq 0V$	—	—	2.0	$\mu A$	YSCL, SHL, $\overline{INH}$ , FR
Input/output leakage current	$I_{LI/O}$	$V_{SS} \leq V_{IN} \leq 0V$	—	—	5.0	$\mu A$	DIO1, DIO2
Static current	$I_{DDS}$	$V_5 = -7.0$ to $-28.0V$ $V_{IH} = V_{DD}$ , $V_{IL} = V_{SS}$	—	—	25	$\mu A$	$V_{DD}$
Output resistance	$R_{COM}$	$\Delta V_{ON} = 0.5V$ $V_5 = -20.0V$ When the $V_1$ , $V_4$ , $V_0$ or $V_5$ level is output	—	0.70	1.40	k $\Omega$	COM0 to COM99
Average operating current consumption (1)	$I_{SS1}$	$V_{SS} = -5.0V$ , $V_{IH} = V_{DD}$ , $V_{IL} = V_{SS}$ , $f_{YSCl} = 12KHz$ , Frame frequency = 60Hz Input data; HIGH at no load every 1/200 duty Other conditions are the same as $V_{SS} = -3.0V$	—	7	15	$\mu A$	$V_{SS}$
			—	5	10		
Average operating current consumption (2)	$I_{SS2}$	$V_{SS} = -5.0V$ , $V_1 = -2.0V$ , $V_4 = -18.0V$ , $V_5 = -20.0V$ Other conditions are the same as in the item of $I_{SS1}$ .	—	7	15	$\mu A$	$V_5$
Input pin capacitance	$C_i$	$T_a = 25^\circ C$	—	—	8	pF	YSCL, SHL, $\overline{INH}$ , FR
Input/output pin capacitance	$C_{I/O}$		—	—	15	pF	DIO1, DIO2

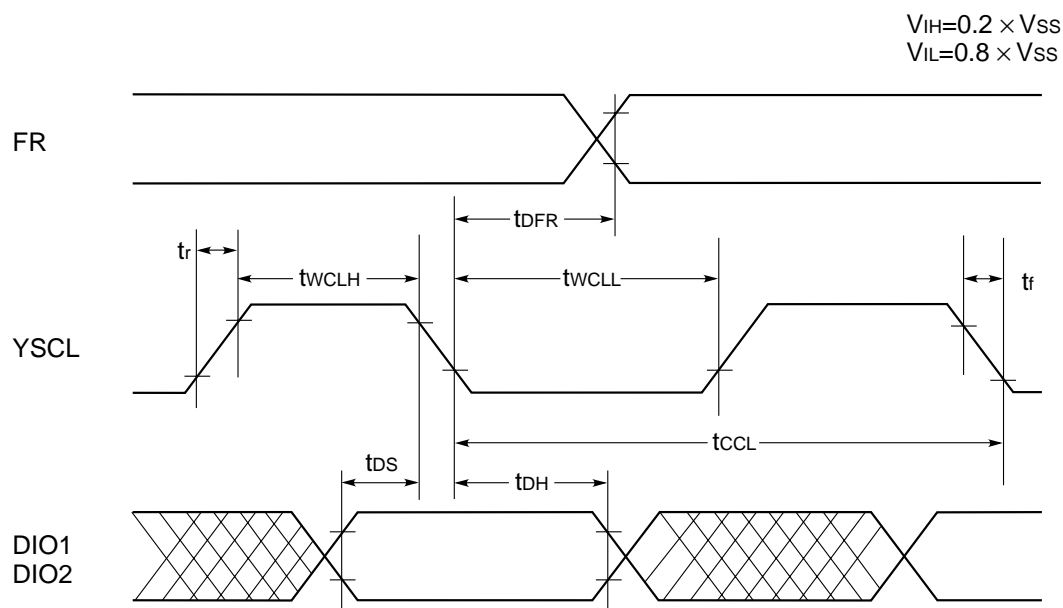
Operating Voltage Range VSS – V5

V5 voltage must be set within the following operating voltage range of VSS – V5.



## AC Characteristics

## Input timing characteristics



Unless otherwise specified  $V_{SS}=-5.0V \pm 10\%$ ,  $T_a=-40$  to  $85^\circ\text{C}$

Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	$t_r$	—	—	50	ns
Input signal fall time	$t_f$	—	—	50	ns
YSCL period	$t_{cCL}$	—	500	—	ns
YSCL HIGH pulsewidth	$t_{wCLH}$	—	70	—	ns
YSCL LOW pulsewidth	$t_{wCLL}$	—	330	—	ns
Data setup time	$t_{ds}$	—	100	—	ns
Data hold time	$t_{DH}$	—	10	—	ns
Allowable FR delay time	$t_{DFR}$	—	-500	500	ns

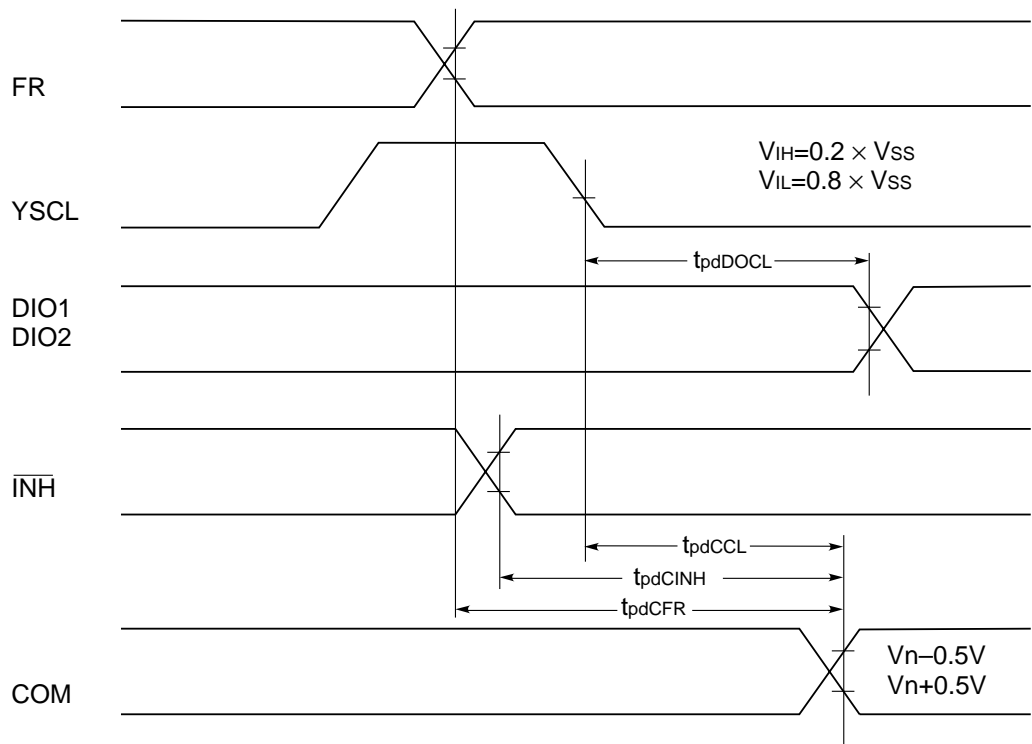
Unless otherwise specified  $V_{SS}=-2.7V$  to  $-4.5V$ ,  $T_a=-40$  to  $85^\circ\text{C}$

Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	$t_r$	—	—	50	ns
Input signal fall time	$t_f$	—	—	50	ns
YSCL period	$t_{cCL}$	—	1000	—	ns
YSCL HIGH pulsewidth	$t_{wCLH}$	—	160	—	ns
YSCL LOW pulsewidth	$t_{wCLL}$	—	330	—	ns
Data setup time	$t_{ds}$	—	200	—	ns
Data hold time	$t_{DH}$	—	10	—	ns
Allowable FR delay time	$t_{DFR}$	—	-500	500	ns

The standard applicable to  $t_{cCL}$ ,  $t_{wCLH}$ ,  $t_{wCLL}$ ,  $t_{ds}$  and  $t_{DH}$  when  $V_{SS} = -2.4V$  must be 1.3 times of that applies when  $V_{SS} = -2.7V$  to  $-4.5V$ .



Output timing characteristics



Unless otherwise specified  $V_{SS}=-5.0V \pm 10\%$ ,  $T_a=-40$  to  $85^\circ C$

Parament	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	$t_{pdDOCL}$	$CL=15pF$	30	300	ns
(YSCL - fall to COM output) delay time	$t_{pdCCL}$	$V_5=-7.0$ to $-28.0V$	-	3.0	$\mu s$
( $\overline{INH}$ to COM output) delay time	$t_{pdCINH}$				
(FR to COM output) delay time	$t_{pdCFR}$	$CL=100pF$	-	3.0	$\mu s$

Unless otherwise specified  $V_{SS}=-2.7V$  to  $-4.5V$ ,  $T_a=-40$  to  $85^\circ C$

Parament	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	$t_{pdDOCL}$	$CL=15pF$	60	600	ns
(YSCL - fall to COM output) delay time	$t_{pdCCL}$	$V_5=-7.0$ to $-28.0V$	-	3.0	$\mu s$
( $\overline{INH}$ to COM output) delay time	$t_{pdCINH}$				
(FR to COM output) delay time	$t_{pdCFR}$	$CL=100pF$	-	3.0	$\mu s$

The standard applicable when  $V_{SS} = -2.4 V$  must be 1.3 times of that applies when  $V_{SS} = -2.7 V$  to  $-4.5 V$ .

## 11. LCD DRIVE POWER

### Each voltage level forming method

To obtain each voltage level for LCD driving, it is the most simple to divide the resistance of potential as shown in the connection example.

On the other hand, to obtain a high quality display, it is necessary to raise the accuracy and constancy of each voltage level and to set the divided resistance value as low as possible in the range of system power capacity. Especially when a low-power LCD driving is required, set the divided resistance to a higher value and drive the LCD with a voltage follower by means of operational amplifier instead. In taking into consideration of a case where the operational amplifier is employed, the maximum potential level  $V_0$  for LCD driving has been isolated from the VDD pin. When the potential of  $V_0$  lowers than that of VDD and the potential difference between the two becomes larger, however, the capacity of LCD drive output driver lowers. To avoid it, use the system with the potential difference of 0 V to 2.5 V between  $V_0$  and VDD.

When no operational amplifier is used, connect  $V_0$  and VDD pins.

### Note in power ON/OFF

Since this LSI is high in the voltage of LCD driving system, when a high voltage is applied to the LCD driving system with the logic system power supply kept floating, an overcurrent flows and LSI breaks down in some cases.

### Be sure to follow the power ON/OFF sequence as shown below:

At power ON ... Logic system ON → LCD driving system ON or simultaneous ON of the both  
 At power OFF ... LCD driving system OFF → Logic system OFF or simultaneous OFF of the both

### Precautions:

Users of this development specification are reminded of the following precautions.

1. This development specification is subject to change without previous notice.
2. This specification does not warrant the user to exercise the industrial property right or other rights, nor does this specification vest such rights to the user.  
 Application examples provided in this specification are solely intended to ensure better understanding of the product. The manufacturer shall not be liable for any circuit related problem arising from using such examples.  
 Numeric representation of measure or size provided in the characteristics table is one obtained from the numeric line.
3. No part of this specification may be reproduced or duplicated in any form or by any means without the written permission of the manufacturer.
4. As for use of semiconductor elements, users are required to pay attention to the following points.  
 [Precautions on the Product Handling in Light]  
 Characteristics of semiconductor elements are changed if they are exposed to light. Thus, exposing this IC to light can result in its malfunction. In order to prevent IC malfunctioning due to light, make sure that the following measures are taken for the boards or products equipped with our IC.
  - (1) Design and mounting procedure employed do not allow light to IC.
  - (2) The inspection process is implemented in the environment that does not allow light to IC.
  - (3) Light shielding measures are established not only for surface of IC but also for rear face and side faces, too.

# 12. DIFFERENT POINTS FROM REPLACEMENT PRODUCT

	S1D16702*00**	S1D16300*****
Function	Bidirectional shift register INH 68 output segments	Bidirectional shift register INH 68 output segments
Output Tr configuration	Fig. 1	Fig. 2
PAD layout	Identical to the equivalent product	—
PAD coordinates	Different from the equivalent product	—

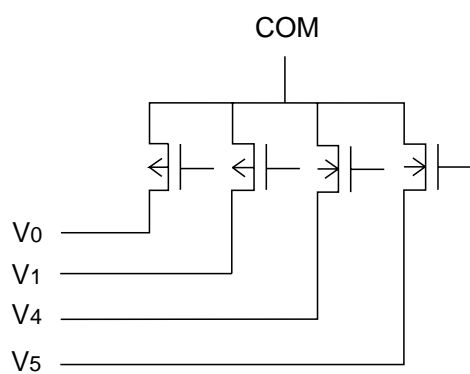


Fig. 1

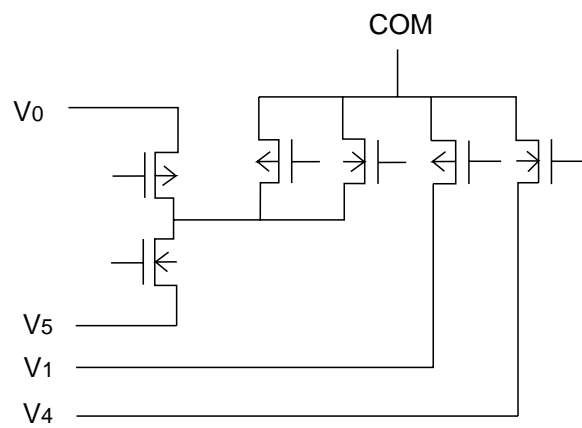


Fig. 2

# EPSON International Sales Operations

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# **S1D16000 Series**

## Technical Manual

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