

DESCRIPTION

2SK930 is a super mini outline resin sealed silicon N channel junction type FET. It is designed for low frequency voltage amplify, application, analog switch application.

FEATURE

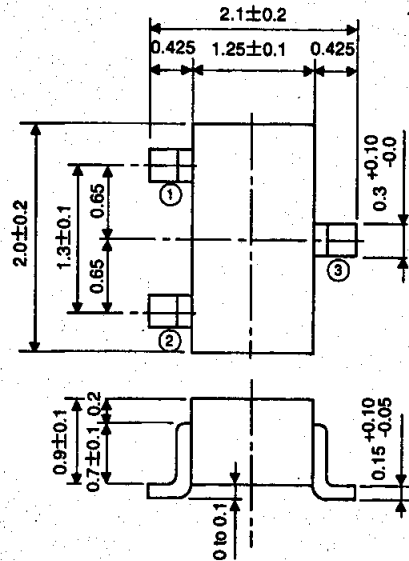
- Small type for mounting
- High $|y_{fs}|$ $|y_{fs}| = 4\text{mS}(\text{typ})$
- Low $R_{DS(ON)}$ $R_{DS(ON)} = 250\Omega$ typ

APPLICATION

General purpose voltage amplify, analog switch circuit for stereo, cassette deck, VCR.

OUTLINE DRAWING

Unit:mm



TERMINAL CONNECTOR

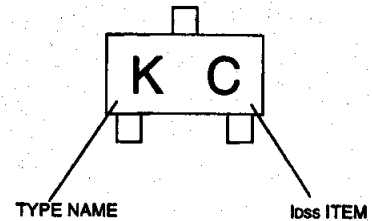
- ① : SOURCE
- ② : DRAIN
- ③ : GATE

EIAJ : SC-70

Note)

The dimension without tolerance represent central value.

MARKING



MAXIMUM RATINGS (Ta=25°C)

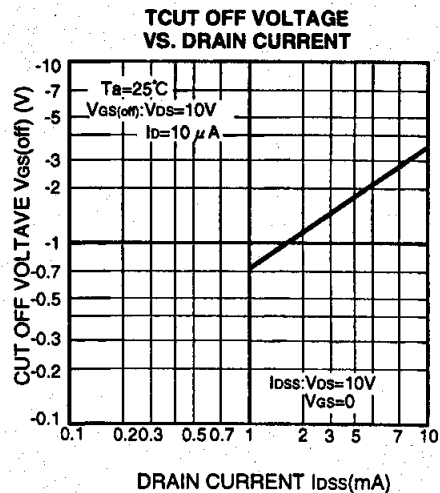
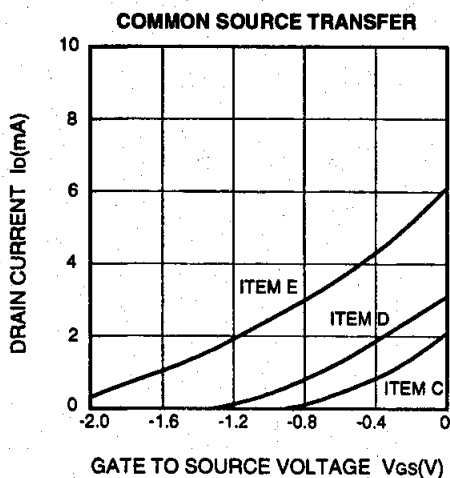
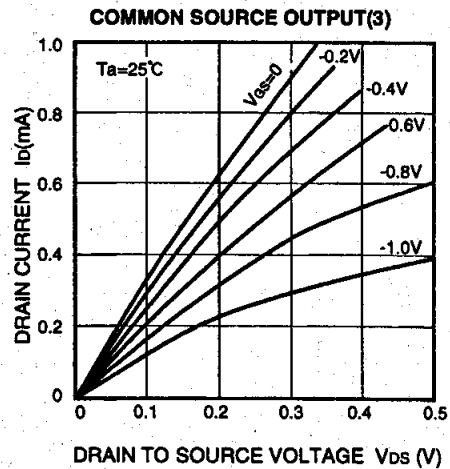
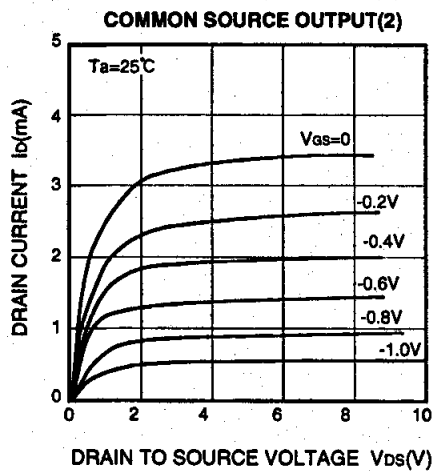
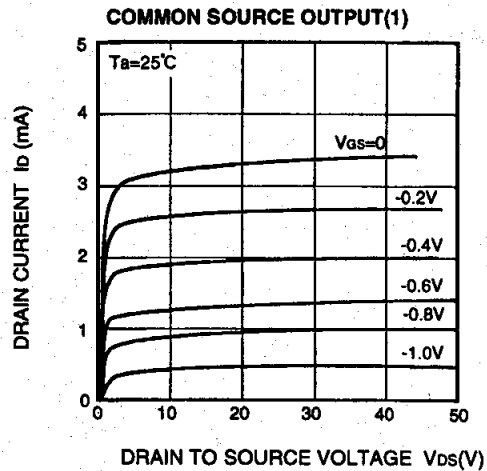
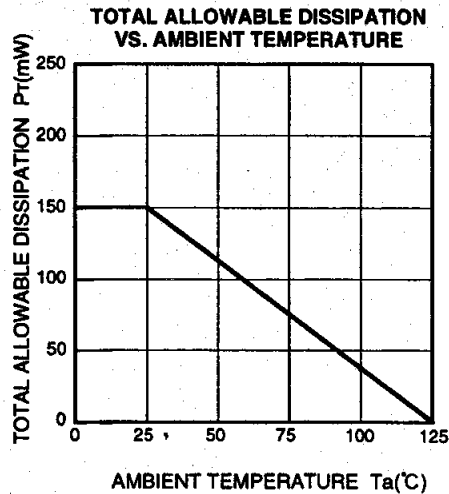
Symbol	Parameter	Ratings	Unit
V _{GD0}	Gate to Drain voltage	-50	V
I _g	Gate current	10	mA
P _T	Total allowable dissipation(Ta=25°C)	150	mW
T _{ch}	Channel temperature	+125	°C
T _{stg}	Storage temperature	-55 to +125	°C

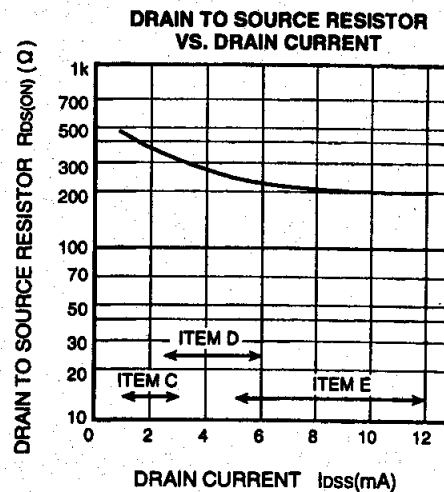
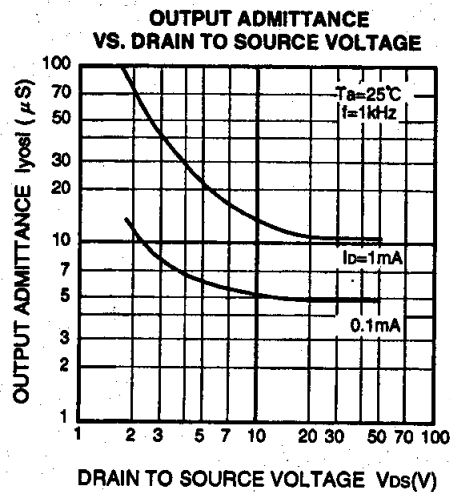
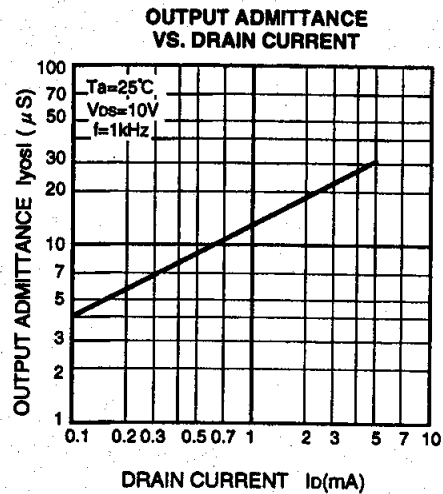
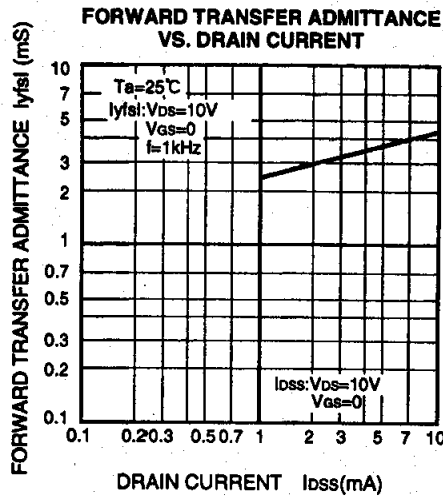
ELECTRICAL CHARACTERISTICS (Ta=25°C)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{(BR)GDO}	G to D break down voltage	I _g =-10μA, I _s =0	-50			V
I _{GSS}	Gate leakage current	V _{GS} =-30V, V _{DS} =0			-1	nA
I _{DSS} *	Drain current	V _{DS} =10V, V _{GS} =0	1.0		12	mA
V _{GS(off)}	Cut off voltage	V _{DS} =10V, I _D =10μA	-0.3	-1.5	-6.0	V
y _{fs}	Forward transfer admittance	V _{DS} =10V, V _{GS} =0, f=1kHz	1.0	3.0		mS
y _{os}	Output admittance	V _{DS} =10V, V _{GS} =0, f=1kHz		10		μS
C _{iss}	Input capacitance	V _{DS} =10V, V _{GS} =0, f=1MHz		8		pF
C _{rss}	Feed back capacitance	V _{DS} =10V, V _{GS} =0, f=1MHz		1.5		pF
R _{DS(ON)}	Drain to source resistor	V _{DS} =10mVrms(1kHz), V _{GS} =0, I _{DSS} =5mA		250		Ω

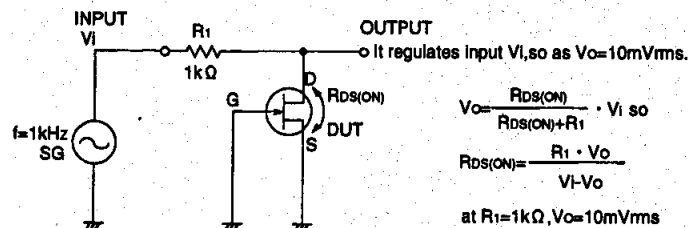
* : It shows loss classification in right table.

Item	C	D	E
I _{DSS}	1.0 to 3.0	2.5 to 6.0	5.0 to 12

**FOR LOW FREQUENCY AMPLIFY APPLICATION
N CHANNEL JUNCTION TYPE****TYPICAL CHARACTERISTICS**



DRAIN TO SOURCE RESISTOR $R_{ds(on)}$ TEST CIRCUIT





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