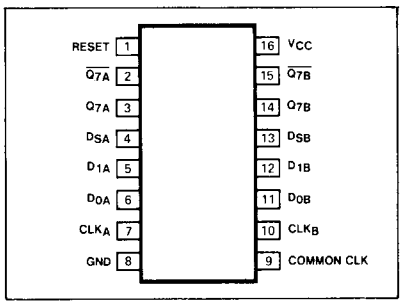
DESCRIPTION

The 8277 is a dual 8-Bit Shift Register which provides the designer with sixteen (16) bits of serial storage operating at a typical shift rate of 20MHz. Features of the 8277 are:

1. TRUE and COMPLEMENT outputs are provided on each register's eighth bit.
2. Positive edge triggering on clock input.
3. SEPARATE CLOCK lines (pins 7 and 10) for each 8-bit register are provided as well as a COMMON CLOCK line (pin 9) for all sixteen storage bits.
4. Common RESET (pin 1).
5. AND-OR gating to the input of each 8-bit register is provided to accomplish the multiplex function.
6. Direct replacement for 9328.

PIN CONFIGURATION



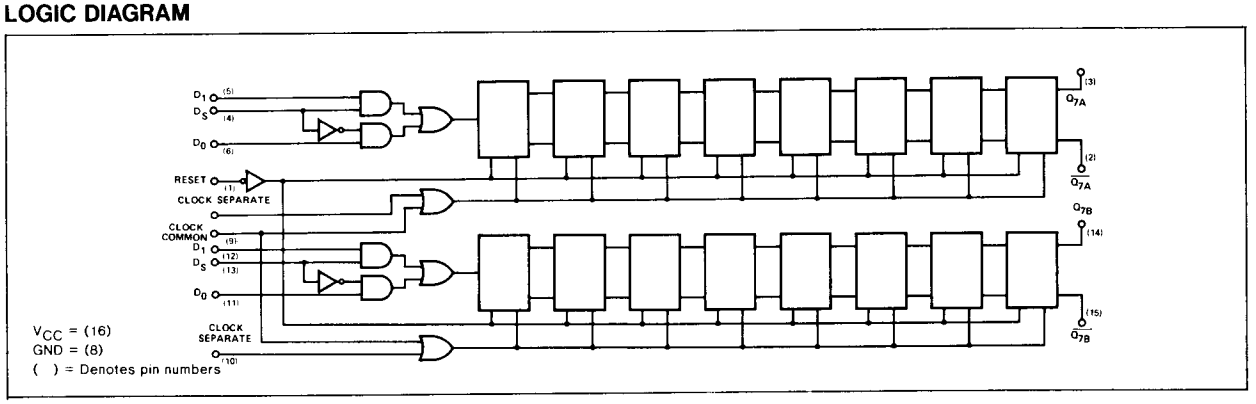
ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V_{CC}=5V ± 5%; T_A=0°C to +75°C	MILITARY RANGES V_{CC}=5V ± 5%; T_A=−55°C to +125°C
Plastic DIP	N8277N	
Ceramic DIP	N8277F	
Flatpak		

FUNCTION TABLE

D_S	D_0	D_1	Reset	Function
L	L	X	H	Shift in "0"
L	H	X	H	Shift in "1"
H	X	L	H	Shift in "0"
H	X	H	H	Shift in "1"
X	X	X	L	Reset "Q" to "0"

LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	8277 Min	8277 Max	UNIT
V_{OH}	Output HIGH voltage	V_{CC} = 4.75V, I_{OH} = −800μA	2.6		V
V_{OL}	Output LOW voltage	V_{CC} = 4.75V, I_{OL} = 16mA		0.4	V
I_{IH}	Input HIGH Current Data, Reset, Clock separate Data select, Clock common	V_{CC} = 5.25V, V_{IN} = 4.5V		 40 80	 μA μA
I_{IL}	Input LOW current Data, Reset, Clock separate Data select, Clock common	V_{CC} = 5.25V, V_{IN} = 0.4V		 −1.6 −3.2	 mA mA
V_{BD}	Input breakdown voltage	V_{CC} = 4.75V, I_{IN} = 10mA	5.5		V
I_{CC}	Supply current	V_{CC} = 5.25V		103	mA

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AC CHARACTERISTICS: T_A = 25° C (See Section 4 for Waveforms and Conditions)

PARAMETER		TEST CONDITIONS	8277 C_L = 18pF R_1 = ∞Ω R_2 = 84.5Ω		UNIT
			Min	Max	
t_{PHL} t_{PLH}	Propagation delay Clock to output	Figure 1		40 40	ns ns
t_{PHL} t_{PLH}	Propagation delay Reset to output	Figure 1		40 40	ns ns

NOTE
b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

	PARAMETER	TEST CONDITIONS	8277		UNIT
			Min	Max	
f_{Max}	Maximum clock frequency		15		MHz
t_W	Clock pulse width	Figure 1	15		ns
t_s	Set-up time	Figure 1	30		ns
t_h	Hold time	Figure 1	5		ns

AC WAVEFORM