

LVDS UHF VCXO AB-A3DBXXX Series

Description

The **AB-A3DBXXX Series** of voltage controlled crystal oscillators (VCXO) provides ultra high frequency with LVDS complementary outputs. The outputs can be disabled for test automation or combining multiple clocks. The device is based on low noise analog harmonic frequency multiplication, providing exceptionally low Phase Noise and Jitter. It is packaged in a miniature, FR-4 based 9x14mm SMD package.

Applications and Features

- Wide frequency range – 200.0MHz to 1.000GHz
- Fiber Channel; 10 GbE; Infiniband; Network Processors; SONET/SDH
- High Reliability - NEL HALT/HASS qualified for crystal oscillator start-up conditions
- Extremely Low Phase Noise and Jitter
- High shock resistance, to 1000g
- Absolute Pull Range (APR) to ± 1000 ppm
- SONET ± 20 ppm overall free-run stability available
- RoHS Compliant, Lead Free Construction

Creating a Part Number			
AB - A 3DB X X X - FREQ			
<u>Package Code</u>		<u>Absolute Pull Range, ppm</u>	
AB	6 pad 9x14 mm SMD	E	± 20
		F	± 32
		G	± 50
		H	± 100
		9	Customer specific
<u>Input Voltage</u>		<u>Temperature Range, °C</u>	
A	3.3V $\pm 5\%$	A	0 to 50
		B	0 to 70
		C	-20 to 70
		D	-40 to 85
		9	Customer specific
<u>Enable Option</u>			
H	Positive CMOS Enable		
N	N/A		



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Operating Temperature Range	To	-40 to +85	°C
Storage Temperature Range	Tst	-50 to +90	°C
Supply Voltage	Vcc	-0.5 to 4.5	V
Enable/Disable Voltage	Ven/dis	0 to Vcc	V

Electrical Parameters

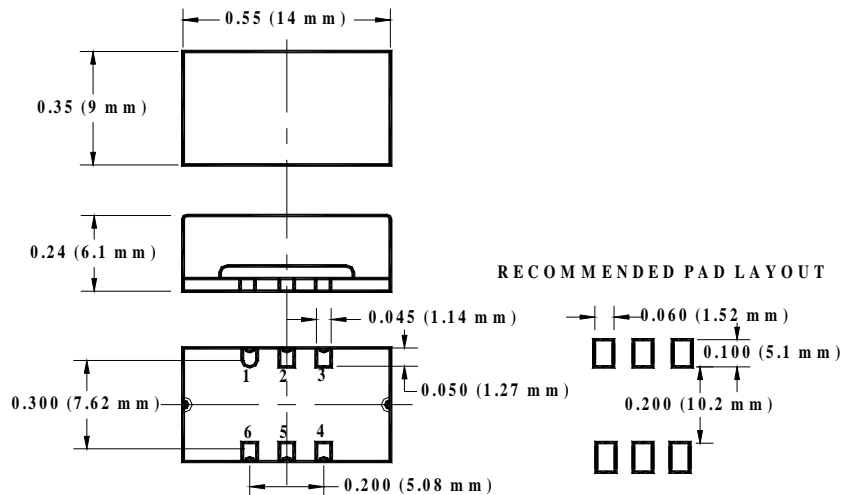
Parameter		Symb	Conditions, Note	MIN	TYP	MAX	Unit
Nominal Frequency		Fo		200		1000	MHz
Supply Voltage		Vcc	Code A	3.135	3.3	3.465	V
Supply current		Icc			50	60	mA
Output Logic Type					LVDS		
Load			At receiving end between the outputs	90	100	110	Ohm
Output Levels		Vod	Differential amplitude	247	330	454	mV
			Amplitude error			50	mV
		Vof	Offset Voltage	1.125	1.25	1.375	V
			Offset Voltage error			50	mV
Duty Cycle (Symmetry)			At outputs crossing, room temperature	45/55	50/50	55/45	%
Rise/Fall Time		Tr/Tf	20 to 80, 80 to 20 %		0.5	0.7	ns
Jitter	Integrated	J	Integrated from Phase Noise, 12 KHz to 20 MHz , RMS		0.1	0.2	ps
			100 Hz to 80 KHz, RMS			1.0	ps
			50 Khz to 80 Mhz		0.3		ps
	Wavecrest characterized		Random period,		2.5		ps
			Accumul., pk-to-pk		25		ps
			Deterministic		1		ps
			Sub-Harmonics			@ 622.08MHz	
Phase Noise		£(Δf)	622.08 MHz, APR 50ppm or less	@ 10 Hz @100 Hz @1 KHz @10KHz @100KHz @>1MHz	-60 -90 -118 -135 -135 -140	-55 -85 -113 -130 -130 -135	dBc/Hz
Frequency Stability		ΔF/F	Overall, including initial calibration, temperature, aging 10 years, shock and vibration @ Vc=Vcc/2; APR 50ppm, or less	±20	±30		ppm
Control Voltage Range		Vc		0V		Vcc	V
Setability		Vcs	Vc to set F at Fo; T, Vcc, load - nominal, as shipped	0.4 Vcc	0.5 Vcc	0.6 Vcc	V
Absolute Pull Range		APR	Over all conditions, see part # creation	20,32, 50,100			ppm
Input Impedance		Zin	@ Fmod < 100 Khz	50			KOhm
Modulation Bandwidth			At Vc = Vcc/2, -3dB	20			KHz
Enable/Disable Option							
Pin 2 Enabled			CMOS logic 1 or N/C	0.7 Vcc		Vcc	V
Pin 2 Disabled			CMOS logic 0	0		0.3 Vcc	

Rev. B

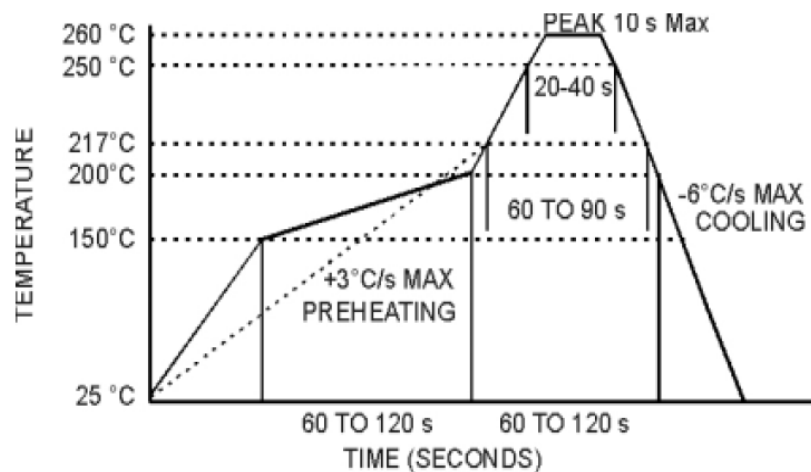
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Electrical Connection

Pin	Connection
1	V _{co}
2	Enable/Disable
3	Gnd
4	Output
5	Output Complement
6	V _{cc}

**Environmental and Mechanical Characteristics**

Operating temp. range	see part # table
Mechanical Shock	Per MIL-STD-202, Method 213, Cond. E
Thermal Shock	Per MIL-STD-883, Method 1011, Cond. A
Vibration	Per MIL-STD-883, Method 2007, Cond. A
Hermetic Seal	Leak rate less than 1×10^{-8} atm.cc/s of helium
Soldering conditions	See MAX reflow profile below

Maximum Reflow Profile**NEL**

FREQUENCY
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