

GENERAL DESCRIPTION

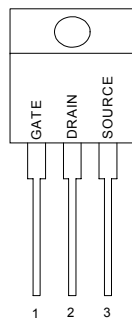
This Power MOSFET is designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

FEATURES

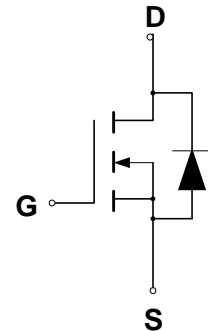
- ◆ Dynamic dv/dt Rating
- ◆ Repetitive Avalanche Rated
- ◆ Fast Switching
- ◆ Ease of Paralleling
- ◆ Simple Drive Requirements

PIN CONFIGURATION

TO-220
Top View



SYMBOL



N-Channel MOSFET

ORDERING INFORMATION

Part Number	Package
CMT09N20N220	TO-220

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain to Current — Continuous	I_D	9.0	A
— Pulsed (Note 1)	I_{DM}	36	
Gate-to-Source Voltage — Continue	V_{GS}	± 20	V
Total Power Dissipation	P_D	74	W
Derate above 25°C		0.59	W/°C
Single Pulse Avalanche Energy (Note 2)	E_{AS}	56	mJ
Avalanche Current (Note 1)	I_{AR}	9.0	A
Repetitive Avalanche Energy (Note 1)	E_{AR}	7.4	mJ
Peak Diode Recovery dv/dt	dv/dt	5.0	V/ns
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C
Thermal Resistance — Junction to Case	θ_{JC}	1.70	°C/W
— Junction to Ambient	θ_{JA}	62	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	300	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_J = 25^\circ\text{C}$.

		CMT09N20				
Characteristic	Symbol	Min	Typ	Max	Units	
Drain-Source Breakdown Voltage (V _{GS} = 0 V, I _D = 250 μA)	V _{(BR)DSS}	200			V	
Drain-Source Leakage Current (V _{DS} = 200V, V _{GS} = 0 V) (V _{DS} = 160V, V _{GS} = 0 V, T _J = 125°C)	I _{DSS}			25 250	μA	
Gate-Source Leakage Current-Forward (V _{gsf} = 20 V, V _{DS} = 0 V)	I _{GSSF}			100	nA	
Gate-Source Leakage Current-Reverse (V _{gsr} = -20 V, V _{DS} = 0 V)	I _{GSSR}			-100	nA	
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μA)	V _{GS(th)}	2.0		4.0	V	
Static Drain-Source On-Resistance (V _{GS} = 10 V, I _D = 5.4A) (Note 4)		R _{DS(on)}		0.40	Ω	
Forward Transconductance (V _{DS} = 50V, I _D = 5.4 A) (Note 4)		g _{FS}	3.8		mhos	
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz)	C _{iss}		800	pF	
Output Capacitance		C _{oss}		240	pF	
Reverse Transfer Capacitance		C _{rss}		76	pF	
Turn-On Delay Time	(V _{DD} = 100 V, I _D = 5.9 A, R _G = 12Ω, R _D = 16Ω) (Note 4)	t _{d(on)}		9.4	ns	
Rise Time		t _r		28	ns	
Turn-Off Delay Time		t _{d(off)}		39	ns	
Fall Time		t _f		20	ns	
Total Gate Charge	(V _{DS} = 160V, I _D = 5.9A V _{GS} = 10 V) (Note 4)	Q _g		43	nC	
Gate-Source Charge		Q _{gs}		7.0	nC	
Gate-Drain Charge		Q _{gd}		23	nC	
Internal Drain Inductance (Measured from the drain lead 0.25" from package to center of die)		L _D		4.5	nH	
Internal Drain Inductance (Measured from the source lead 0.25" from package to source bond pad)		L _S		7.5	nH	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Reverse Recovery Charge	I _F = 5.9A, di/dt = 100A/μs , T _J = 25°C (Note 4)	Q _{rr}		1.1	2.2	μC
Forward Turn-On Time		t _{on}		**		
Reverse Recovery Time		t _{rr}		170	340	ns
Diode Forward Voltage	I _S = 9.0A, V _{GS} = 0 V, T _J = 25°C (Note 4)	V _{SD}			1.5	V

Note

- (1) Repetitive rating; pulse width limited by max. junction temperature
 - (2) $V_{DD} = 100\text{ V}$, $V_{GS} = 10\text{ V}$, starting $T_J = 25^\circ\text{C}$, $L = 1.38\text{ mH}$, $R_G = 25\Omega$, $I_{AS} = 9.0\text{ A}$
 - (3) $I_{SD} \leq 9.0\text{ A}$, $di/dt \leq 120\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$
 - (4) Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
- ** Negligible, Dominated by circuit inductance

TYPICAL ELECTRICAL CHARACTERISTICS

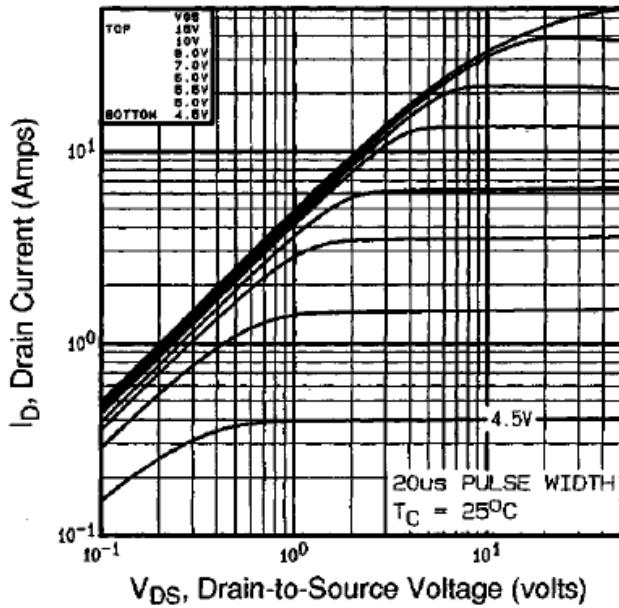


Fig 1. Typical Output Characteristics,
 $T_C = 25^\circ\text{C}$

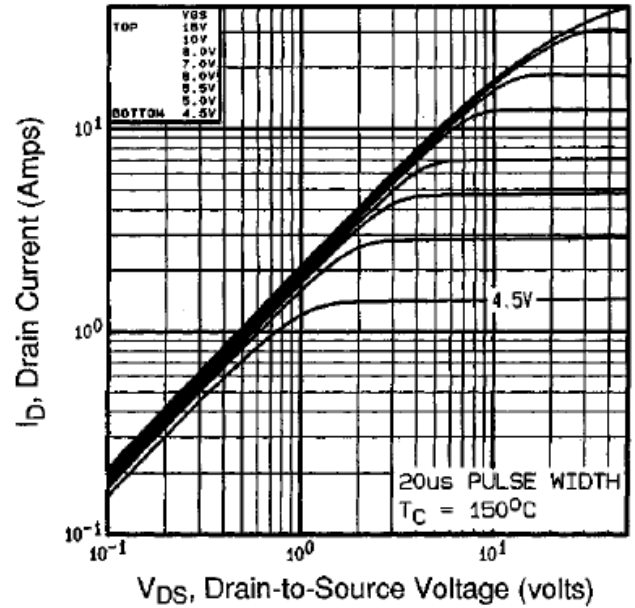


Fig 2. Typical Output Characteristics,
 $T_C = 150^\circ\text{C}$

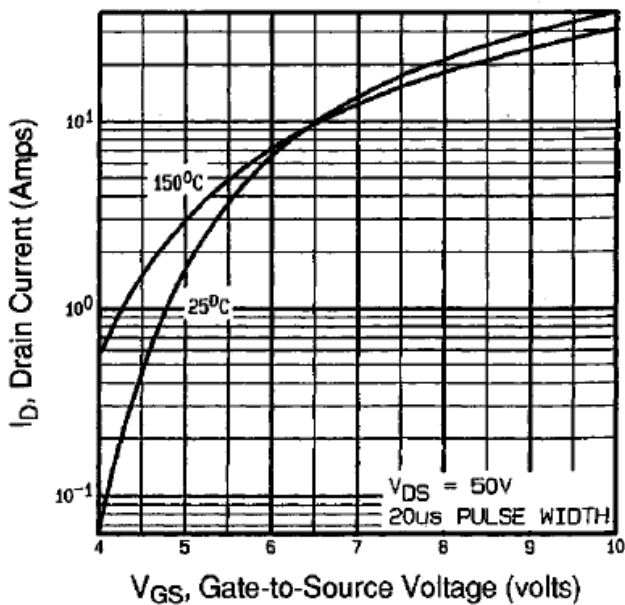


Fig 3. Typical Transfer Characteristics

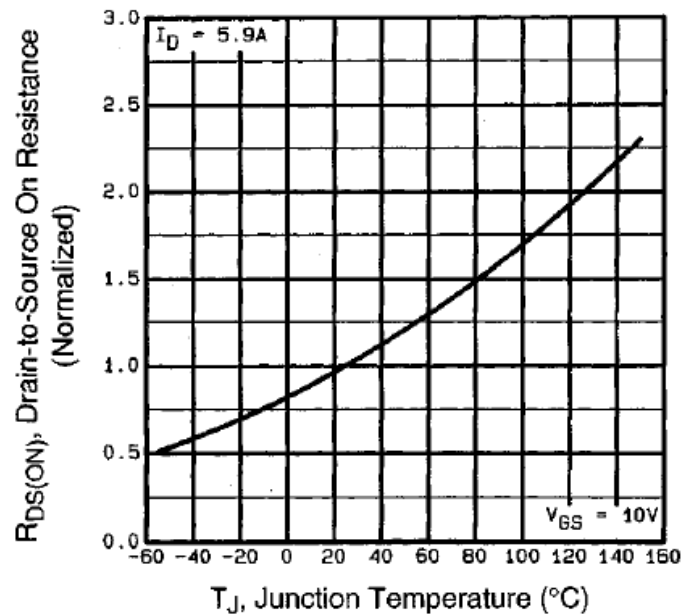


Fig 4. Normalized On-Resistance
Vs. Temperature

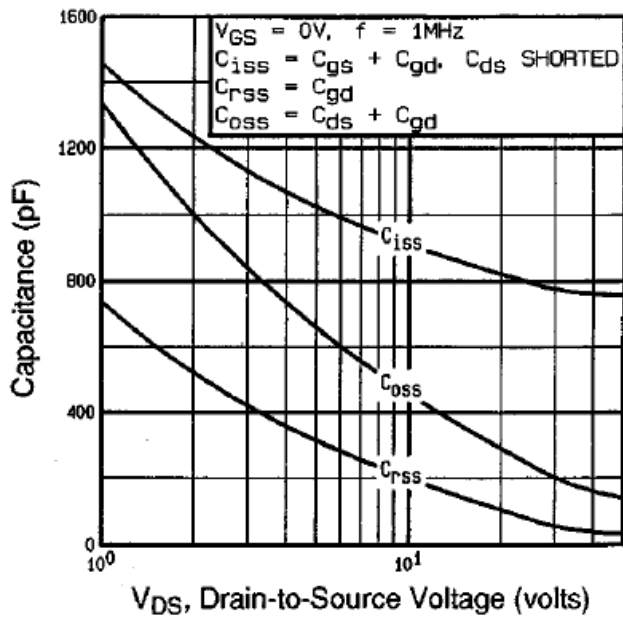


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

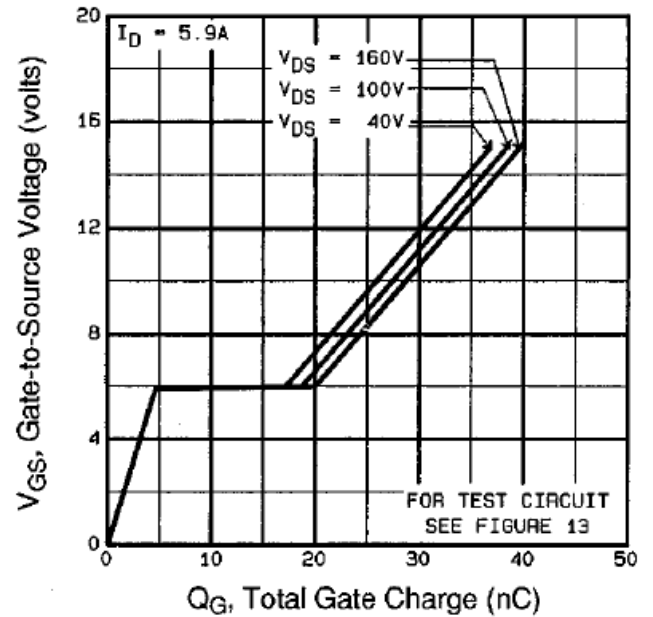


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

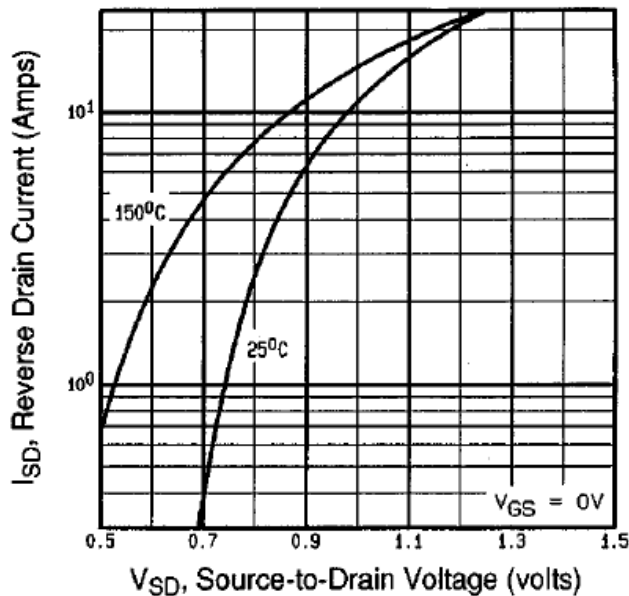


Fig 7. Typical Source-Drain Diode Forward Voltage

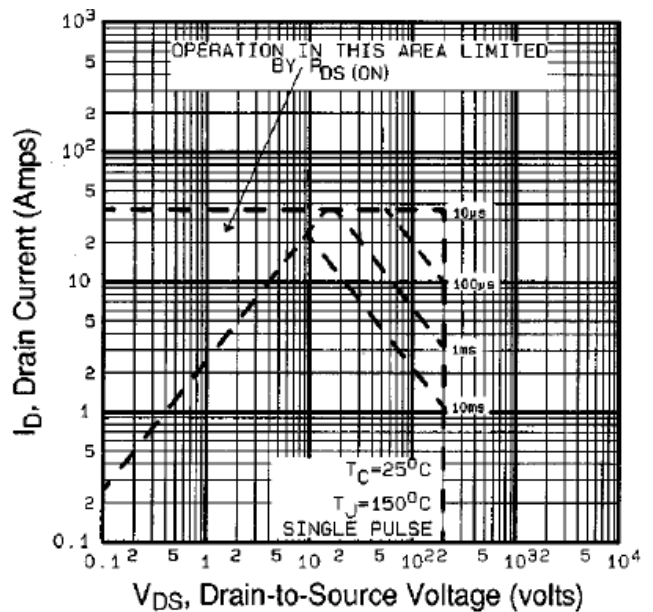


Fig 8. Maximum Safe Operating Area

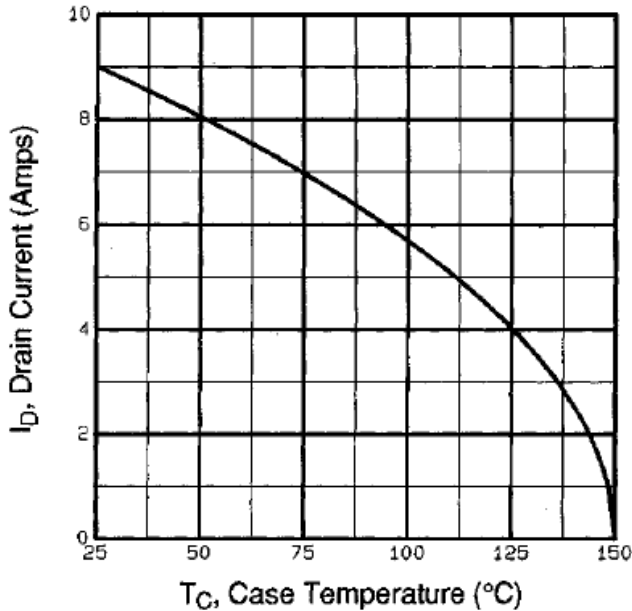


Fig 9. Maximum Drain Current Vs. Case Temperature

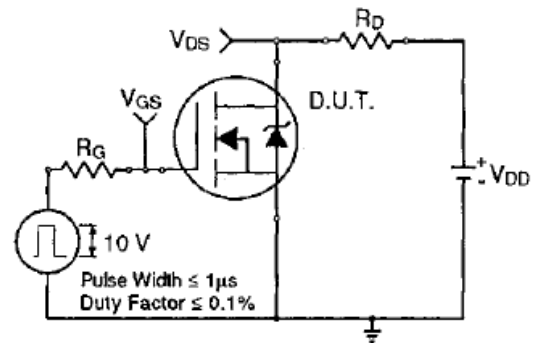


Fig 10a. Switching Time Test Circuit

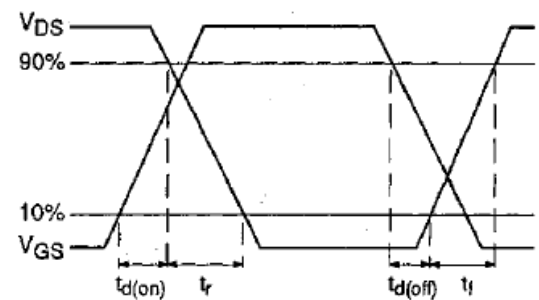


Fig 10b. Switching Time Waveforms

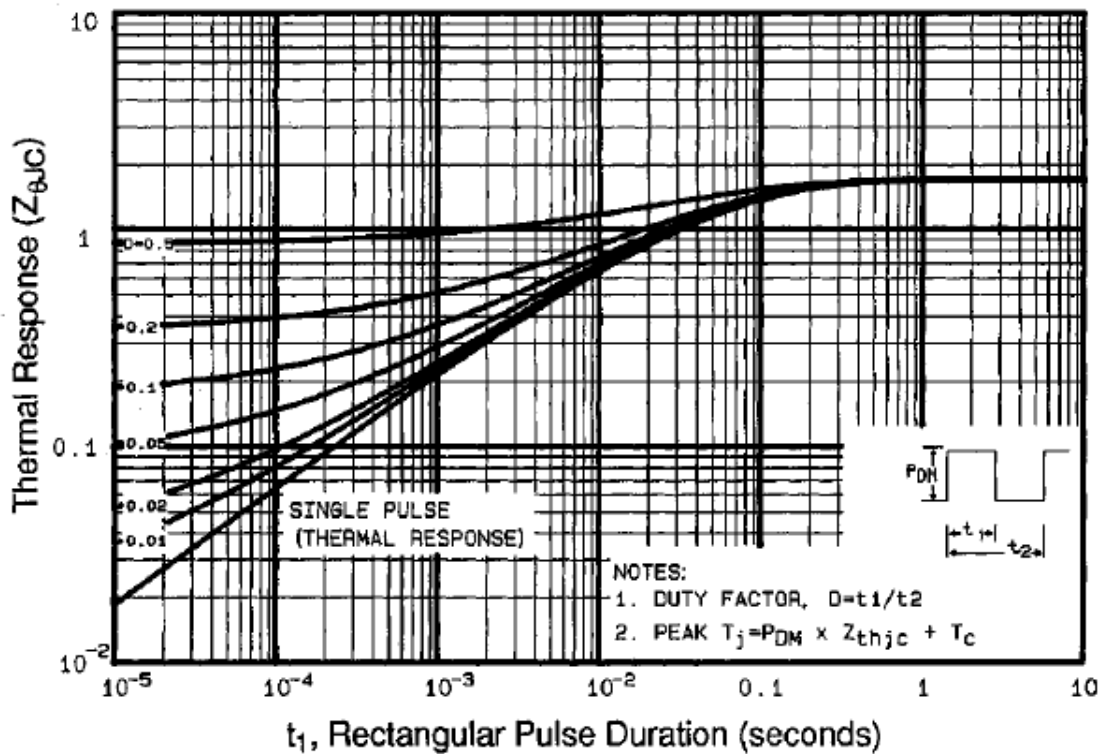


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

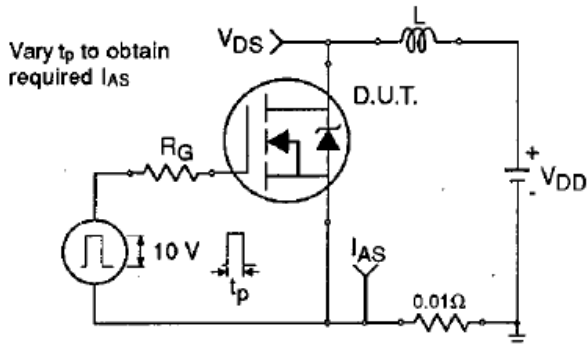


Fig 12a. Unclamped Inductive Test Circuit

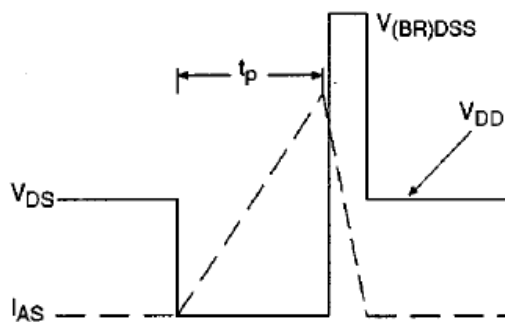


Fig 12b. Unclamped Inductive Waveforms

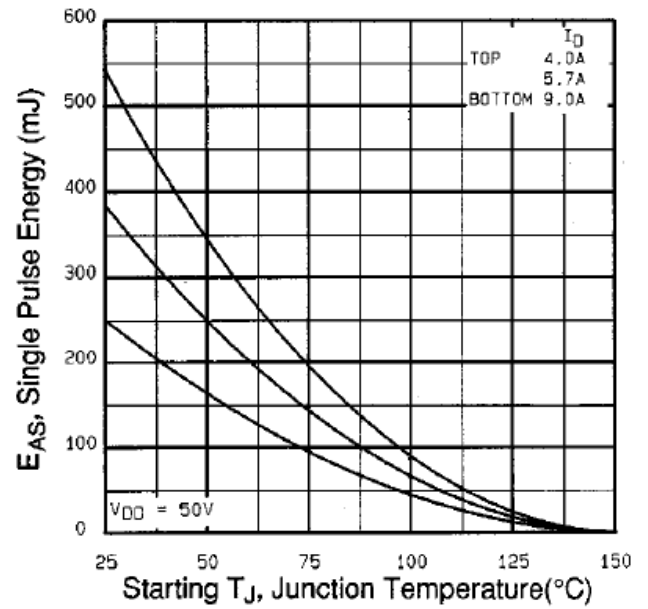


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

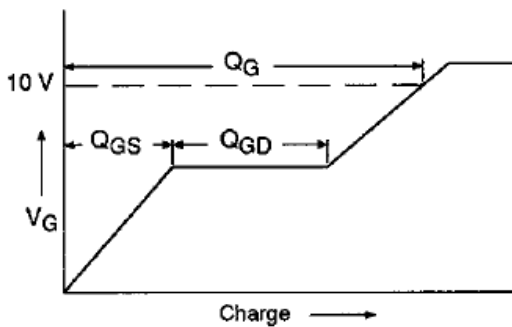


Fig 13a. Basic Gate Charge Waveform

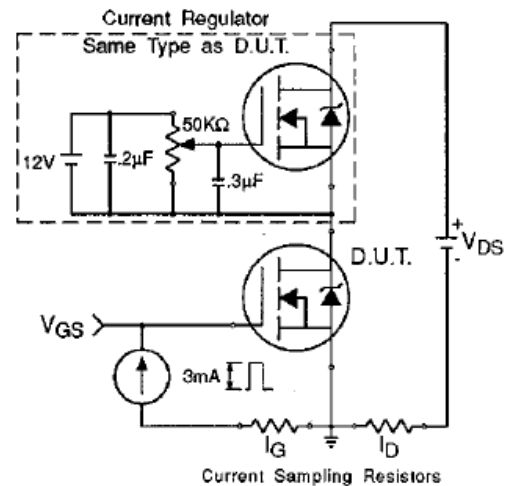
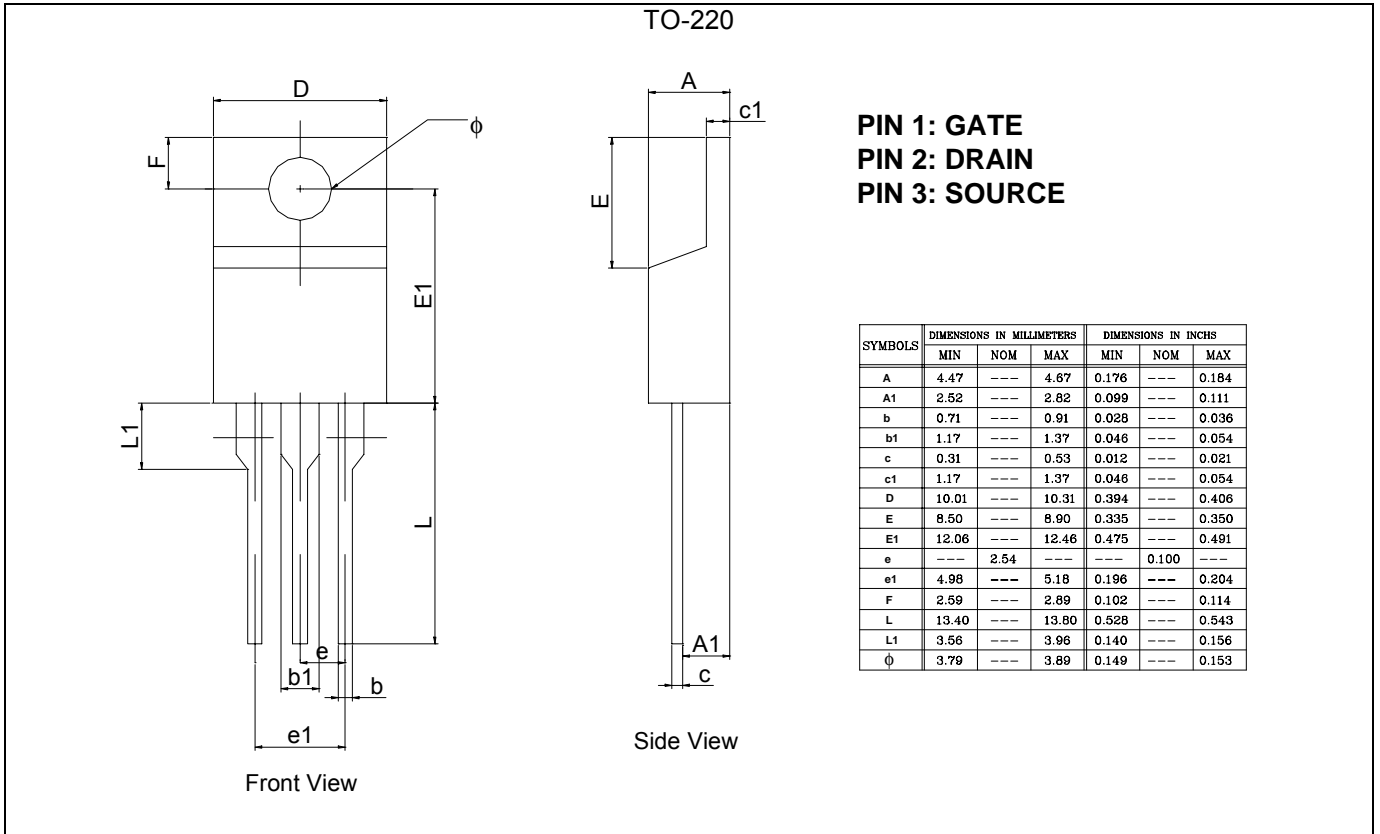


Fig 13b. Gate Charge Test Circuit

PACKAGE DIMENSION

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