



## TRI-STATE® Quad Buffers

## General Description

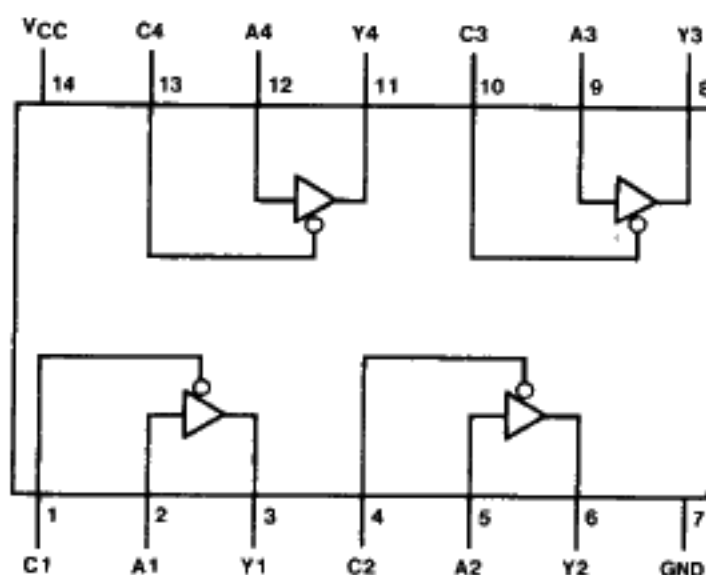
The DM7093/DM8093 and DM7094/DM8094 are quad two-input buffers which accept normal TTL or DTL input levels; and have outputs which provide either normal low-impedance TTL characteristics, or a high-impedance third logic state. One of the two inputs to each buffer is used as a control line to gate the output into the high-impedance state. The other input simply passes the non-inverted data through the buffer. The DM7093/DM8093 provides the high-impedance state when a high logic level is applied to the control input, the DM7094/DM8094 when a low logic level is applied to the control input. The low output impedance of these devices provides good capacitive-drive capability and rapid transition from the low to the high logic

levels, thus assuring both speed and waveform integrity. It is possible to connect as many as 128 devices to a common bus line, and still have adequate drive capability.

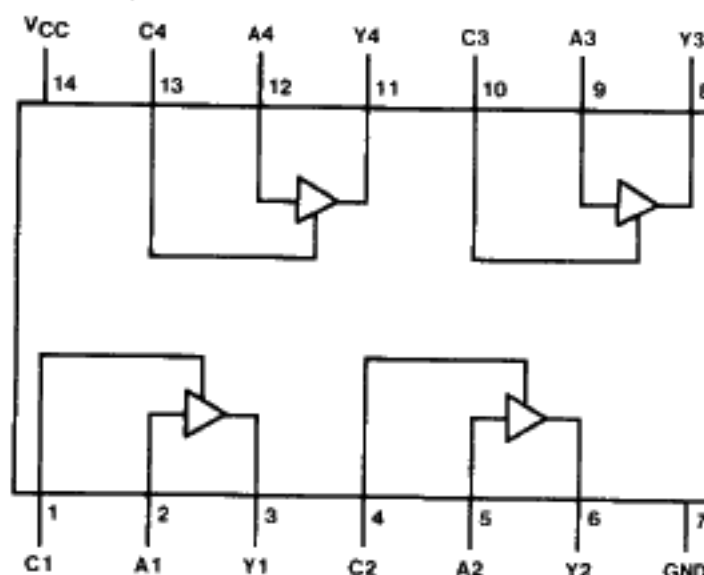
## Features

- Pin equivalent to DM54125/74125 (7093/8093) and DM54126/74126 (7094/8094)
- Up to 128 devices can be connected to a common bus line
- High capacitive-drive capability
- Independent control of each buffer
- Typical propagation delay—12 ns

## Connection Diagrams



7093 (J,W); 8093 (N)



7094 (J,W); 8094 (N)

## Truth Tables

DM7093/DM8093

Data	Controls	Outputs
H	L	H
L	L	L
X	H	Hi-Z

DM7094/DM8094

Data	Controls	Outputs
H	H	H
L	H	L
X	L	Hi-Z

**Electrical Characteristics** over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions	DM70			DM80			Units
			93, 94			93, 94			
			Min	Typ (1)	Max	Min	Typ (1)	Max	
V <sub>IH</sub>	High Level Input Voltage		2			2			V
V <sub>IL</sub>	Low Level Input Voltage				0.8			0.8	V
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> Min, I <sub>I</sub> = -12 mA			-1.5			-1.5	V
I <sub>OH</sub>	High Level Output Current				-2.0			-5.2	mA
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, V <sub>IH</sub> = 2 V V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = Max	2.4	3.4		2.4	3.1		V
I <sub>OL</sub>	Low Level Output Current				16			16	mA
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, V <sub>IH</sub> = 2 V V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 16 mA			0.4			0.4	V
I <sub>O(OFF)</sub>	Off-State (High Impedance State) Output Current	V <sub>CC</sub> = Max, V <sub>IH</sub> = 2 V V <sub>IL</sub> = 0.8 V			-40			-40	μA
		V <sub>O</sub> = 0.4 V V <sub>O</sub> = 2.4 V			40			40	
I <sub>I</sub>	Input Current at Maximum Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> 5.5 V			1			1	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.4 V			40			40	μA
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4 V			-1.6			-1.6	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (2)	-30		-70	-28		-70	mA
I <sub>CCH</sub>	Supply Current (Total, Outputs High)	V <sub>CC</sub> = Max		32	54		32	54	mA
I <sub>CCL</sub>	Supply Current (Total, Outputs Low)	V <sub>CC</sub> = Max		36	62		36	62	mA

Note 1: All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time.

**Switching Characteristics** V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

Parameter		Conditions	DM70/80						Units
			93			94			
			Min	Typ	Max	Min	Typ	Max	
tPLH	Propagation Delay Time, Low-to-High Level Output	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 400 Ω		10	15		10	15	ns
tPHL	Propagation Delay Time, High-to-Low Level Output			12	18		12	18	ns
tZH	Output Enable Time to High Level			12	18		13	19	ns
tZL	Output Enable Time to Low Level			16	25		16	25	ns
tHZ	Output Disable Time from High Level	C <sub>L</sub> = 5 pF, R <sub>L</sub> = 400 Ω		5	8		10	16	ns
tLZ	Output Disable Time from Low Level			9	14		14	20	ns