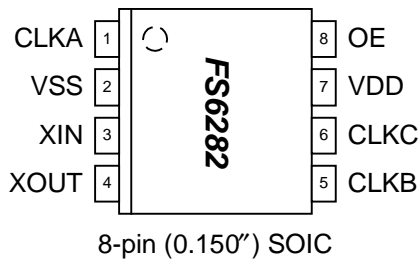


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### 1.0 Features

- Dual phase-locked loop (PLL) device with three output clock frequencies
- 3.3V supply voltage
- Small circuit board footprint (8-pin 0.150" SOIC)
- Custom frequency selections available - contact your local AMI Sales Representative for more information

**Figure 1: Pin Configuration**



### 2.0 Description

The FS6282 is a monolithic CMOS clock generator IC designed to minimize cost and component count in digital video/audio systems.

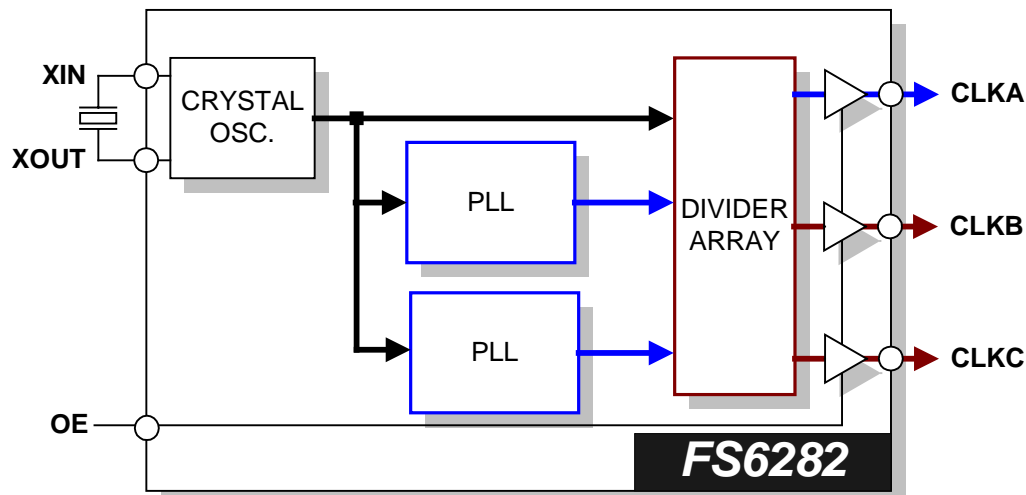
Two high-resolution phase-locked loops generate two output clocks (CLKA and CLKB) through an array of post-dividers. All frequencies are ratiometrically derived from the crystal oscillator frequency. The locking of all the output frequencies together can eliminate unpredictable artifacts in video systems and reduce electromagnetic interference (EMI) due to frequency harmonic stacking.

**Table 1: Crystal / Output Frequencies**

DEVICE	$f_{XIN}$ (MHz)	CLKA (MHz)	CLKB (MHz)	CLKC (MHz)
FS6282-03	20.000	20.000	48.000	8.000

NOTE: Contact AMI for custom PLL frequencies

**Figure 2: Block Diagram**



# FS6282

## Dual PLL Clock Generator IC



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### Table 2: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI<sup>U</sup> = Input with Internal Pull-Up; DI<sub>D</sub> = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low pin

PIN	TYPE	NAME	DESCRIPTION
1	DO	CLKA	Clock Output A
2	P	VSS	Ground
3	AI	XIN	Crystal Oscillator Feedback
4	AO	XOUT	Crystal Oscillator Drive
5	DO	CLKB	Clock Output B
6	DO	CLKC	Clock Output C
7	P	VDD	Power (+3.3 volts)
8	DI <sup>U</sup>	OE	Output Enable (outputs active when OE=VDD)

## 3.0 Electrical Specifications

### Table 3: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage ( $V_{SS}$ = ground)	$V_{DD}$	$V_{SS}-0.5$	7	V
Input Voltage, dc	$V_I$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	$V_O$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Input Clamp Current, dc ( $V_I < 0$ or $V_I > V_{DD}$ )	$I_{IK}$	-50	50	mA
Output Clamp Current, dc ( $V_I < 0$ or $V_I > V_{DD}$ )	$I_{OK}$	-50	50	mA
Storage Temperature Range (non-condensing)	$T_S$	-65	150	°C
Ambient Temperature Range, Under Bias	$T_A$	-55	125	°C
Junction Temperature	$T_J$		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV



#### **CAUTION: ELECTROSTATIC SENSITIVE DEVICE**

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

### Table 4: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	$V_{DD}$	3.3V $\pm$ 10%	3.0	3.3	3.6	V
Ambient Operating Temperature Range	$T_A$		0		70	°C

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### Table 5: DC Electrical Specifications

Unless otherwise stated,  $V_{DD} = 3.3V \pm 10\%$ , no load on any output, and ambient temperature range  $T_A = 0^\circ C$  to  $70^\circ C$ . Parameters denoted with an asterisk ( \* ) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are  $\pm 3\sigma$  from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
<b>Overall</b>						
Supply Current, Dynamic, with Loaded Outputs	$I_{DD}$	$f_{XTAL} = 13.5MHz$ ; $C_L = 10pF$ , $V_{DD} = 3.6V$		30		mA
<b>Crystal Oscillator</b>						
Crystal Loading Capacitance	$C_{L(xtal)}$	As seen by a crystal connected to XIN and XOUT		18		pF
<b>Clock Outputs (CLKA, CLKB)</b>						
Output Impedance *	$Z_{OH}$	$V_O = 0.1V_{DD}$ ; output driving high		45		$\Omega$
	$Z_{OL}$	$V_O = 0.1V_{DD}$ ; output driving low		45		
Short Circuit Source Current *	$I_{OSH}$	$V_O = 0V$ ; shorted for 30s, max.		-35		mA
Short Circuit Sink Current *	$I_{OSL}$	$V_O = 3.3V$ ; shorted for 30s, max.		35		mA

### Table 6: AC Timing Specifications

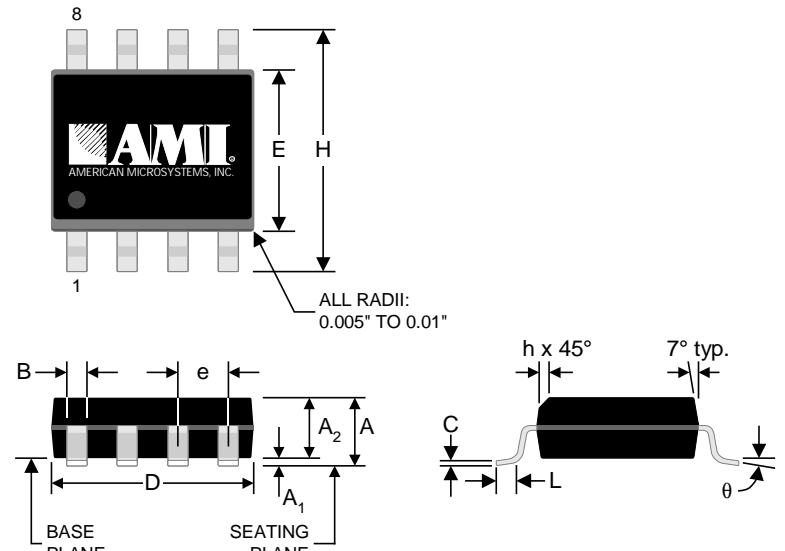
Unless otherwise stated,  $V_{DD} = 3.3V \pm 10\%$ , no load on any output, and ambient temperature range  $T_A = 0^\circ C$  to  $70^\circ C$ . Parameters denoted with an asterisk ( \* ) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are  $\pm 3\sigma$  from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
<b>Overall</b>						
Synthesis Error		(unless otherwise noted in Frequency Table)			0	ppm
<b>Clock Outputs (CLKA, CLKB, CLKC)</b>						
Duty Cycle *		Ratio of high pulse width (as measured from rising edge to next falling edge at $V_{DD}/2$ ) to one clock period	45		55	%
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to next rising edge at $V_{DD}/2$ , $C_L = 10pF$		300		ps
Rise Time *	$t_r$	$V_{DD} = 3.3V$ ; $V_O = 0.3V$ to $3.0V$ ; $C_L = 10pF$		3		ns
Fall Time *	$t_f$	$V_{DD} = 3.3V$ ; $V_O = 3.0V$ to $0.3V$ ; $C_L = 10pF$		2.5		ns

### 4.0 Package Information

**Table 7: 8-pin SOIC (0.150") Package Dimensions**

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.102	0.249
A2	0.055	0.061	1.40	1.55
B	0.013	0.019	0.33	0.49
C	0.0075	0.0098	0.191	0.249
D	0.189	0.196	4.80	4.98
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
$\Theta$	0°	8°	0°	8°



The diagram illustrates the mechanical dimensions of the 8-pin SOIC package. It includes a top view showing the package body with pins 1 through 8, and a side view showing the lead profile. Key dimensions labeled include: A (package height), A1 (lead height at base), A2 (lead height at seating plane), B (lead width), C (lead thickness), D (package width), E (package length), e (pitch), h (lead thickness), L (lead length), and  $\Theta$  (lead angle). The diagram also indicates 'ALL RADII: 0.005" TO 0.01"' and shows the 'BASE PLANE' and 'SEATING PLANE'.

**Table 8: 8-pin SOIC (0.150") Package Characteristics**

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air 8-pin 0.150" SOIC	$\Theta_{JA}$	Air flow = 0 m/s	110	°C/W
Lead Inductance, Self	$L_{11}$	Corner lead	2.0	nH
		Center lead	1.6	
Lead Inductance, Mutual	$L_{12}$	Any lead to any adjacent lead	0.4	nH
Lead Capacitance, Bulk	$C_{11}$	Any lead to $V_{SS}$	0.27	pF

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## 5.0 Ordering Information

ORDERING CODE	DEVICE NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
11640-828	FS6282-03	8-pin (0.150") SOIC (Small Outline Package)	0° C to 70° C (Commercial)	Tape and Reel
11640-838	FS6282-03	8-pin (0.150") SOIC (Small Outline Package)	0° C to 70° C (Commercial)	Tubes

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