

Features :

- * 65,536 words by 16 bits organization.
- * Fast access time and cycle time.
- * Dual $\overline{\text{WE}}$ Input.
- * Low power dissipation.
- * Read-Modify-Write, $\overline{\text{RAS}}$ -Only Refresh, $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh, Hidden Refresh and Test Mode Capability.
- * 256 refresh cycles per 4ms.
- * Available in 40-pin 400 mil SOJ, and 40/44 pin TSOP (II).
- * Single 5.0V \pm 10% Power Supply.
- * All inputs and Outputs are TTL compatible. * Fast Page Mode operation.

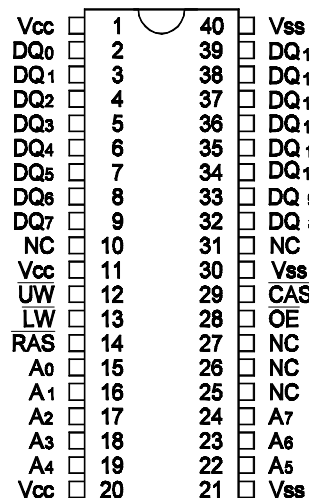
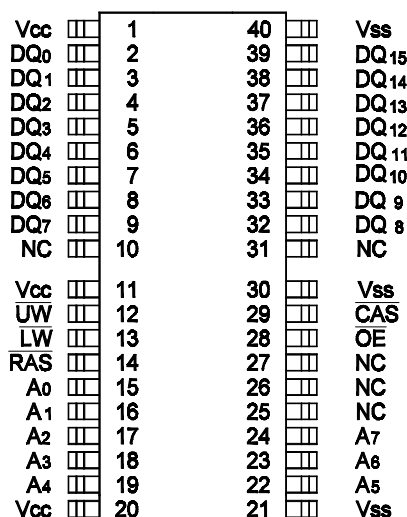
Description :

The GLT41316 is a 65,536 x 16 bit high-performance CMOS dynamic random access memory. The GLT41316 offers Fast Page mode, and has both BYTE WRITE and WORD WRITE access cycles via two $\overline{\text{WE}}$ pins. The GLT41316 has symmetric address and accepts 256-cycle refresh in 4ms interval.

All inputs are TTL compatible. Fast Page Mode operation allows random access up to 256x16 bits, within a page, with cycle times as short as 18ns.

The GLT41316 is best suited for graphics, and DSP applications requiring high performance memories.

HIGH PERFORMANCE	30	35	40	45
Max. $\overline{\text{RAS}}$ Access Time, (t_{RAC})	30 ns	35 ns	40 ns	45 ns
Max. Column Address Access Time, (t_{AA})	15 ns	18 ns	20 ns	22 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	18 ns	21 ns	23 ns	25 ns
Min. Read/Write Cycle Time, (t_{RC})	65 ns	70 ns	75 ns	80 ns
Max. $\overline{\text{CAS}}$ Access Time (t_{CAC})	10 ns	11 ns	12 ns	12 ns

Pin Configuration :
**GLT41316
SOJ Top View**

**TSOP(Type II)
Top View**

Pin Descriptions:

Name	Function
A ₀ - A ₇	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{UW}}$	Read / Upper Byte Write Enable
$\overline{\text{LW}}$	Read / Lower Byte Write Enable
$\overline{\text{OE}}$	Output Enable
DQ ₀ - DQ ₁₅	Data Inputs / Outputs
V _{CC}	+5V Power Supply
V _{SS}	Ground
NC	No Connection

Absolute Maximum Ratings*

Operating Temperature, T_A (ambient)
-0°C to +70°C
 Storage Temperature(plastic)....-55°C to +150°C
 Voltage Relative to V_{SS}-1.0V to + 7.0V
 Short Circuit Output Current.....50mA
 Power Dissipation.....1.0W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

$T_A=25^{\circ}\text{C}$, $V_{CC}=5\text{V}\pm 10\%$, $V_{SS}=0\text{V}$

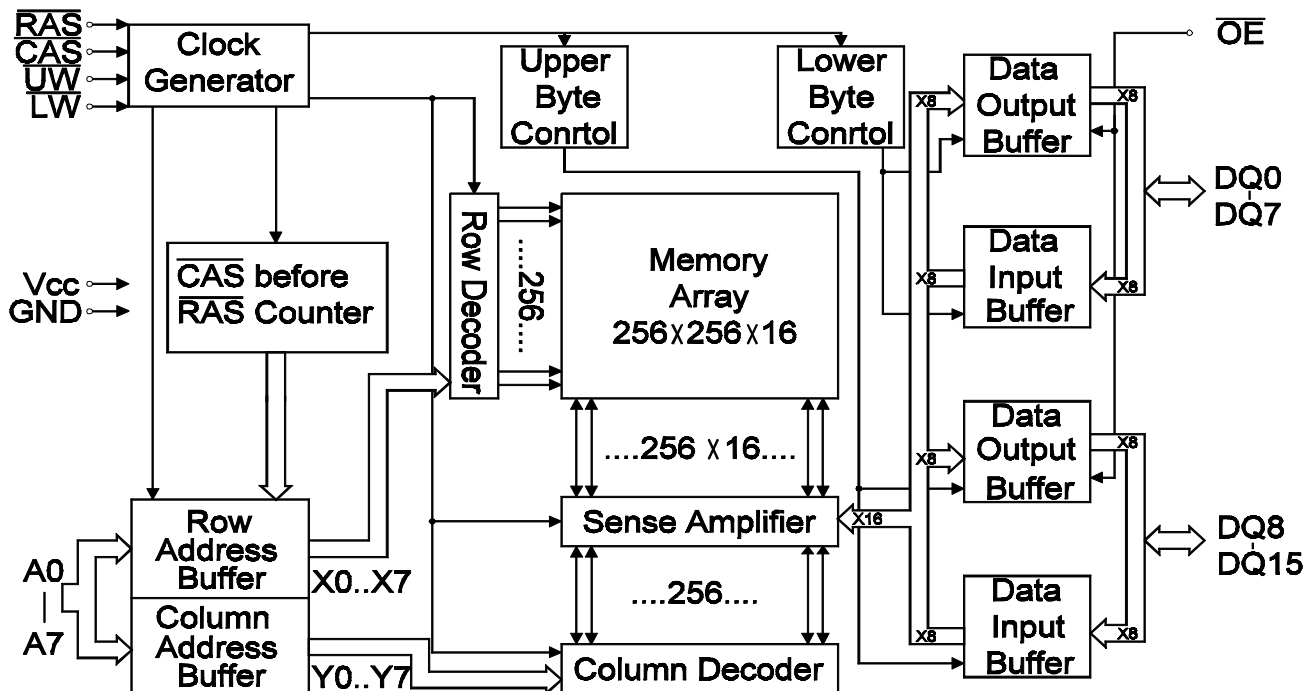
Symbol	Parameter	Max.	Unit
C_{IN1}	Address Input	5	pF
C_{IN2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{UW}}$, $\overline{\text{LW}}$, $\overline{\text{OE}}$	7	pF
C_{OUT}	Data Input/Output	7	pF

*Note: Capacitance is sampled and not 100% tested

Electrical Specifications

- $\overline{\text{WE}}$ means $\overline{\text{UW}}$ and $\overline{\text{LW}}$.
- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ -only refresh cycles as dummy cycles to initialize internal circuit.

Block Diagram :



Truth Table: GLT41316

Function		RAS	CAS	\overline{UW}	\overline{LW}	\overline{OE}	ADDRESS	DQs	Notes
Standby		H	H→X	X	X	X		High-Z	
Read: Word		L	L	H	H	L	ROW/COL	Data Out	
Write: Word(Early Write)		L	L	L	L	X	ROW/COL	Data-In	
Write: Lower Byte (Early)		L	L	H	L	X	ROW/COL	Lower Byte,Data-In Upper Byte,High-Z	
Write: Upper Byte (Early)		L	L	L	H	X	ROW/COL	Lower Byte,High-Z Upper Byte,Data-In	
Read Write		L	L	H→L	H→L	L→H	ROW/COL	Data-Out,Data-In	1,2
Fast-Page- Mode Read	1st Cycle	L	H→L	H	H	L	ROW/COL	Data-Out	1
	2nd Cycle	L	H→L		H	L	COL	Data-Out	1
Fast-Page- Mode Write	1st Cycle	L	H→L	L	L	X	ROW/COL	Data-In	2
	2nd Cycle	L	H→L	L	L	X	COL	Data-In	2
Fast-Page- Mode Read- Write	1st Cycle	L	H→L	H→L	H→L	L→H	ROW/COL	Data-Out,Data-In	1,2
	2nd Cycle	L	H→L	H→L	H→L	L→H	COL	Data-Out,Data-In	1,2
Hidden Refresh	Read	L→H→L	L	H	H	L	ROW/COL	Data-Out	1
	Write	L→H→L	L	L	L	X	ROW/COL	Data-In	2,3
\overline{RAS} -Only Refresh		L	H	X	X	X	ROW	High-Z	
CBR Refresh		H→L	L	X	X	X		High-Z	

Notes:

1. These READ cycles are always WORD READ cycles .
2. These WRITE cycles may also be BYTE READ cycles (either \overline{UW} or \overline{LW} active).
3. EARLY WRITE only.

DC and Operating Characteristics (1-2)
 $T_A = 0^{\circ}\text{C to } 70^{\circ}\text{C}$, $V_{CC}=5\text{V}\pm 10\%$, $V_{SS}=0\text{V}$, unless otherwise specified.

Sym.	Parameter	Test Conditions	Access Time	Min.	Typ	Max.	Unit	Notes
I_{LI}	Input Leakage Current (any input pin)	$0\text{V} \leq V_{IN} \leq 5.5\text{V}$ (All other pins not under test=0V)		-10		+10	μA	
I_{LO}	Output Leakage Current (for High-Z State)	$0\text{V} \leq V_{out} \leq 5.5\text{V}$ Output is disabled (Hiz)		-10		+10	μA	
I_{CC1}	Operating Current, Random READ/WRITE	$t_{RC} = t_{RC}(\text{min.})$	$t_{RAC} = 30\text{ns}$ $t_{RAC} = 35\text{ns}$ $t_{RAC} = 40\text{ns}$ $t_{RAC} = 45\text{ns}$			180 170 160 150	mA	1,2
I_{CC2}	Standby Current,(TTL)	$\overline{\text{RAS}}, \overline{\text{CAS}}$ at V_{IH} other inputs $\geq V_{SS}$				4	mA	
I_{CC3}	Refresh Current, RAS-Only	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ at V_{IH} $t_{RC} = t_{RC}(\text{min.})$	$t_{RAC} = 30\text{ns}$ $t_{RAC} = 35\text{ns}$ $t_{RAC} = 40\text{ns}$ $t_{RAC} = 45\text{ns}$			180 170 160 150	mA	2
I_{CC4}	Operating Current, EDO Page Mode	$\overline{\text{RAS}}$ at V_{IL} , $\overline{\text{CAS}}$, address cycling: $t_{PC} = t_{PC}(\text{min.})$	$t_{RAC} = 30\text{ns}$ $t_{RAC} = 35\text{ns}$ $t_{RAC} = 40\text{ns}$ $t_{RAC} = 45\text{ns}$			180 170 160 150	mA	1,2
I_{CC5}	Refresh Current, CAS Before RAS	$\overline{\text{RAS}}, \overline{\text{CAS}}$, address cycling: $t_{RC} = t_{RC}(\text{min.})$	$t_{RAC} = 30\text{ns}$ $t_{RAC} = 35\text{ns}$ $t_{RAC} = 40\text{ns}$ $t_{RAC} = 45\text{ns}$			180 170 160 150	mA	1
I_{CC6}	Standby Current, (CMOS)	$\overline{\text{RAS}} \geq V_{CC}-0.2\text{V}$, $\overline{\text{CAS}} \geq V_{CC}-0.2\text{V}$, All other inputs $\geq V_{SS}$				2	mA	
V_{IL}	Input Low Voltage			-1		+0.8	V	3
V_{IH}	Input High Voltage			2.4		$V_{CC}+1$	V	3
V_{OL}	Output Low Voltage	$I_{OL} = 4.2\text{mA}$				0.4	V	
V_{OH}	Output High Voltage	$I_{OH} = -5\text{mA}$		2.4			V	

Notes:

- I_{CC} is dependent on output loading when the device output is selected. Specified $I_{CC(\text{max.})}$ is measured with the output open.
- I_{CC} is dependent upon the number of address transitions specified $I_{CC(\text{max.})}$ is measured with a maximum of one transition per address cycle in random Read/Write and Fast Page Mode.
- Specified $V_{IL(\text{min.})}$ is steady state operation. During transitions $V_{IL(\text{min.})}$ may undershoot to -1.0V for a period not to exceed 20ns. All AC parameters are measured with $V_{IL(\text{min.})} \geq V_{SS}$ and $V_{IH(\text{max.})} \leq V_{CC}$.

AC Characteristics (0°C ≤ T_A ≤ 70°C, See note 1,2)

Test condition: V_{CC}=5.0V±10%, V_{IH}/V_{IL}=2.4V/0.8V, V_{OH}/V_{OL}=2.4V/0.4V

Parameter	Symbol	t _{RAC} = 30 ns		t _{RAC} = 35 ns		t _{RAC} = 40 ns		t _{RAC} = 45 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t _{RC}	65	-	70	-	75	-	80	-	ns	
Read Midify Write Cycle Time	t _{RWC}	80	-	99	-	105	-	110	-	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	-	30	-	35	-	40	-	45	ns	3,4
Access Time from $\overline{\text{CAS}}$	t _{CAC}	-	10	-	11	-	12	-	12	ns	3,4
Access Time from Column Address	t _{AA}	-	15	-	18	-	20	-	22	ns	3,4
CAS to Output in Low-Z	t _{CLZ}	0		0	-	0	-	0	-	ns	3
Output Buffer Turn-off Delay from $\overline{\text{CAS}}$	t _{OFF}	3	8	3	8	3	8	3	8	ns	7
Transition Time(Rise and Fall)	t _T	3	50	3	50	3	50	3	50	ns	2
RAS Precharge Time	t _{RP}	25	-	25	-	25	-	25	-	ns	
RAS Pulse Width	t _{RAS}	30	100k	35	100k	40	100K	45	100K	ns	
RAS Hold Time	t _{RSH}	10	-	12	-	12	-	13	-	ns	
CAS Hold Time	t _{CSH}	30	-	36	-	40	-	46	-	ns	
CAS Pulse Width	t _{CAS}	10	10000	12	10000	12	10000	13	10000	ns	
RAS to CAS Delay Time	t _{RCD}	13	20	17	24	18	28	18	33	ns	4
RAS to Column Address Delay Time	t _{RAD}	10	15	12	17	13	20	13	23	ns	4
CAS to RAS Precharge Time	t _{CRP}	5	-	5	-	5	-	5	-	ns	8
Row Address Setup Time	t _{ASR}	0	-	0	-	0	-	0	-	ns	
Row Address Hold Time	t _{RAH}	7	-	7	-	8	-	8	-	ns	
Column Address Setup Time	t _{ASC}	0	-	0	-	0	-	0	-	ns	
Column Address Hold Time	t _{CAH}	6	-	6	-	6	-	6	-	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t _{AR}	26	-	30	-	34	-	39	-	ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t _{RAL}	15	-	18	-	20	-	23	-	ns	
Read Command Setup Time	t _{RCS}	0	-	0	-	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{RRH}	0	-	0	-	0	-	0	-	ns	9
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{RCH}	0	-	0	-	0	-	0	-	ns	9
WE Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	6	-	6	-	6	-	6	-	ns	10
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t _{WCR}	26	-	30	-	34	-	39	-	ns	5
WE Pulse Width	t _{WP}	6	-	6	-	6	-	6	-	ns	10

Parameter	Symbol	t _{RAC} = 30 ns		t _{RAC} = 35 ns		t _{RAC} = 40 ns		t _{RAC} = 45 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	t _{RWL}	10	-	11	-	12	-	12	-	ns	
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{CAS}}$	t _{CWL}	10	-	11	-	12	-	12	-	ns	
Data-In Setup Time	t _{DS}	0	-	0	-	0	-	0	-	ns	11
Data-In Hold Time	t _{DH}	7	-	7	-	8	-	8	-	ns	11
Data Hold Time Referenced to $\overline{\text{RAS}}$	t _{DHR}	27	-	31	-	36	-	41	-	ns	6
$\overline{\text{WE}}$ Setup Time	t _{WCS}	0	-	0	-	0	-	0	-	ns	5
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	47	-	58	-	63	-	68	-	ns	5
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	24	-	29	-	30	-	30	-	ns	5
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	29	-	36	-	38	-	40	-	ns	5
$\overline{\text{CAS}}$ Setup Time($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CSR}	5	-	5	-	5	-	5	-	ns	
$\overline{\text{CAS}}$ Hold Time($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t _{CHR}	10	-	10	-	10	-	10	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	t _{RPC}	5	-	5	-	5	-	5	-	ns	
$\overline{\text{CAS}}$ Precharge Time(CBR Counter Test Cycle)	t _{CPT}	20	-	20	-	20	-	20	-	ns	
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	-	18	-	21	-	23	-	25	ns	3
Fast Page mode Read/Write Cycle Time	t _{PC}	18	-	21	-	23	-	25	-	ns	
Fast Page mode Read Modify Write Cycle Time	t _{PRWC}	48	-	60	-	63	-	65	-	ns	
$\overline{\text{CAS}}$ Precharge Time(Fast Page mode)	t _{CP}	5.5	-	6	-	7	-	7	-	ns	
$\overline{\text{RAS}}$ Pulse Width(Fast Page mode)	t _{RASP}	30	100k	35	100k	40	100K	45	100K	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	25	-	25	-	25	-	30	-	ns	
Access Time from $\overline{\text{OE}}$	t _{OEa}	-	10	-	11	-	12	-	12	ns	
$\overline{\text{OE}}$ to Delay Time	t _{OED}	8	-	8	-	8	-	8	-	ns	
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	t _{OEZ}	3	8	3	8	3	8	3	8	ns	7
$\overline{\text{OE}}$ Hold Time	t _{OEh}	6	-	6	-	7	-	7	-	ns	
$\overline{\text{WE}}$ Hold Time(Hidden Refresh Cycle)	t _{WHR}	15	-	15	-	15	-	15	-	ns	
Refresh Time(256cycles)	t _{REF}	-	4	-	4	-	4	-	4	ms	

Notes

1. An initial pause of 100 μ s is required after power-up followed by any $\overline{\text{RAS}}$ only Refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh cycles to initialize the internal circuit.
2. $V_{IH(min.)}$ and $V_{IL(min.)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min.)}$ and $V_{IL(max.)}$. AC measurements assume $t_T = 3\text{ns}$.
3. Measured with an equivalent to 2 TTL loads and 100pF.
4. For read cycles, the access time is defined as follows:

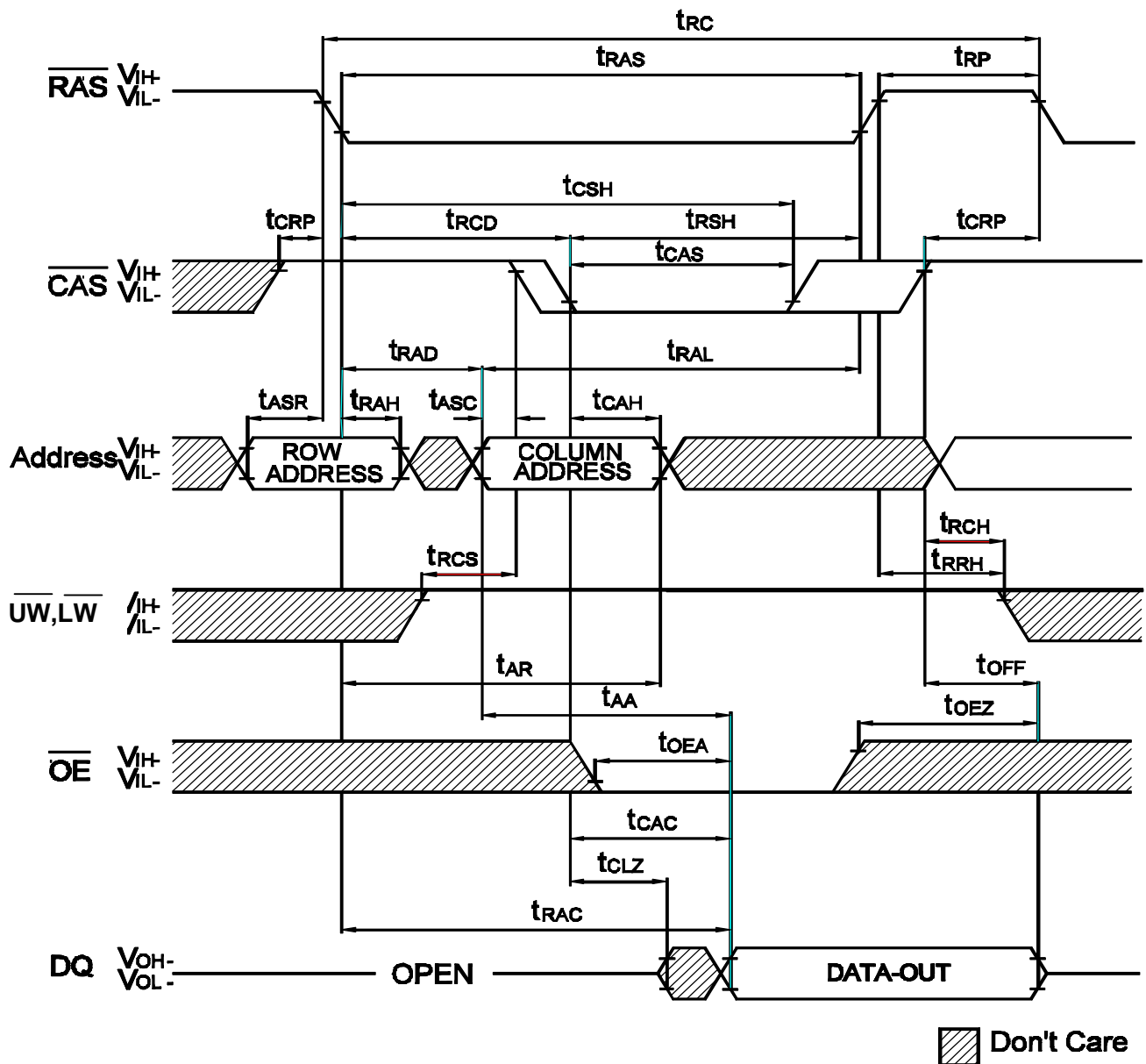
Input Conditions	Access Time
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD(max.)} < t_{RAD}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$
$t_{RCD(max.)} < t_{RCD}$	$t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ indicate the points which the access time changes and are not the limits of operation.

5. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS(min.)}$, the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min.)}$, $t_{RWD} \geq t_{RWD(min.)}$ and $t_{AWD} \geq t_{AWD(min.)}$, then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
6. t_{AR} , t_{WCR} , and t_{DHR} are referenced to $t_{RAD(max.)}$.
7. $t_{OFF(max.)}$ and $t_{OEZ(max.)}$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL} .
8. $t_{CRP(min.)}$ requirement should be applicable for $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycle preceded by any cycles.
9. Either $t_{RCH(min.)}$ or $t_{RRH(min.)}$ must be satisfied for a read cycle.
10. $t_{WP(min.)}$ is applicable for late write cycle or read modify write cycle. In early write cycles, $t_{WCH(min.)}$ should be satisfied.
11. This specification is referenced to $\overline{\text{CAS}}$ falling edge in early write cycles and to $\overline{\text{WE}}$ falling edge in late write or read modify write cycles.

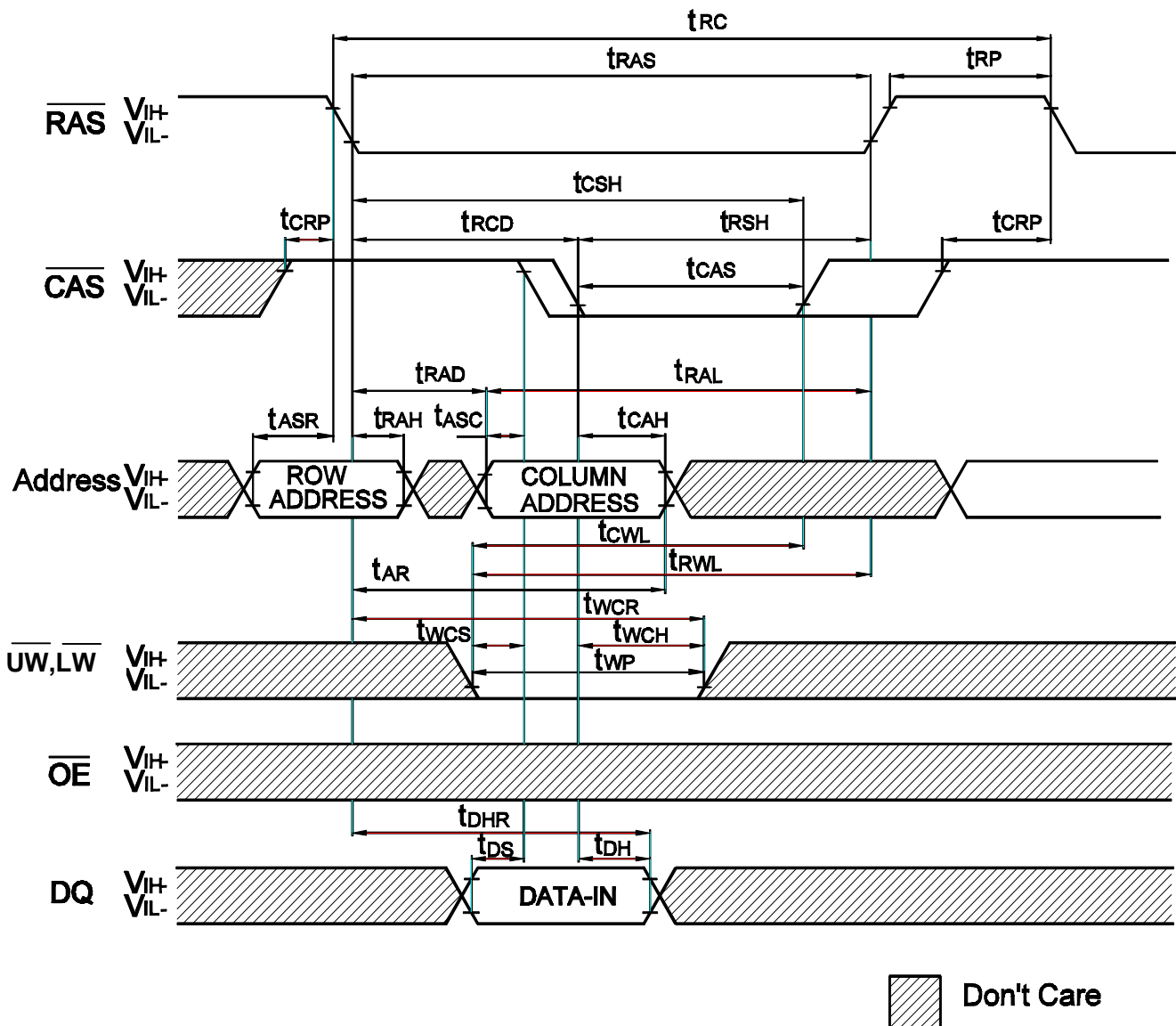
Read Cycle

Note : $D_{IN} = OPEN$



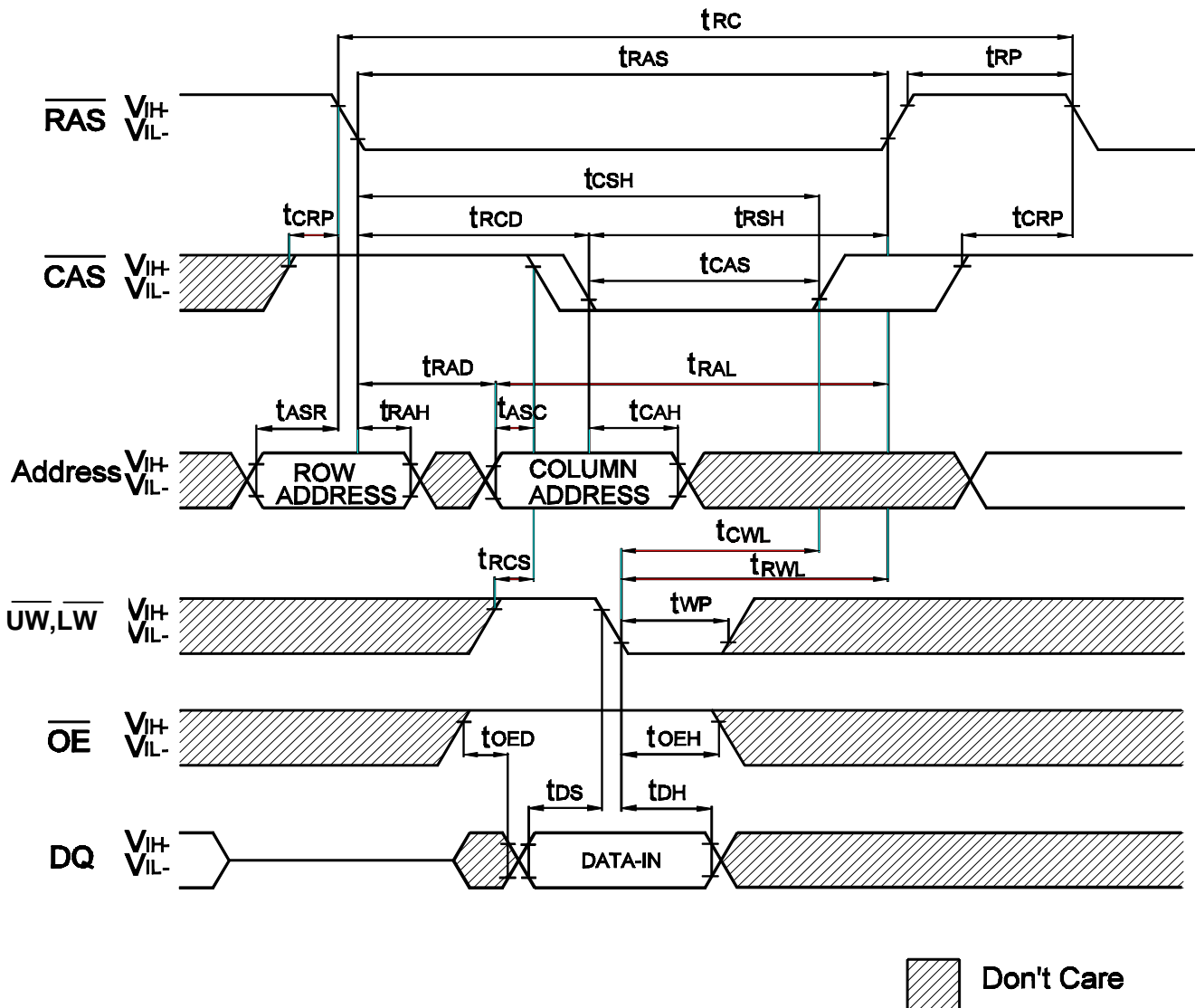
Early Write Cycle

NOTE : D_{OUT} = OPEN

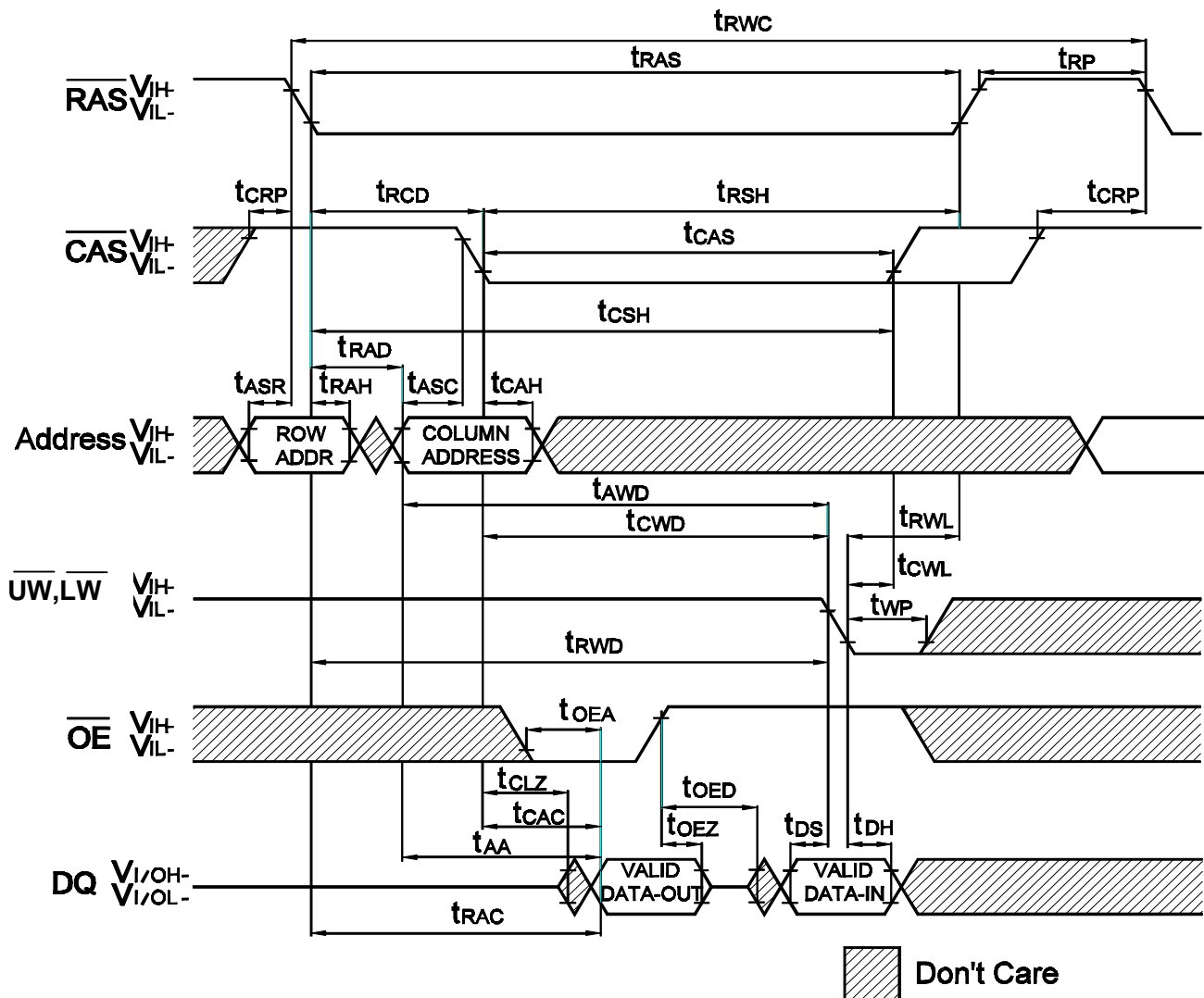


Late Write Cycle (OE Controlled Write)

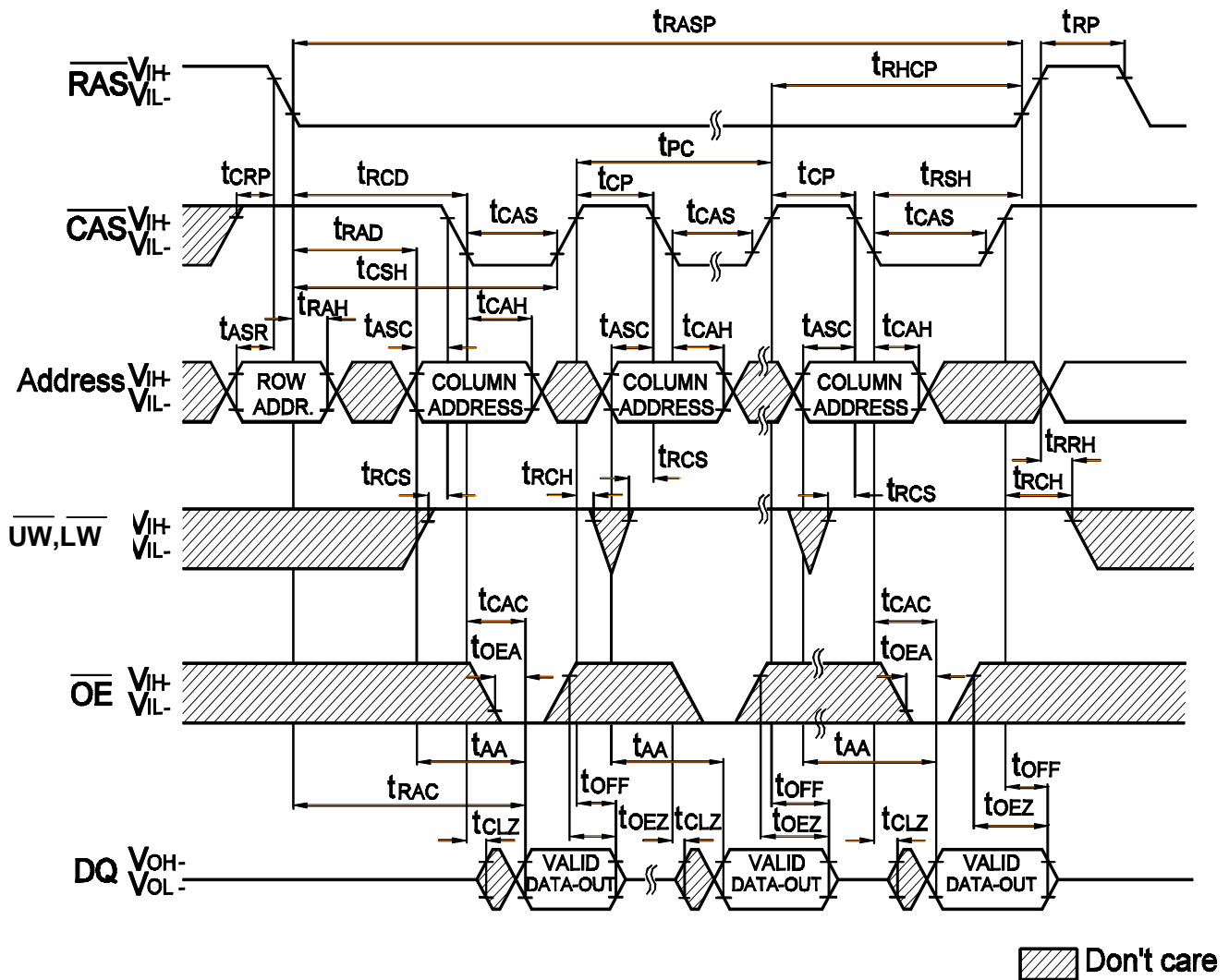
NOET : D_{OUT} = OPEN



Read - Modify - Write Cycle

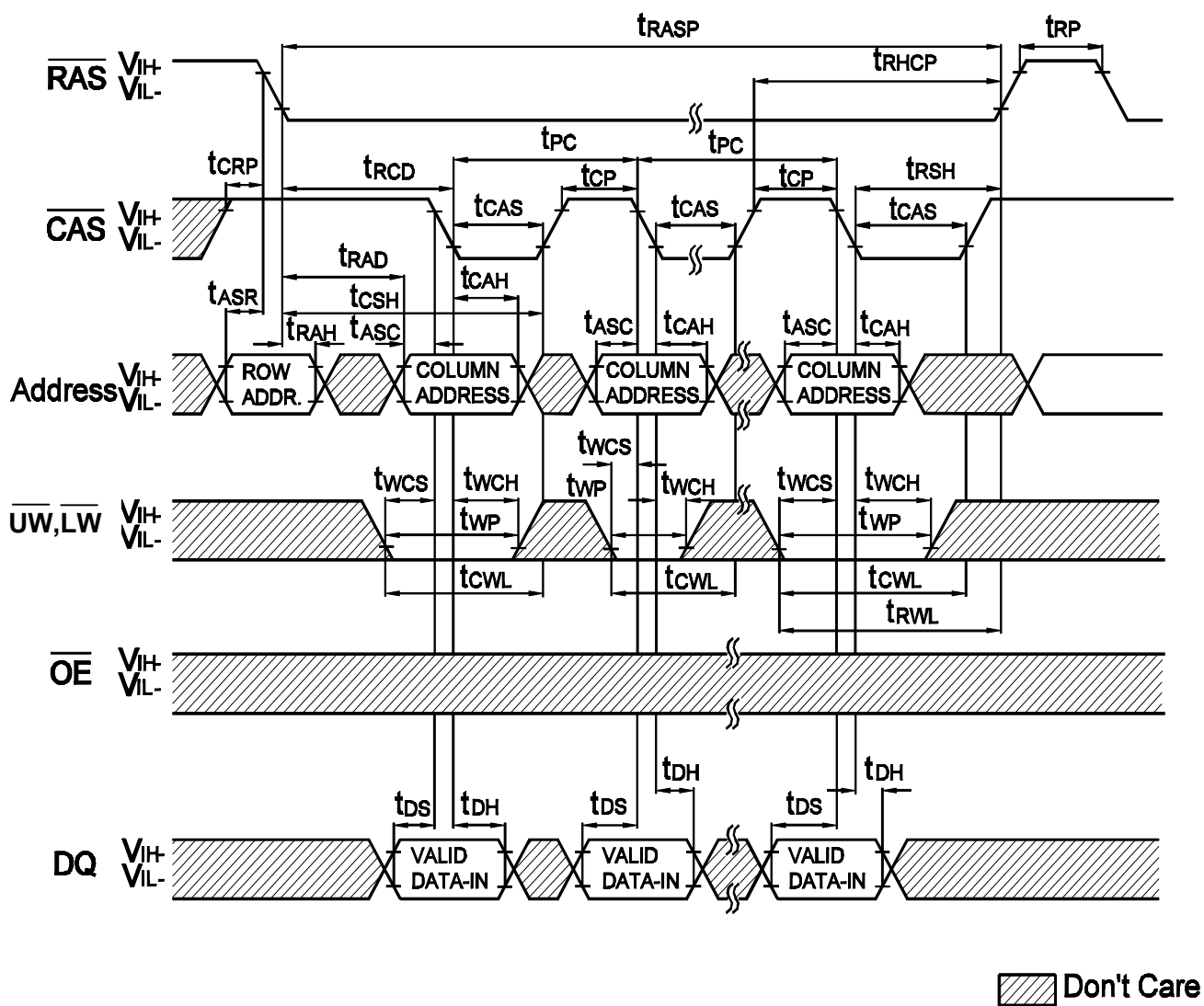


Fast Page Read Cycle



Fast Page Early Write Cycle

NOTE : D_{OUT} = OPEN





The diagram illustrates the timing relationships for a memory device. The signals and their timing parameters are as follows:

- RAS**: V_{IH} to V_{IL} transition. Timing parameters include t_{RASP} (RAS pulse width), t_{CRP} (RAS to CAS setup), t_{RSH} (RAS to CAS hold), t_{RAD} (RAS to Address delay), t_{RAH} (RAS to Address hold), t_{RCS} (RAS to Column Address Setup), t_{RWL} (RAS to Row Address Setup), t_{RCS} (RAS to Column Address Setup), t_{RCS} (RAS to Column Address Setup), t_{RCS} (RAS to Column Address Setup).
- CAS**: V_{IH} to V_{IL} transition. Timing parameters include t_{CRP} (CAS to RAS setup), t_{RCD} (CAS to RAS delay), t_{CAS} (CAS pulse width), t_{CP} (CAS to Data Setup), t_{CAH} (CAS to Data Hold), t_{ASC} (CAS to Data Setup), t_{CWL} (CAS to Data Setup), t_{RCS} (CAS to Column Address Setup), t_{RWL} (CAS to Row Address Setup), t_{RCS} (CAS to Column Address Setup), t_{RCS} (CAS to Column Address Setup).
- Address**: V_{IH} to V_{IL} transition. Timing parameters include t_{ASR} (Address Setup), t_{CAH} (Address to Data Hold), t_{ASC} (Address to Data Setup), t_{CWL} (Address to Data Setup), t_{RCS} (Address to Column Address Setup), t_{RWL} (Address to Row Address Setup), t_{RCS} (Address to Column Address Setup), t_{RCS} (Address to Column Address Setup).
- UW, LW**: V_{IH} to V_{IL} transition. Timing parameters include t_{CWL} (UW, LW Setup), t_{RCS} (UW, LW Setup), t_{RWL} (UW, LW Setup), t_{RCS} (UW, LW Setup).
- OE**: V_{IH} to V_{IL} transition. Timing parameters include t_{OE} (OE Setup), t_{DS} (OE to Data Setup), t_{DH} (OE to Data Hold), t_{OE} (OE Setup), t_{DS} (OE to Data Setup), t_{DH} (OE to Data Hold), t_{OE} (OE Setup), t_{DS} (OE to Data Setup), t_{DH} (OE to Data Hold).
- DQ**: V_{IH} to V_{IL} transition. Timing parameters include t_{OE} (DQ Setup), t_{DS} (DQ to Data Setup), t_{DH} (DQ to Data Hold), t_{OE} (DQ Setup), t_{DS} (DQ to Data Setup), t_{DH} (DQ to Data Hold), t_{OE} (DQ Setup), t_{DS} (DQ to Data Setup), t_{DH} (DQ to Data Hold).

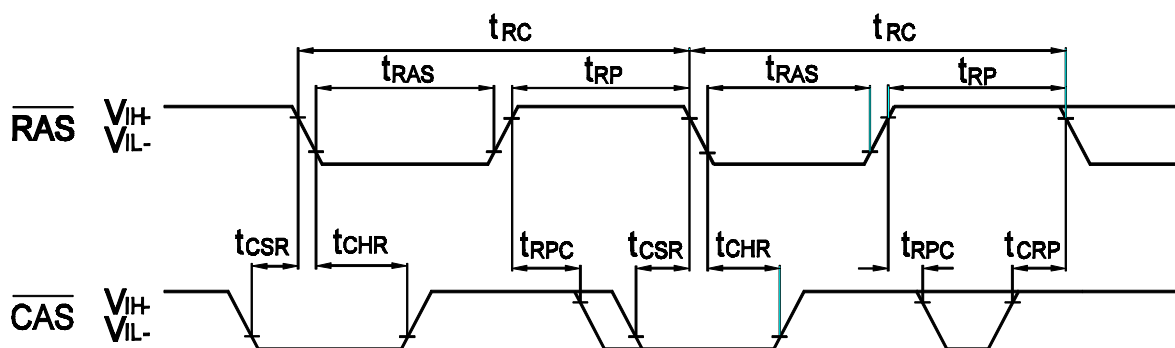


NOTE : D_{OUT} = OPEN



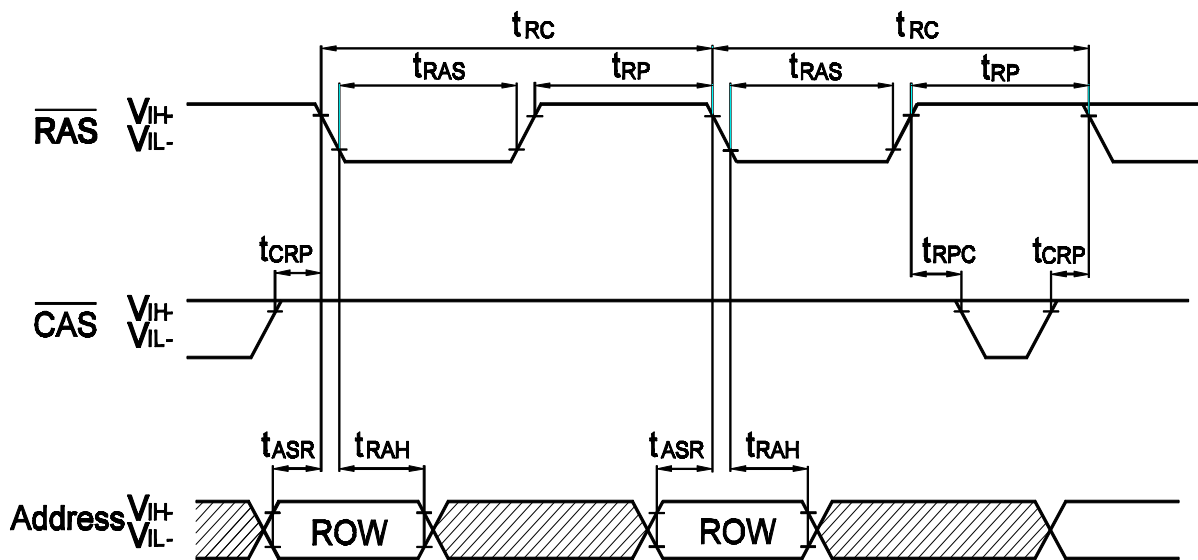
G-Link Technology Corporation, Taiwan
2F, No.12, R&D Rd. II, Science-Based Industrial Park,
Hsin Chu, Taiwan, R.O.C.

CAS Before RAS Refresh Cycle



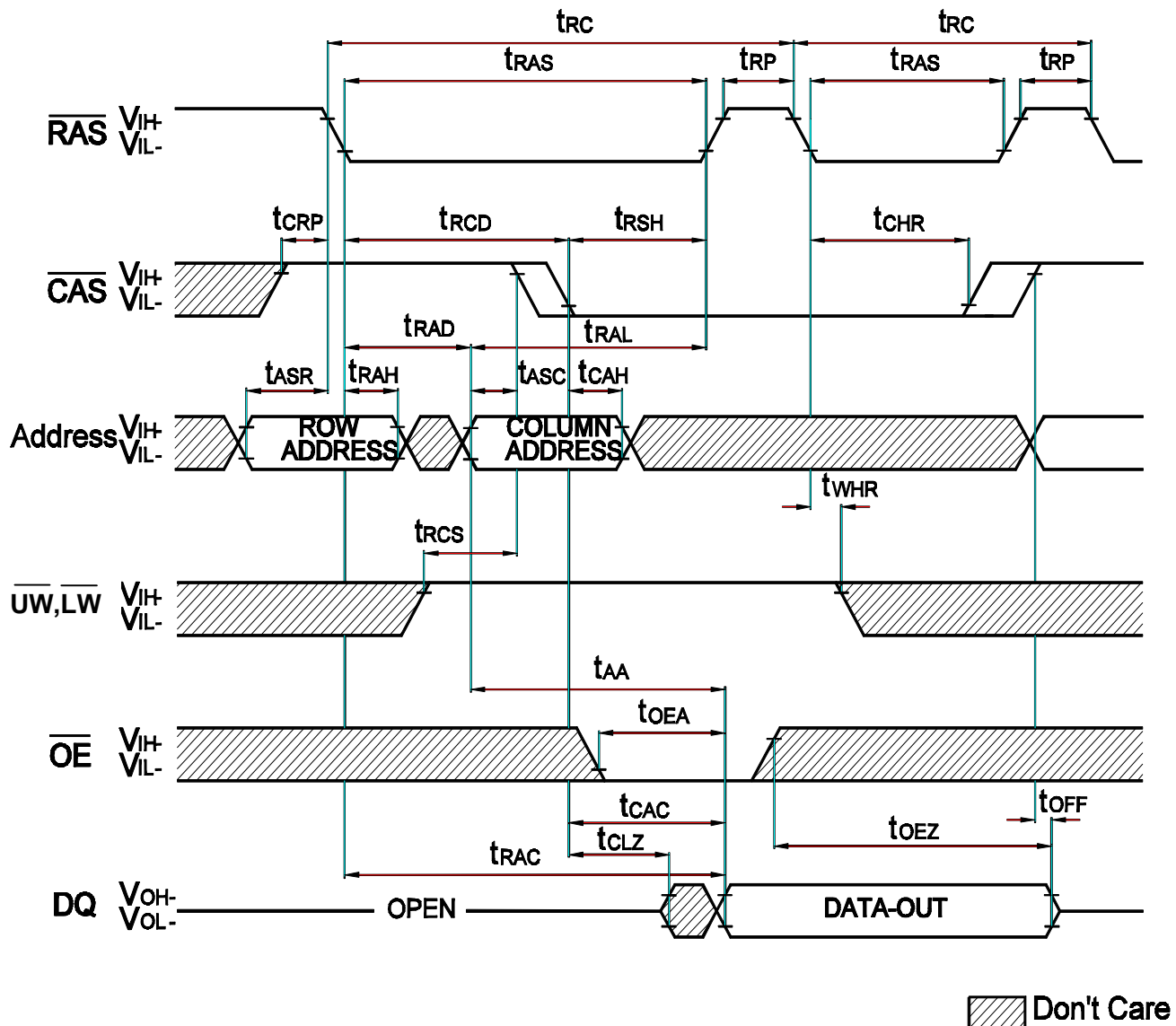
Remark Address, \overline{WE} , \overline{OE} : Don't care DQ : Hi - Z

RAS-Only Refresh Cycle



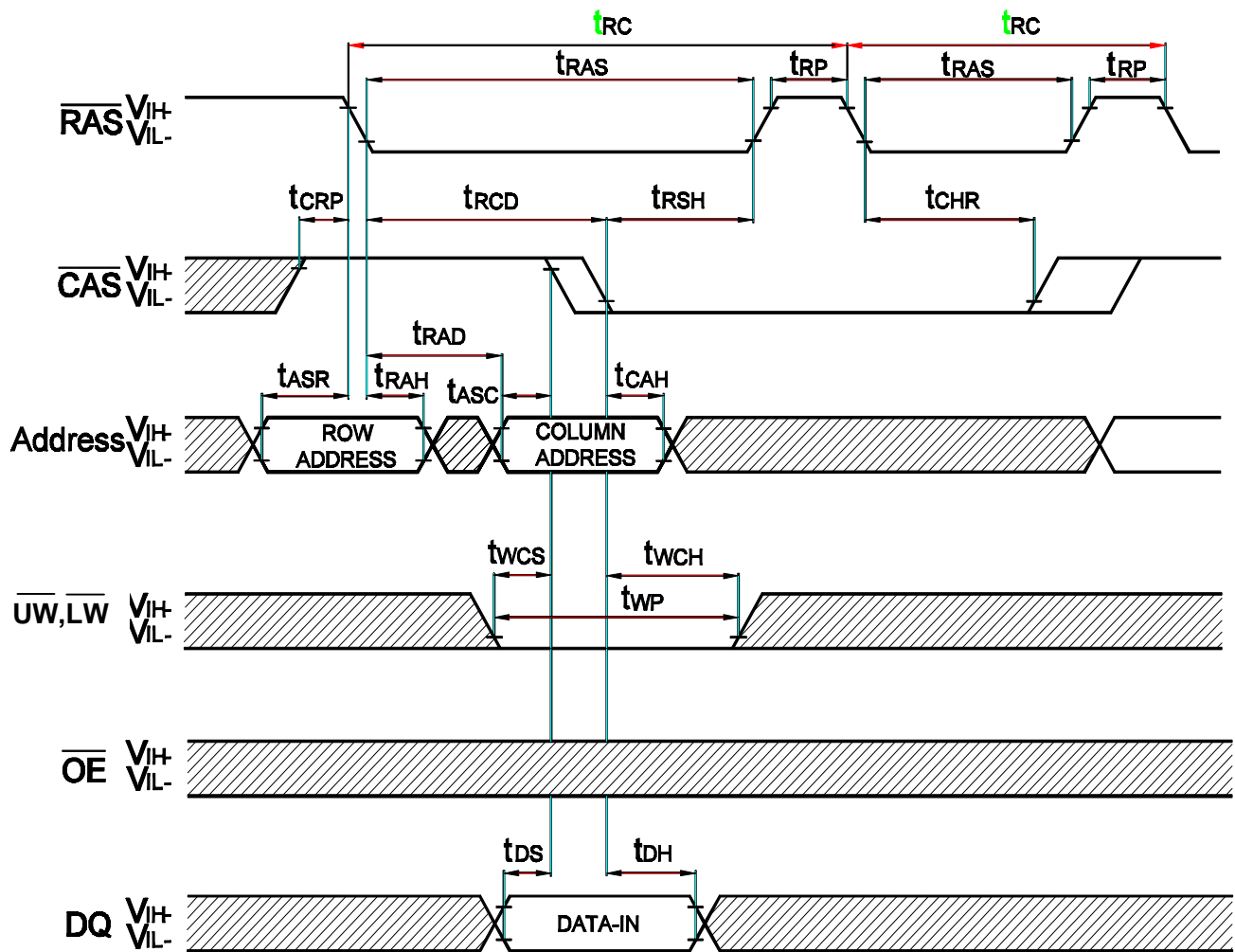
Remark Address, \overline{WE} , \overline{OE} : Don't care DQ : Hi - Z

Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)

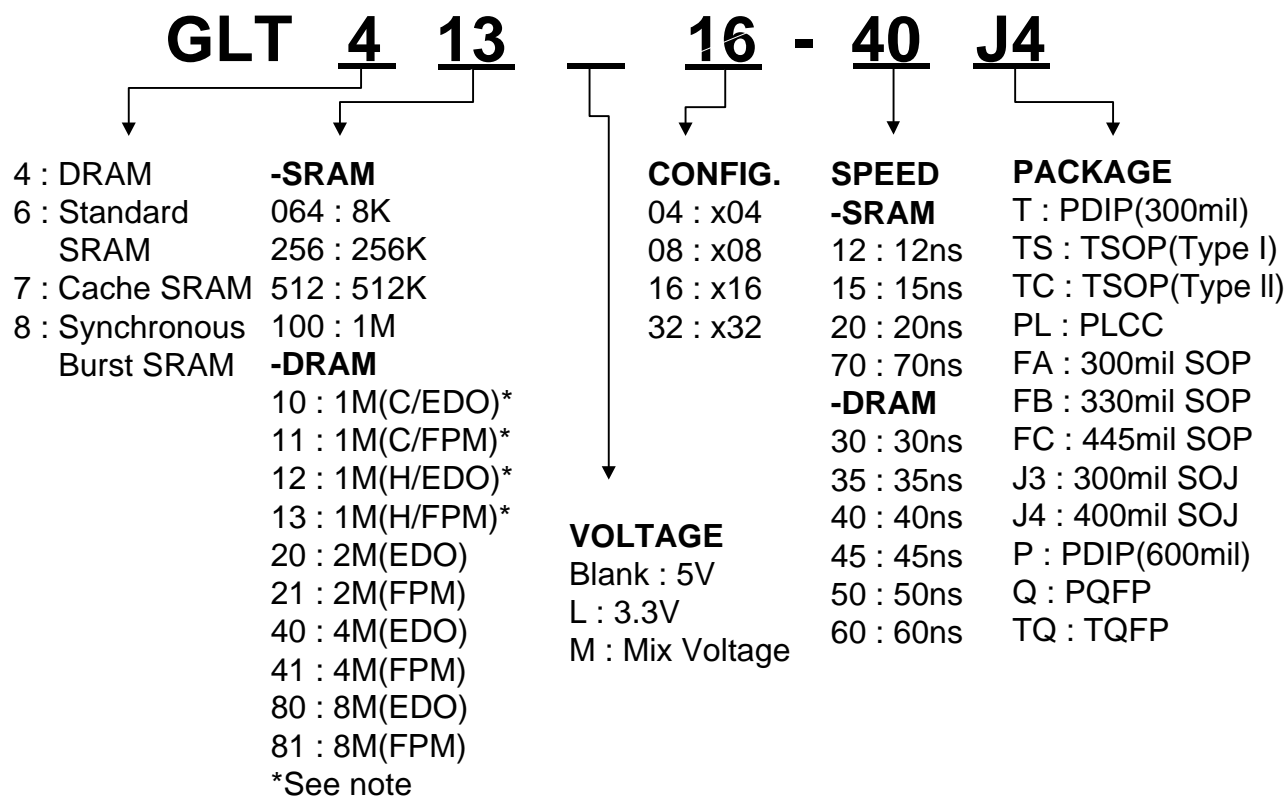
NOTE : D_{OUT} = OPEN



 Don't Care

Ordering Information

<i>Part Number</i>	<i>SPEED</i>	<i>POWER</i>	<i>FEATURE</i>	<i>PACKAGE</i>
GLT41316-30J4	30ns	Normal	FPM	SOJ 400mil 40L
GLT41316-35J4	35ns	Normal	FPM	SOJ 400mil 40L
GLT41316-40J4	40ns	Normal	FPM	SOJ 400mil 40L
GLT41316-45J4	45ns	Normal	FPM	SOJ 400mil 40L
GLT41316-30TC	30ns	Normal	FPM	TSOP 400mil 44L
GLT41316-35TC	35ns	Normal	FPM	TSOP 400mil 44L
GLT41316-40TC	40ns	Normal	FPM	TSOP 400mil 44L
GLT41316-45TC	45ns	Normal	FPM	TSOP 400mil 44L

Parts Numbers (Top Mark) Definition :


Note : C→CDROM , H→HDD.

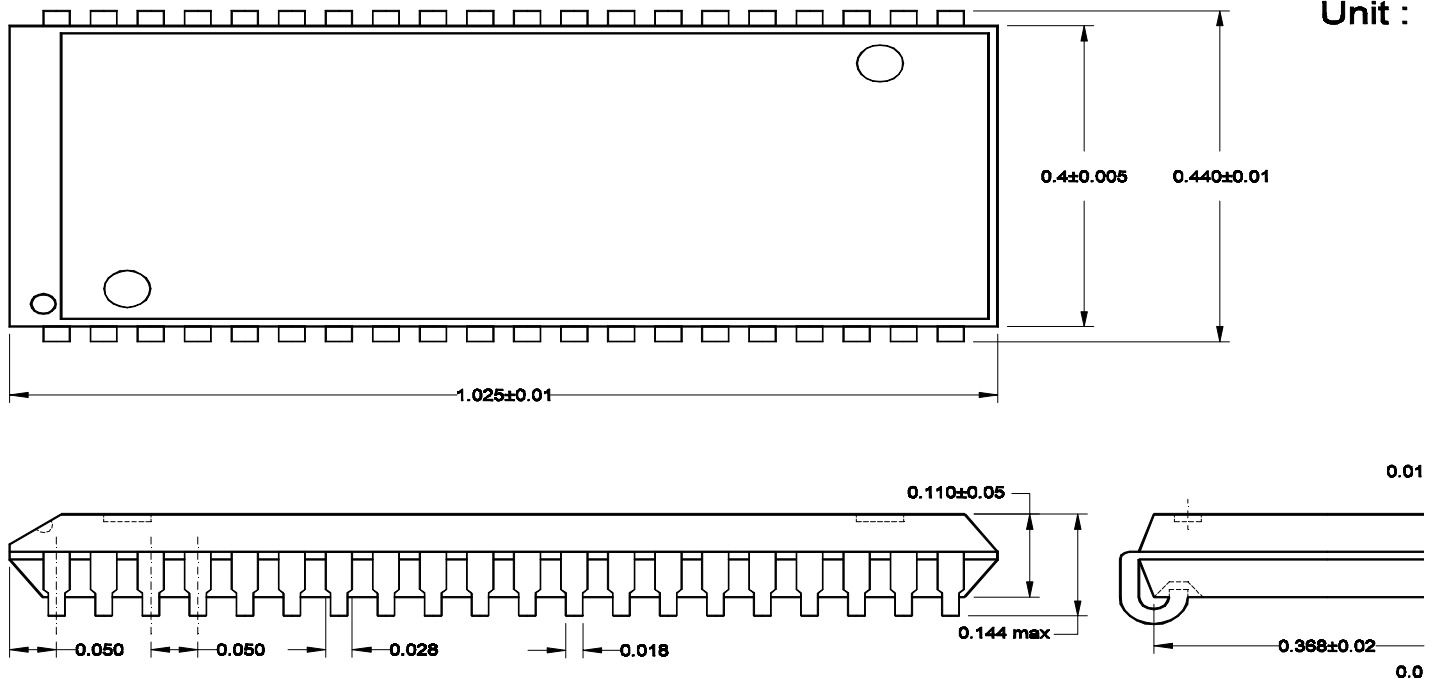
Example :

- 1.GLT710008-15T 1Mbit(128Kx8)15ns 5V SRAM PDIP(300mil)Package type.
- 2.GLT44016-40J4 4Mbit(256Kx16)40ns 5V DRAM SOJ(400mil)Package type.

Package Information

400mil 40 pin Small Outline J-form Package (SOJ)

Unit :



40/44 Lead Thin Small Outline Package TSOP(Type II)

