

## Features :

- \* 524,288 words by 8 bits organization.
- \* Fast access time and cycle time.
- \* Low power dissipation.  
Operating Current-150mA max.  
TTL Standby Current-2mA max.
- \* Read-Modify-Write,  $\overline{\text{RAS}}$ -Only Refresh,  $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  Refresh, Hidden Refresh and Test Mode Capability.
- \* 1024 refresh cycles/16ms.
- \* Available in 28pin 400 mil SOJ
- \* Single +5.0V $\pm$ 10% Power Supply.
- \* All inputs and Outputs are TTL-compatible.
- \* Fast Page Mode supports sustained data rates up to 50MHZ.

## Description :

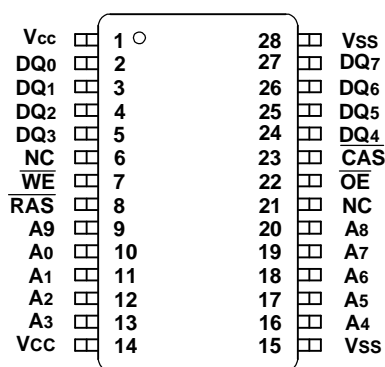
The GLT44108 is a 524,288 x 8 bit high-performance CMOS dynamic random access memory. The GLT44108 offers Fast Page mode with asymmetric address and accepts 512-cycle refresh in 8ms interval.

All inputs are TTL compatible. Fast Page Mode operation allows random access up to 512 x 8 bits within a page, with cycle times as short as 22ns.

The GLT44108 is best suited for graphics, digital signal processing and high performance peripherals.

## PIN CONFIGURATION :

**GLT44108**  
**28 Lead SOJ**

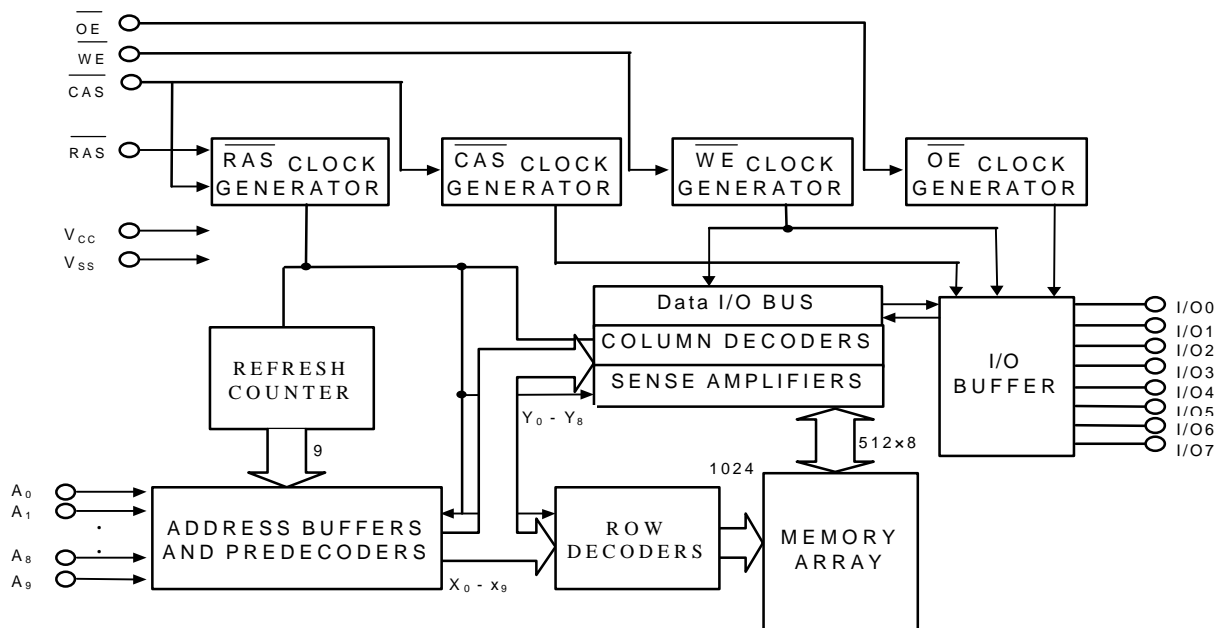


HIGH PERFORMANCE	-40	-50	-60
Max. RAS Access Time, ( $t_{RAC}$ )	40 ns	50 ns	60 ns
Max. Column Address Access Time, ( $t_{AA}$ )	20 ns	25 ns	30 ns
Min. Fast Page Mode Cycle Time, ( $t_{PC}$ )	22 ns	31 ns	40 ns
Min. Read/Write Cycle Time, ( $t_{RC}$ )	75 ns	90 ns	110 ns
Max. CAS Access Time ( $t_{CAC}$ )	12 ns	13 ns	15 ns

### Pin Descriptions:

Name	Function
$A_0 - A_9$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$DQ_0 - DQ_7$	Data Inputs / Outputs
$V_{CC}$	+5V Power Supply
$V_{SS}$	Ground

### Block Diagram:



### Absolute Maximum Ratings\*

Operating Temperature,  $T_A$  (ambient)  
 .....-10°C to +80°C  
 Storage Temperature(plastic)....-55°C to +150°C  
 Voltage Relative to  $V_{SS}$ .....-1.0V to + 7.0V  
 Short Circuit Output Current.....50mA  
 Power Dissipation.....1.0W

\*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

### Capacitance\*

$T_A=25^{\circ}\text{C}$ ,  $V_{CC}=5\text{V}\pm 10\%$ ,  $V_{SS}=0\text{V}$

Symbol	Parameter	Max.	Unit
$C_{IN1}$	Address Input	5	pF
$C_{IN2}$	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$	7	pF
$C_{OUT}$	Data Input/Output	7	pF

\*Note: Capacitance is sampled and not 100% tested

### Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 200 $\mu\text{s}$  and then, execute eight  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  or  $\overline{\text{RAS}}$  only refresh cycles as dummy cycles to initialize internal circuit.

### DC and Operating Characteristics (1-2)

TA = 0°C to 70°C, V<sub>CC</sub>=5V±10%, V<sub>SS</sub>=0V, unless otherwise specified.

Sym.	Parameter	Test Conditions	Access Time	Min.	Typ	Max.	Unit	Notes
I <sub>LI</sub>	Input Leakage Current (any input pin)	0V ≤ V <sub>IN</sub> ≤ 5.5V (All other pins not under test=0V)		-10		+10	μA	
I <sub>LO</sub>	Output Leakage Current (for High-Z State)	0V ≤ V <sub>out</sub> ≤ 5.5V Output is disabled (Hiz)		-10		+10	μA	
I <sub>CC1</sub>	Operating Current, Random READ/WRITE	t <sub>RC</sub> = t <sub>RC</sub> (min.)	t <sub>RAC</sub> = 40ns t <sub>RAC</sub> = 50ns t <sub>RAC</sub> = 60ns			150 140 120	mA	1,2
I <sub>CC2</sub>	Standby Current,(TTL)	RAS, CAS, at V <sub>IH</sub> other inputs ≥ V <sub>SS</sub>				2	mA	
I <sub>CC3</sub>	Refresh Current, RAS -Only	RAS cycling, CAS at V <sub>IH</sub> t <sub>RC</sub> = t <sub>RC</sub> (min.)	t <sub>RAC</sub> = 40ns t <sub>RAC</sub> = 50ns t <sub>RAC</sub> = 60ns			150 140 120	mA	2
I <sub>CC4</sub>	Operating Current, FAST Page Mode	RAS at V <sub>IL</sub> , CAS ,address cycling:t <sub>PC</sub> =t <sub>PC</sub> (min.)	t <sub>RAC</sub> = 40ns t <sub>RAC</sub> = 50ns t <sub>RAC</sub> = 60ns			150 140 120	mA	1,2
I <sub>CC5</sub>	Refresh Current, CAS Before RAS	RAS, CAS, address cycling: t <sub>RC</sub> =t <sub>RC</sub> (min.)	t <sub>RAC</sub> = 40ns t <sub>RAC</sub> = 50ns t <sub>RAC</sub> = 60ns			150 140 120	mA	1
I <sub>CC6</sub>	Standby Current, (CMOS)	RAS ≥ V <sub>CC</sub> -0.2V, CAS ≥ V <sub>CC</sub> -0.2V, All other inputs ≥ V <sub>SS</sub>				1	mA	
V <sub>IL</sub>	Input Low Voltage			-1		+0.8	V	3
V <sub>IH</sub>	Input High Voltage			2.4		V <sub>CC</sub> +1	V	3
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 4.2mA				0.4	V	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -5mA		2.4			V	

#### Notes:

- 1.I<sub>CC</sub> is dependent on output loading when the device output is selected. Specified I<sub>CC(max.)</sub> is measured with the output open.
- 2.I<sub>CC</sub> is dependent upon the number of address transitions specified. I<sub>CC(max.)</sub> is measured with a maximum of one transition per address cycle in random Read/Write and Fast Page Mode.
3. Specified V<sub>IL(min.)</sub> is steady state operation. During transitions, V<sub>IL(min.)</sub> may undershoot to -1.0V for a period not to exceed 20ns.All AC parameters are measured with V<sub>IL(min.)</sub>≥V<sub>SS</sub> and V<sub>IH(max.)</sub>≤V<sub>CC</sub>.

### AC Characteristics (0°C ≤ T<sub>A</sub> ≤ 70°C, See note 1,2)

Test condition: V<sub>CC</sub>=5.0V±10%, V<sub>IH</sub>/V<sub>IL</sub>=2.4V/0.8V, V<sub>OH</sub>/V<sub>OL</sub>=2.0V/0.8V

Parameter	Symbol	40 ns		50 ns		60 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t <sub>RC</sub>	75	-	90	-	110	-	ns	
Read Midify Write Cycle Time	t <sub>RWC</sub>	120	-	140	-	160	-	ns	
Access Time from $\overline{\text{RAS}}$	t <sub>RAC</sub>	-	40	-	50	-	60	ns	3,4
Access Time from CAS	t <sub>CAC</sub>	-	12	-	13	-	15	ns	3,4
Access Time from Column Address	t <sub>AA</sub>	-	20	-	25	-	30	ns	3,4
CAS to Output in Low-Z	t <sub>CLZ</sub>	0	-	0	-	0	-	ns	3
Output Buffer Turn-off Delay from $\overline{\text{CAS}}$	t <sub>OFF</sub>	0	8	0	10	0	13	ns	7
Transition Time(Rise and Fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	2
RAS Precharge Time	t <sub>RP</sub>	25	-	30	-	40	-	ns	
RAS Pulse Width	t <sub>RAS</sub>	40	10000	50	10000	60	10000	ns	
RAS Hold Time	t <sub>RSH</sub>	12	-	13	-	15	-	ns	
CAS Hold Time	t <sub>CSH</sub>	40	-	50	-	60	-	ns	
CAS Pulse Width	t <sub>CAS</sub>	12	10000	13	10000	15	10000	ns	
RAS to CAS Delay Time	t <sub>RCD</sub>	16	30	18	37	20	45	ns	4
RAS to Column Address Delay Time	t <sub>RAD</sub>	11	22	13	25	15	30	ns	4
CAS to RAS Precharge Time	t <sub>CRP</sub>	5	-	5	-	5	-	ns	8
Row Address Setup Time	t <sub>ASR</sub>	0	-	0	-	0	-	ns	
Row Address Hold Time	t <sub>RAH</sub>	6	-	8	-	10	-	ns	
Column Address Setup Time	t <sub>ASC</sub>	0	-	0	-	0	-	ns	
Column Address Hold Time	t <sub>CAH</sub>	6	-	8	-	10	-	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t <sub>AR</sub>	30	-	40	-	45	-	ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t <sub>RAL</sub>	20	-	25	-	30	-	ns	
Read Command Setup Time	t <sub>RCS</sub>	0	-	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t <sub>RRH</sub>	0	-	0	-	0	-	ns	9
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t <sub>RCH</sub>	0	-	0	-	0	-	ns	9
WE Hold Time Referenced to $\overline{\text{CAS}}$	t <sub>WCH</sub>	6	-	7	-	10	-	ns	10
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t <sub>WCR</sub>	30	-	40	-	45	-	ns	5

Parameter	Symbol	40 ns		50 ns		60 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
WE Pulse Width	$t_{WP}$	6	-	7	-	10	-	ns	10
WE Lead Time Referenced to RAS	$t_{RWL}$	13	-	17	-	15	-	ns	
WE Lead Time Referenced to CAS	$t_{CWL}$	13	-	14	-	15	-	ns	
Data-In Setup Time	$t_{DS}$	0	-	0	-	0	-	ns	11
Data-In Hold Time	$t_{DH}$	6	-	7	-	10	-	ns	11
Data Hold Time Referenced to RAS	$t_{DHR}$	33	-	40	-	45	-	ns	6
Refresh Time(256cycles)	$t_{REF}$	-	8	-	8	-	8	ms	
WE Setup Time	$t_{WCS}$	0	-	0	-	0	-	ns	5
RAS to WE Delay Time	$t_{RWD}$	60	-	70	-	85	-	ns	5
CAS to WE Delay Time	$t_{CWD}$	28	-	33	-	38	-	ns	5
Column Address to WE Delay Time	$t_{AWD}$	38	-	43	-	53	-	ns	5
CAS Setup Time(CAS before RAS Refresh)	$t_{CSR}$	5	-	5	-	5	-	ns	
CAS Hold Time(CAS before RAS Refresh)	$t_{CHR}$	10	-	10	-	10	-	ns	
RAS to CAS Precharge Time	$t_{RPC}$	5	-	5	-	5	-	ns	
CAS Precharge Time(CBR Counter Test Cycle)	$t_{CPT}$	20	-	20	-	20	-	ns	
Access Time from CAS Precharge	$t_{CPA}$	-	25	-	30	-	35	ns	3
Fast Page mode Read/Write Cycle Time	$t_{PC}$	30	-	35	-	40	-	ns	
Fast Page mode Read Modify Write Cycle Time	$t_{PRWC}$	65	-	80	-	90	-	ns	
CAS Precharge Time(Fast Page mode)	$t_{CP}$	7	-	8	-	10	-	ns	
RAS Pulse Width(Fast Page mode)	$t_{RASP}$	40	125000	50	125000	60	125000	ns	
RAS Hold Time from CAS Precharge	$t_{RHCP}$	25	-	30	-	35	-	ns	
Access Time from OE	$t_{OEA}$	-	10	-	13	-	15	ns	
OE to Delay Time	$t_{OED}$	8	-	10	-	13	-	ns	
Output Buffer Turn-off Delay Time from OE	$t_{OEZ}$	0	8	0	10	0	13	ns	7
OE Hold Time	$t_{OEH}$	0	-	0	-	0	-	ns	
WE Hold Time(Hidden Refresh Cycle)	$t_{WHR}$	15	-	15	-	15	-	ns	

## Notes

1. An initial pause of 200 $\mu$ s is required after power-up followed by any 8  $\overline{\text{RAS}}$  only Refresh or  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  Refresh cycles to initialize the internal circuit.
2.  $V_{IH(min.)}$  and  $V_{IL(min.)}$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH(min.)}$  and  $V_{IL(max.)}$  are assumed to be 5ns for all inputs.
3. Measured with an equivalent to 1 TTL loads and 50pF.
4. For read cycles, the access time is defined as follows:

Input Conditions	Access Time
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD(max.)} < t_{RAD}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$
$t_{RCD(max.)} < t_{RCD}$	$t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$  and  $t_{RCD(MAX.)}$  indicate the points which the access time changes and are not the limits of operation.

5.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If  $t_{WCS} \geq t_{WCS(min.)}$ , the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If  $t_{CWD} \geq t_{CWD(min.)}$ ,  $t_{RWD} \geq t_{RWD(min.)}$  and  $t_{AWD} \geq t_{AWD(min.)}$ , then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
6.  $t_{AR}$ ,  $t_{WCR}$ , and  $t_{DHR}$  are referenced to  $t_{RAD(max.)}$ .
7.  $t_{OFF(max.)}$  and  $t_{OEZ(max.)}$  define the time at which the output achieves the open circuit condition and are not referenced to  $V_{OH}$  or  $V_{OL}$ .
8.  $t_{CRP(min.)}$  requirement should be applicable for  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  cycle preceded by any cycles.
9. Either  $t_{RCH(min.)}$  or  $t_{RRH(min.)}$  must be satisfied for a read cycle.
10.  $t_{WP(min.)}$  is applicable for late write cycle or read modify write cycle. In early write cycles,  $t_{WCH(min.)}$  should be satisfied.
11. This specification is referenced to  $\overline{\text{CAS}}$  falling edge in early write cycles and to  $\overline{\text{WE}}$  falling edge in late write or read modify write cycles.



The diagram illustrates the timing relationships for a 256K1T1 DRAM. The signals shown are RAS, CAS, Address, WE, OE, and DQ. The timing parameters are defined as follows:

- t<sub>CRP</sub>**: RAS precharge time (from VIH to VIL).
- t<sub>CSH</sub>**: CAS setup time (from VIH to VIL).
- t<sub>RSH</sub>**: CAS hold time (from VIL to VIH).
- t<sub>CRP</sub>**: RAS precharge time (from VIH to VIL).
- t<sub>TRH</sub>**: RAS to RAS hold time (from VIH to VIL).
- t<sub>RRH</sub>**: RAS to RAS hold time (from VIL to VIH).
- t<sub>OEZ</sub>**: Output enable to output high impedance time (from VIH to VIL).
- t<sub>OFF</sub>**: Output enable to output high impedance time (from VIL to VIH).
- t<sub>AD</sub>**: Address to data delay (from VIH to VIL).
- t<sub>AH</sub>**: Address to data hold time (from VIL to VIH).
- t<sub>AS</sub>**: Address to data setup time (from VIH to VIL).
- t<sub>CAH</sub>**: Address to data hold time (from VIL to VIH).
- t<sub>RCS</sub>**: RAS to column address delay (from VIH to VIL).
- t<sub>AR</sub>**: RAS to row address delay (from VIH to VIL).
- t<sub>AA</sub>**: RAS to row address delay (from VIL to VIH).
- t<sub>OEA</sub>**: Output enable to output high impedance time (from VIH to VIL).
- t<sub>CAC</sub>**: Column address to data delay (from VIH to VIL).
- t<sub>CLZ</sub>**: Column address to data delay (from VIL to VIH).
- t<sub>TRC</sub>**: Row to row delay (from VIH to VIL).
- t<sub>TRP</sub>**: Row to row delay (from VIL to VIH).
- t<sub>TRH</sub>**: Row to row hold time (from VIH to VIL).
- t<sub>RRH</sub>**: Row to row hold time (from VIL to VIH).
- t<sub>OEZ</sub>**: Output enable to output high impedance time (from VIH to VIL).
- t<sub>OFF</sub>**: Output enable to output high impedance time (from VIL to VIH).
- t<sub>Voh</sub>**: Output voltage high time (from VIH to VIL).
- t<sub>Vol</sub>**: Output voltage low time (from VIL to VIH).

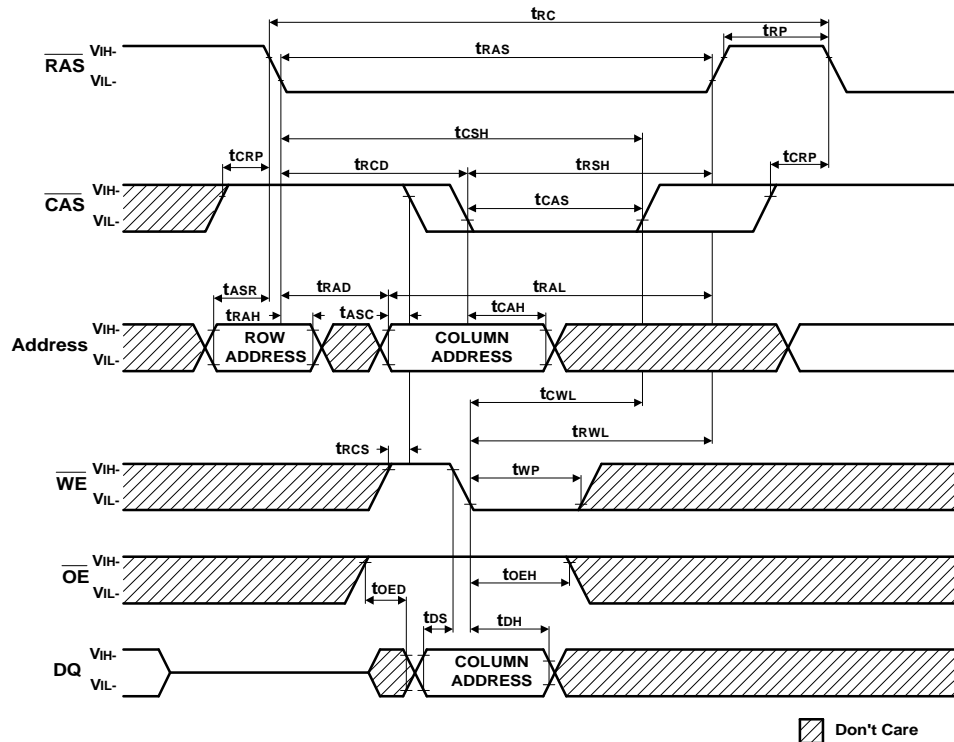
The diagram illustrates the timing relationships for the 16M1602 LCD module. The signals and their timing parameters are as follows:

- RAS**: Row Address Strobe. Timing parameters:  $t_{RC}$  (total pulse width),  $t_{RAS}$  (pulse width),  $t_{RPH}$  (pulse height).
- CAS**: Column Address Strobe. Timing parameters:  $t_{CRP}$  (pulse width),  $t_{CSD}$  (pulse width),  $t_{RSH}$  (pulse height),  $t_{CAS}$  (pulse width).
- Address**: Data bus for Row and Column addresses. Timing parameters:  $t_{ASR}$  (Row Address Setup),  $t_{RAH}$  (Row Address Hold),  $t_{ASC}$  (Column Address Setup),  $t_{CAH}$  (Column Address Hold),  $t_{AL}$  (Address Latency).
- WE**: Write Enable. Timing parameters:  $t_{WCR}$  (Write Enable Setup),  $t_{WCH}$  (Write Enable Hold),  $t_{WP}$  (Write Enable Pulse Width).
- OE**: Output Enable. Timing parameters:  $t_{DHR}$  (Output Enable Setup),  $t_{DS}$  (Output Enable Hold),  $t_{DH}$  (Output Enable Pulse Width).
- DQ**: Data bus. Timing parameters:  $t_{DHR}$  (Data Setup),  $t_{DS}$  (Data Hold),  $t_{DH}$  (Data Pulse Width).

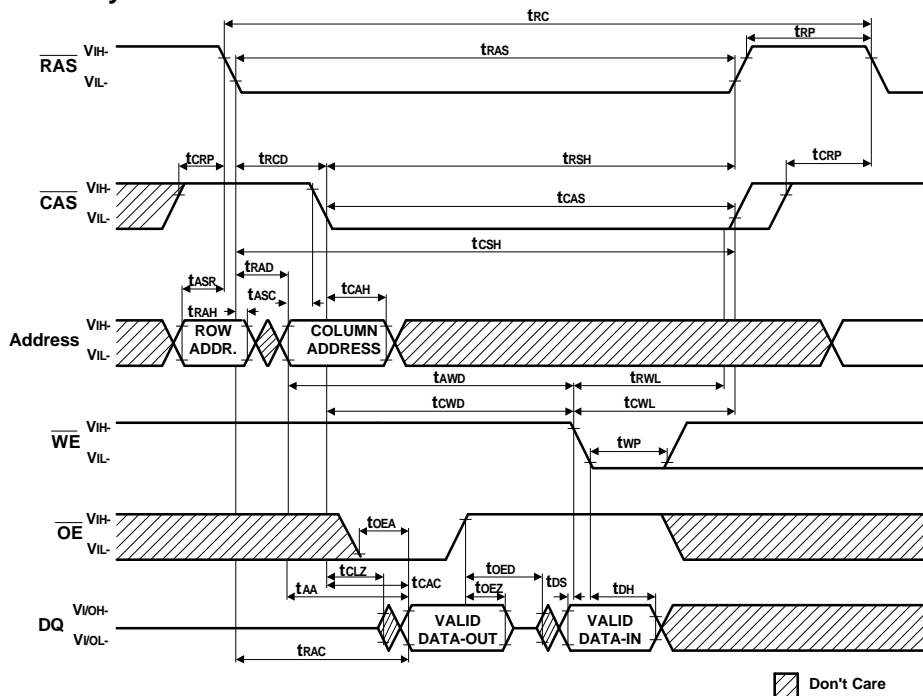
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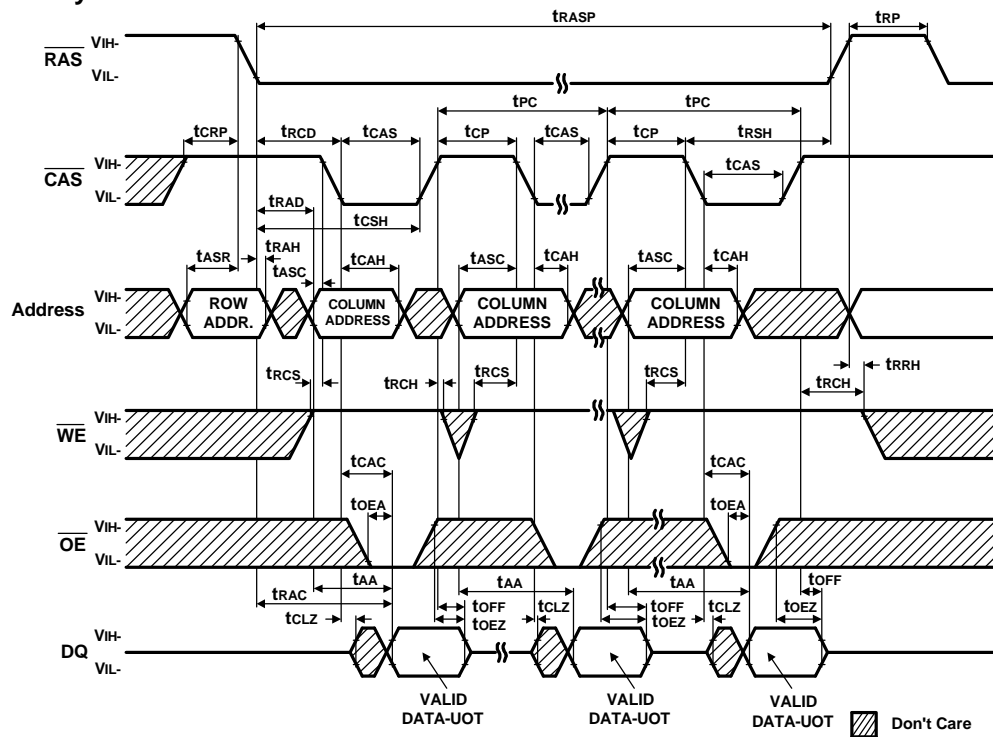
**Late Write Cycle (OE Controlled Write) NOTE : D<sub>OUT</sub> = Open**



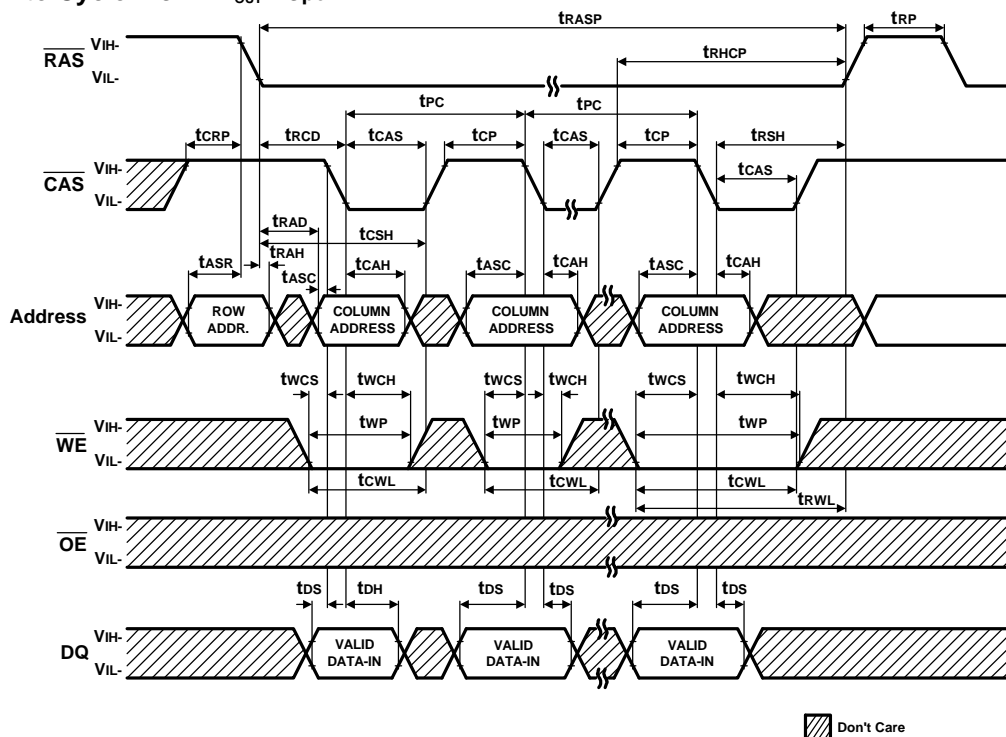
**Read - Modify - Write Cycle**



### Fast Page Read Cycle



### Fast Page Write Cycle NOTE : $D_{OUT} = \text{Open}$





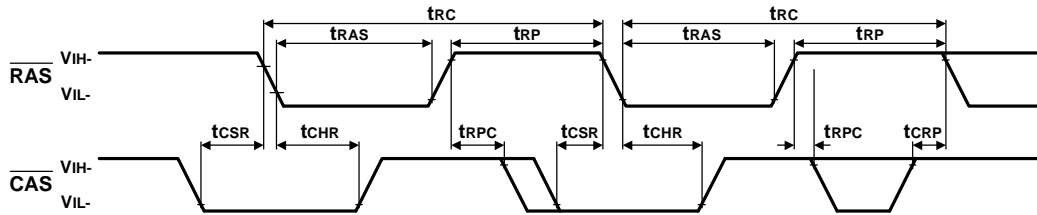
The timing diagram illustrates the relationship between the RAS, CAS, Address, WE, OE, and DQ signals. The signals are shown as waveforms with various timing parameters labeled. The Address signal is shown as a sequence of Row Address (ROW ADDR.) and Column Address (COLUMN ADDRESS) signals. The WE signal is shown as a pulse. The OE signal is shown as a pulse. The DQ signal is shown as a sequence of Hi-Z, VALID DATA-IN, and Hi-Z states. The timing parameters are defined as follows:

- $t_{RSP}$ : RAS setup time before CAS
- $t_{RHP}$ : RAS hold time after CAS
- $t_{RP}$ : RAS pulse width
- $t_{CSH}$ : CAS setup time before Address
- $t_{PC}$ : CAS pulse width
- $t_{CRP}$ : CAS setup time before Address
- $t_{RSH}$ : RAS hold time after Address
- $t_{CRP}$ : CAS setup time before Address
- $t_{ASR}$ : Address setup time before WE
- $t_{RAH}$ : Address hold time after WE
- $t_{ASC}$ : Address setup time before OE
- $t_{CAH}$ : Address hold time after OE
- $t_{RCS}$ : RAS setup time before WE
- $t_{CWL}$ : RAS pulse width
- $t_{RWP}$ : RAS pulse width
- $t_{RWH}$ : RAS hold time after WE
- $t_{OEH}$ : OE setup time before WE
- $t_{OED}$ : OE setup time before WE
- $t_{DS}$ : DQ setup time before WE
- $t_{DH}$ : DQ hold time after WE
- $t_{RCS}$ : RAS setup time before WE
- $t_{CWL}$ : RAS pulse width
- $t_{RWP}$ : RAS pulse width
- $t_{RWH}$ : RAS hold time after WE
- $t_{OEH}$ : OE setup time before WE
- $t_{OED}$ : OE setup time before WE
- $t_{DS}$ : DQ setup time before WE
- $t_{DH}$ : DQ hold time after WE

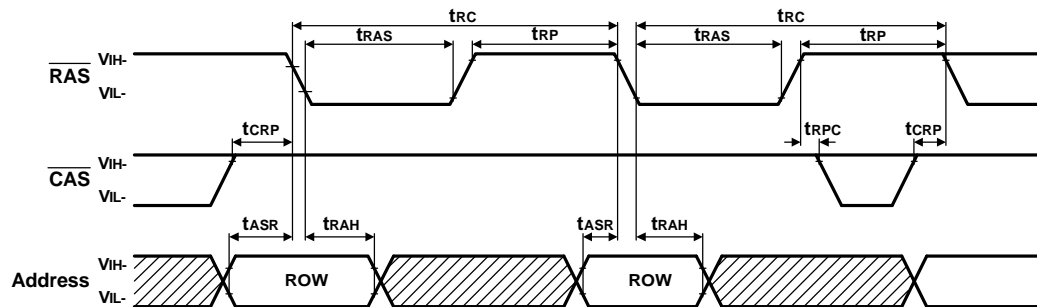
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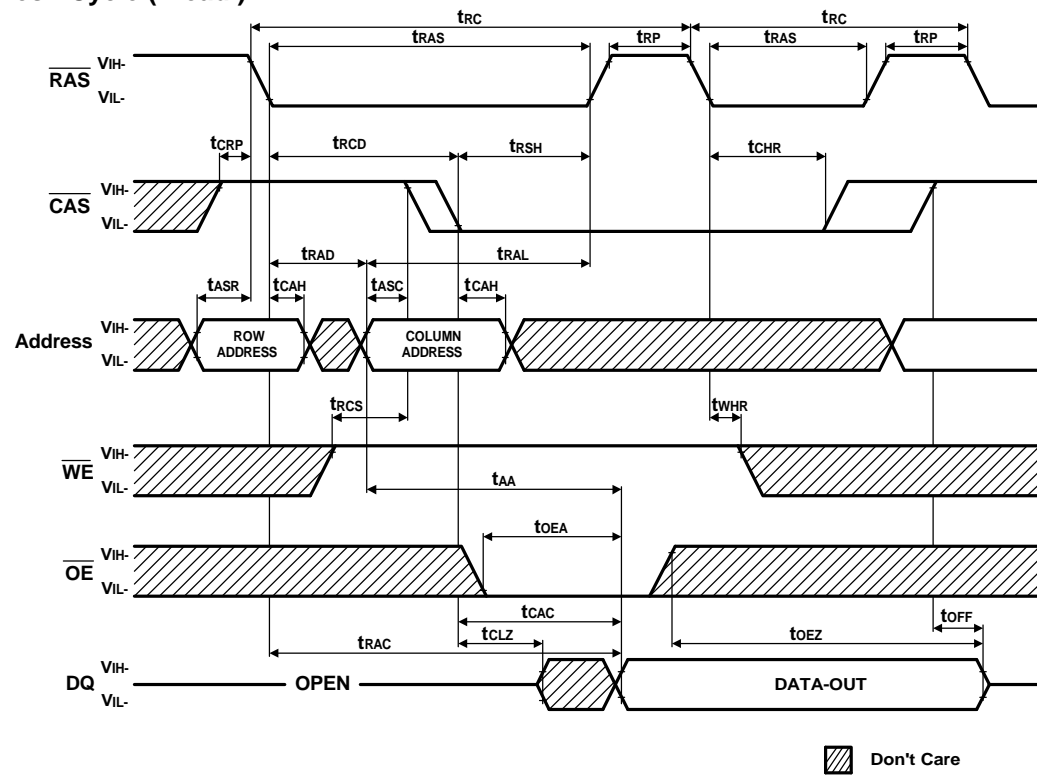
**CAS Before RAS Refresh Cycle**



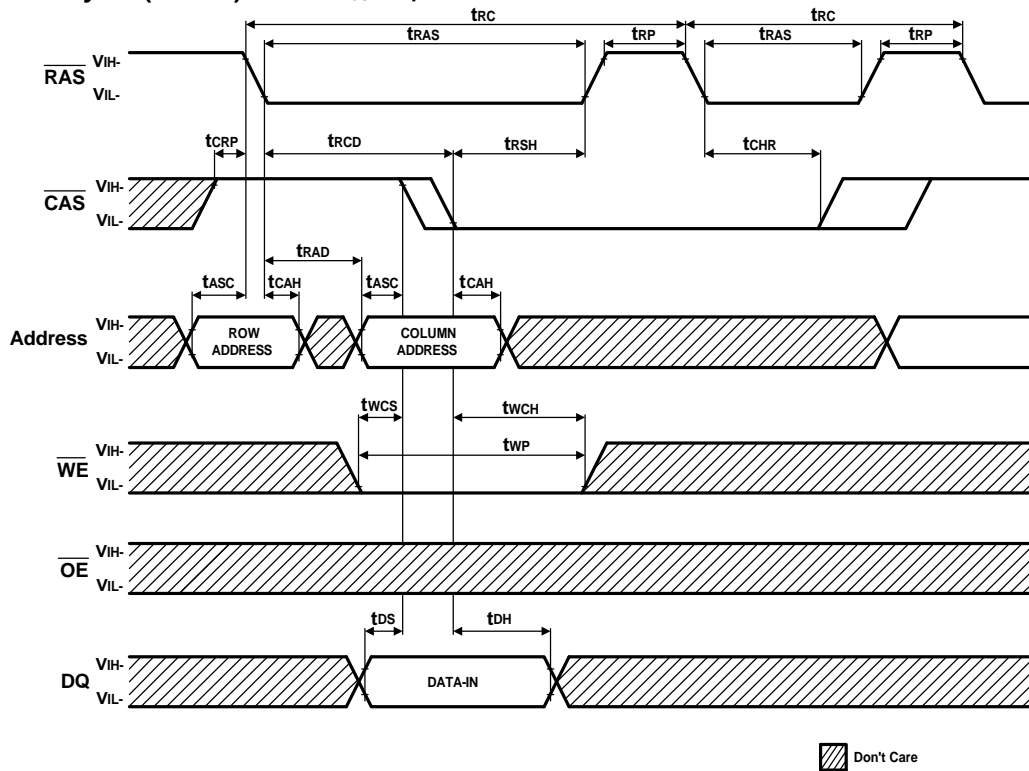
**RAS -Only Refresh Cycle**



**Hidden Refresh Cycle ( Read )**



**Hidden Refresh Cycle ( Write ) NOTE : D<sub>OUT</sub> =Open**





The diagram illustrates the timing relationships for three memory operations: Read Cycle, Write Cycle, and Read-Modify-Write. The signals shown are RAS, CAS, Address, WE, OE, DQ, and V<sub>OH</sub>/V<sub>OL</sub>.

**Read Cycle:** Shows the sequence from address strobe (RAS) to data output (DQ). Key parameters include t<sub>AS</sub> (RAS to CAS delay), t<sub>CH</sub> (CAS to column address), t<sub>CP</sub> (column address to data output), t<sub>SH</sub> (data output to RAS), t<sub>CS</sub> (CAS to data output), t<sub>AL</sub> (column address to data output), t<sub>CAH</sub> (column address to data output), t<sub>RRH</sub> (data output to RAS), and t<sub>CH</sub> (data output to RAS).

**Write Cycle:** Shows the sequence from address strobe (RAS) to data input (DQ). Key parameters include t<sub>WRP</sub> (write recovery period), t<sub>WRH</sub> (write recovery time), t<sub>WC</sub> (write cycle time), t<sub>WL</sub> (write latency), t<sub>WCW</sub> (write cycle width), and t<sub>WP</sub> (write period).

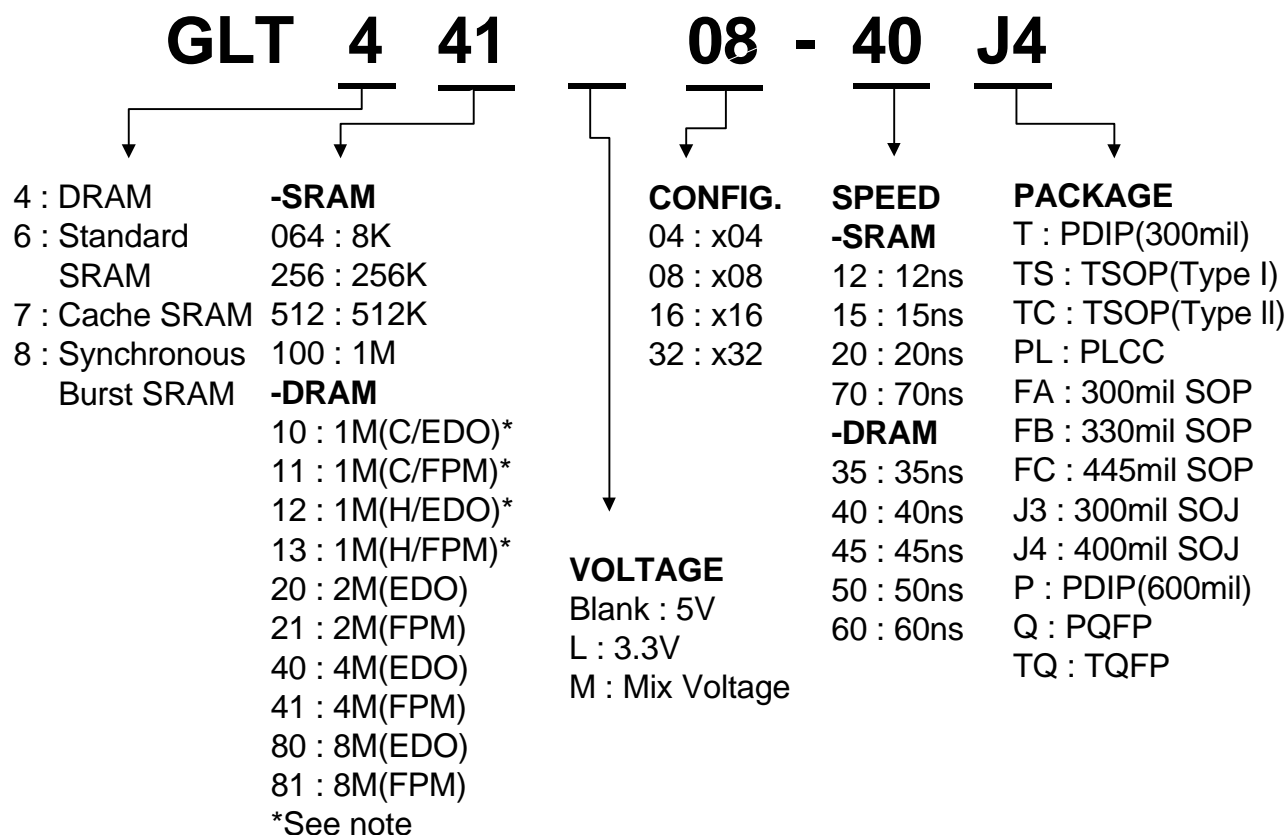
**Read-Modify-Write:** Shows the sequence for reading, modifying, and writing data. Key parameters include t<sub>DS</sub> (data strobe to data output), t<sub>DH</sub> (data output to data input), t<sub>WD</sub> (write data to data output), t<sub>CD</sub> (column address to data output), t<sub>AWD</sub> (address to write data), t<sub>WCW</sub> (write cycle width), t<sub>RWL</sub> (read write latency), t<sub>WP</sub> (write period), t<sub>CS</sub> (CAS to data output), t<sub>CAC</sub> (column address to data output), t<sub>AA</sub> (address to data output), t<sub>OE</sub> (output enable to data output), t<sub>ED</sub> (output enable to data input), t<sub>DL</sub> (data input to data output), t<sub>CLZ</sub> (data output to data input), t<sub>OEZ</sub> (output enable to data input), and t<sub>DS</sub> (data strobe to data input).

The diagram also includes a legend for "Don't Care" states, indicated by a shaded box.

## Ordering Information

<b>Part Number</b>	<b>SPEED</b>	<b>POWER</b>	<b>FEATURE</b>	<b>PACKAGE</b>
GLT44108-40J4	40ns	Normal	FPM	SOJ 400mil 28L
GLT44108-50J4	50ns	Normal	FPM	SOJ 400mil 28L
GLT44108-60J4	60ns	Normal	FPM	SOJ 400mil 28L

## Parts Numbers (Top Mark) Definition :



Note : C→CDROM , H→HDD.

Example :

1. GLT710008-15T    1Mbit(128Kx8)15ns 5V SRAM PDIP(300mil)Package type.
2. GLT44016-40J4    4Mbit(256Kx16)40ns 5V DRAM SOJ(400mil)Package type.

**Package Information**

400mil 28 Lead Small Outline J-form Package (SOJ)

