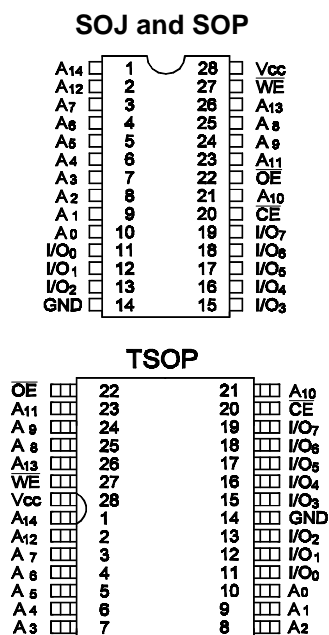
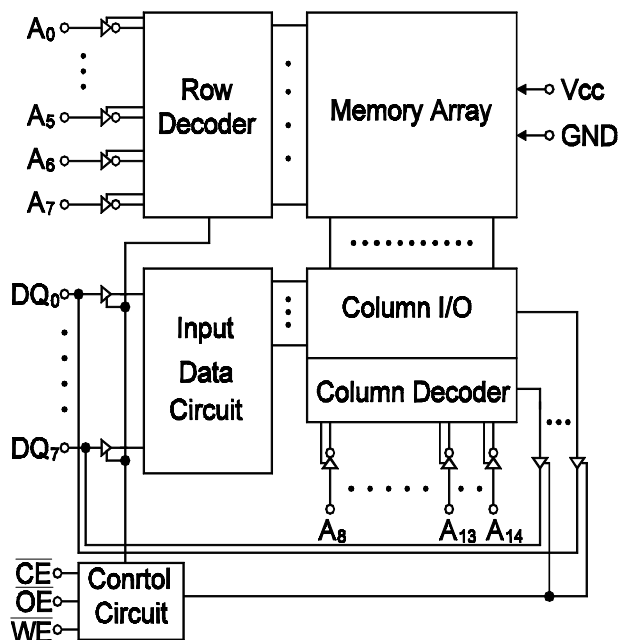


**Features :**

- \* 32K x 8-bit organization.
- \* Very high speed 12,15,20 ns.
- \* Low standby power.
- \* Fully static operation
- \*  $5V \pm 10\%$  power supply.
- \* TTL compatible I/O.
- \* Three state output.
- \* Chip enable for simple memory expansion.
- \* Available 300 mil SOJ, 28 pin TSOP and 330 mil SOP Packages.
- \* Industrial Grade Available ( $-40^{\circ}\text{C} \sim 85^{\circ}\text{C}$ ).

**Description :**

GLT725608 is high performance 256K bit static random access memory organized as 32K by 8 bits and operate at a single 5 volt supply. Fabricated with G-Link Technology's very advanced CMOS sub-micron technology, GLT725608 offer a combination of features: very high speed and very low stand-by current. In addition, this device also supports easy memory expansion with an active LOW chip enable ( $\overline{\text{CE}}$ ) as well as an active LOW output enable ( $\overline{\text{OE}}$ ) and three state outputs.

**Pin Configurations :**

**Function Block Diagram :**


**Pin Descriptions:**

Name	Function
$A_0 - A_{14}$	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$I/O_0 - I/O_7$	Data Input and Data Output
$V_{CC}$	+5V Power Supply
GND	Ground

**Truth Table:**

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	$V_{CC}$ Current
Not Selected (Power Down)	X	H	X	High Z	$I_{CCSB}, I_{CCSB1}$
Output Disabled	H	L	H	High Z	$I_{CC}$
Read	H	L	L	$D_{OUT}$	$I_{CC}$
Write	L	L	X	$D_{IN}$	$I_{CC}$

**Absolute Maximum Ratings:**

Ambient Temperature

Under Bias.....-10°C to +80°C

Storage Temperature(plastic)....-55°C to +125°C

Voltage Relative to GND.....-0.5V to +7.0V

Data Output Current.....50mA

Power Dissipation.....1.0W

1.Stresses greater than those listed under ABSOLUTE MAXIMUM RATING may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Operation Range :**

Range	Temperature	Vcc
Commercial	0°C to + 70°C	5V ± 10%
Industrial	-40°C to 85°C	5V ± 10%

**Capacitance <sup>(1)</sup>TA=25°C,f=1.0MHZ :**

Sym.	Parameter	conditions	Max. Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	8 pF
$C_{I/O}$	Input / output Capacitance	$V_{I/O} = 0V$	10 pF

## DC Characteristics

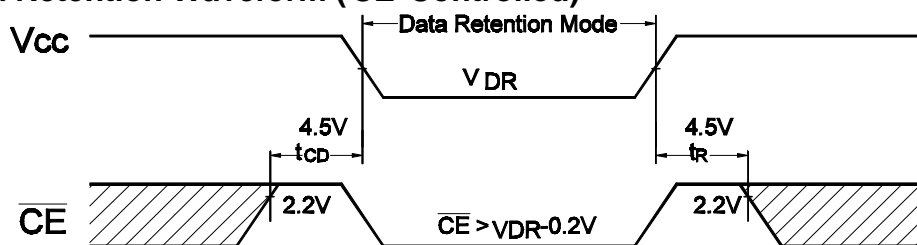
Sym.	Parameter	Test Conditions	Min.	Typ <sup>(1)</sup>	Max.	Unit
V <sub>IL</sub>	Guaranteed Input Low Voltage <sup>(2)</sup>		-0.3	-	+0.8	V
V <sub>IH</sub>	Guaranteed Input High Voltage <sup>(2)</sup>		2.2	-	V <sub>CC</sub> +0.3	V
I <sub>LI</sub>	Input Leakage Current	V <sub>CC</sub> = Max., V <sub>IN</sub> =0V to V <sub>CC</sub>	-5	-	5	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> = Max., $\overline{CE} \geq V_{IH}$	-5	-	5	μA
V <sub>OL</sub>	Output Low Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> =8mA	-	-	0.4	V
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> =-4mA	2.4	-	-	V
I <sub>CC</sub>	Operating Power Supply Current	V <sub>CC</sub> = Max., $\overline{CE} \leq V_{IL}$ , I <sub>I/O</sub> =0mA., F= F <sub>max</sub> <sup>(3)</sup>	-	-	-12 -15 -20 160 150 120	mA
I <sub>CCSB</sub>	Standby Power Supply Current	V <sub>CC</sub> = Max., $\overline{CE} \geq V_{IH}$ , I <sub>I/O</sub> =0mA., F= F <sub>max</sub> <sup>(3)</sup>	-	-	40 30 20	mA
I <sub>CCSB1</sub>	Power Down Power Supply Current	V <sub>CC</sub> = Max., $\overline{CE} \geq V_{CC}-0.2V$ , V <sub>IN</sub> ≥V <sub>CC</sub> . -0.2V or	-	-	10 10 10	mA

1. Typical characteristics are at V<sub>CC</sub>=5V, T<sub>A</sub>=25
2. These are absolute values with reject to device ground and all overshoots due to system or tester noise are included.
3. F<sub>MAX</sub>=1/t<sub>RC</sub>.

## Data Retention

Sym.	Parameter	Test Conditions	Min.	Typ <sup>(1)</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data retention	$\overline{CE} \geq V_{CC}-0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V	2.0	-	5.5	V
I <sub>CCDR</sub> <sup>(1)</sup>	Data Retention Current	V <sub>DR</sub> =2.0V		-	30	μA
		V <sub>DR</sub> =3.0V			50	μA
t <sub>CDR</sub>	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t <sub>R</sub>	Operating Recovery Time		t <sub>RC</sub> <sup>(2)</sup>	-	-	ns

1.  $\overline{CE} \geq V_{DR}-0.2V$ , V<sub>IN</sub> ≥ V<sub>DR</sub> -0.2V or V<sub>IN</sub> ≤ 0.2V.
2. t<sub>RC</sub> =Read Cycle Time.

**Low  $V_{CC}$  Data Retention Waveform ( $\overline{CE}$  Controlled)**

**AC Test Conditions**

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3 ns
Timing Reference Level	1.5V

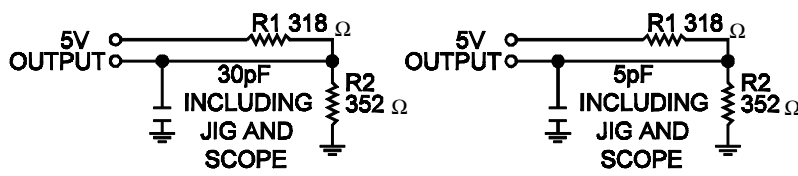
**AC Test Loads and Waveforms**


Figure 1a

Figure 1b

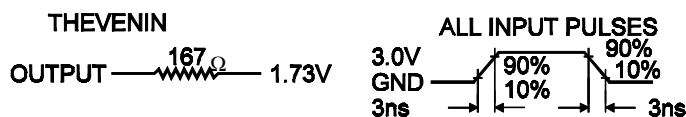
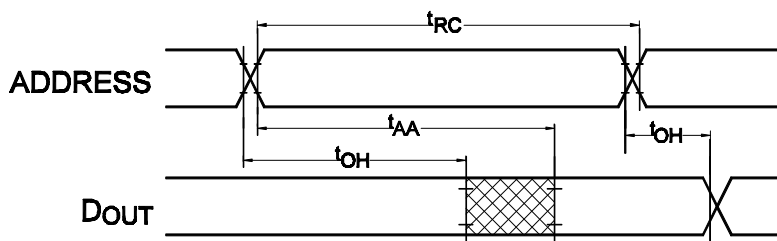
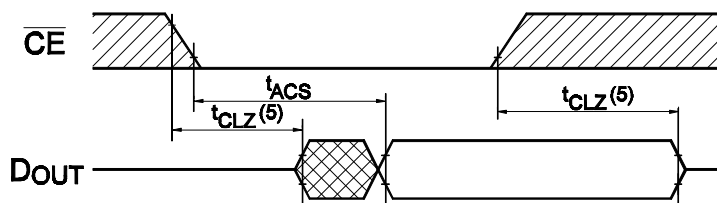
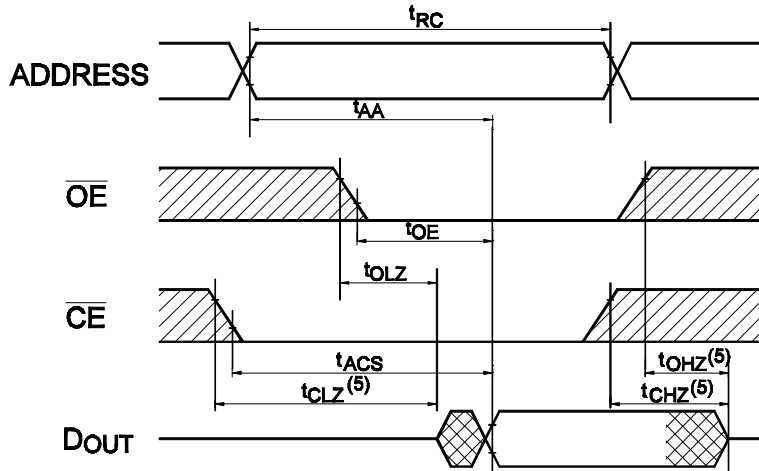


Figure 2

**AC Electrical Characteristics**
**Read Cycle**

JEDEC Parameter Name	Parameter Name	Parameter	725608-12 Min. Max.	725608-15 Min. Max.	725608-20 Min. Max.	Unit
$t_{AVAX}$	$t_{RC}$	Read Cycle Time	12 -	15 -	20 -	ns
$t_{AVQV}$	$t_{AA}$	Address Access Time	- 12	- 15	- 20	ns
$t_{E1LQV}$	$t_{ACS}$	Chip Select Access Time, $\overline{CE}$	- 12	- 15	- 20	ns
$t_{GLQV}$	$t_{OE}$	Output Enable to Output Valid	- 5	- 6	- 8	ns
$t_{E1LQX}$	$t_{CLZ}$	Chip Select to Output Low Z, $\overline{CE}$	3 -	3 -	3 -	ns
$t_{GLQX}$	$t_{OLZ}$	Output Enable to Output in Low Z	3 -	3 -	3 -	ns
$t_{E1HQZ}$	$t_{CHZ}$	Chip Deselect to Output in High Z, $\overline{CE}$	- 7	- 8	- 10	ns
$t_{GHQZ}$	$t_{OHZ}$	Output Disable to Output in High Z	- 6	- 6	- 8	ns
$t_{AXQX}$	$t_{OH}$	Output Hold from Address Change	3 -	3 -	3 -	ns

**Switching Waveform (Read Cycle)**
**READ CYCLE 1 (1,2,4)**

**READ CYCLE 2 (1,3,4)**

**READ CYCLE 3 (1)**

**Notes:**

1.  $\overline{WE}$  is High for READ Cycle.
2. Device is continuously selected  $\overline{CE} \leq V_{IL}$ .
3. Address valid prior to or coincident with  $\overline{CE}$  transition low and/or transition high.
4.  $\overline{OE} \leq V_{IL}$ .
5. Transition is measured  $\pm 200\text{mV}$  from steady state with  $C_L = 5\text{pF}$ .

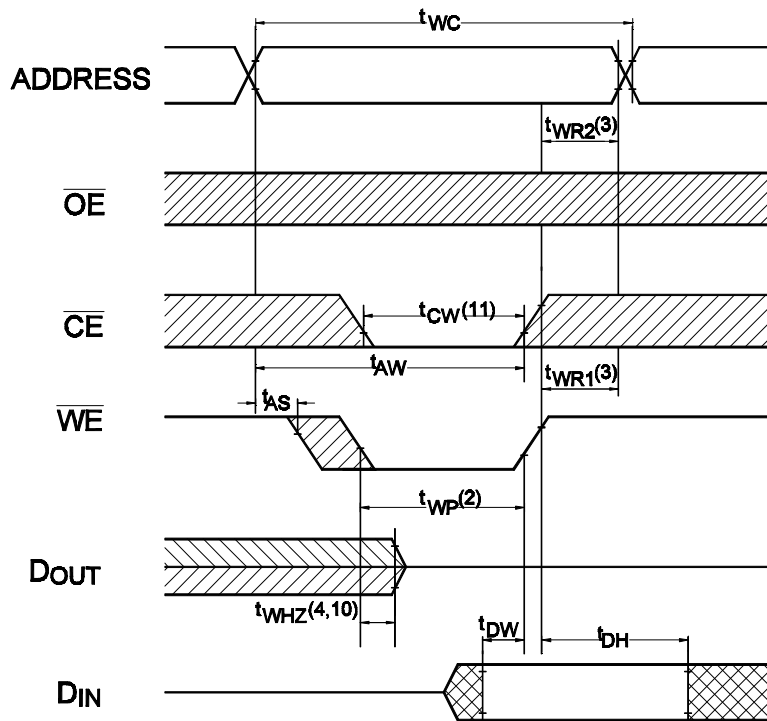
## AC Electrical Characteristics

### Write Cycle

JEDEC Parameter Name	Parameter Name	Parameter	725608-12 Min. Max.	725608-15 Min. Max.	725608-20 Min. Max.	Unit
$t_{AVAX}$	$t_{WC}$	Write Cycle Time	12 -	15 -	20 -	ns
$t_{E1LWH}$	$t_{CW}$	Chip Select to End of Write	10 -	12 -	15 -	ns
$t_{AVWL}$	$t_{AS}$	Address Set up Time	0 -	0 -	0 -	ns
$t_{AVWH}$	$t_{AW}$	Address Valid to End of Write	10 -	12 -	15 -	ns
$t_{WLWH}$	$t_{WP}$	Write Pulse Width	10 -	12 -	15 -	ns
$t_{WHAX}$	$t_{WR1}$	Write Recovery Time, $\overline{WE}$	0 -	0 -	0 -	ns
$t_{E2LAX}$	$t_{WR2}$	Write Recovery Time, $\overline{CE}$	0 -	0 -	0 -	ns
$t_{WLQZ}$	$t_{WHZ}$	Write to Output in High Z	- 7	- 8	- 10	ns
$t_{DVWH}$	$t_{DW}$	Data to Write Time Overlap	6 -	7 -	8 -	ns
$t_{WHDX}$	$t_{DH}$	Data Hold from Write Time	0 -	0 -	0 -	ns
$t_{WHQX}$	$t_{OW}$	End of Write to Output Active	3 -	3 -	3 -	ns

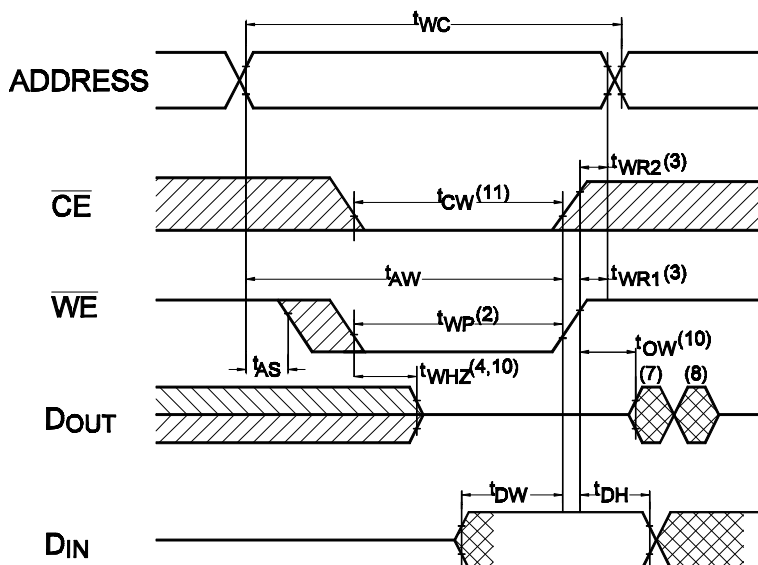
### Switching Waveforms(Write Cycle)

#### WRITE CYCLE 1<sup>(1)</sup>



## Switching Waveform (Write Cycle)

### WRITE CYCLE 2<sup>(1,6)</sup>



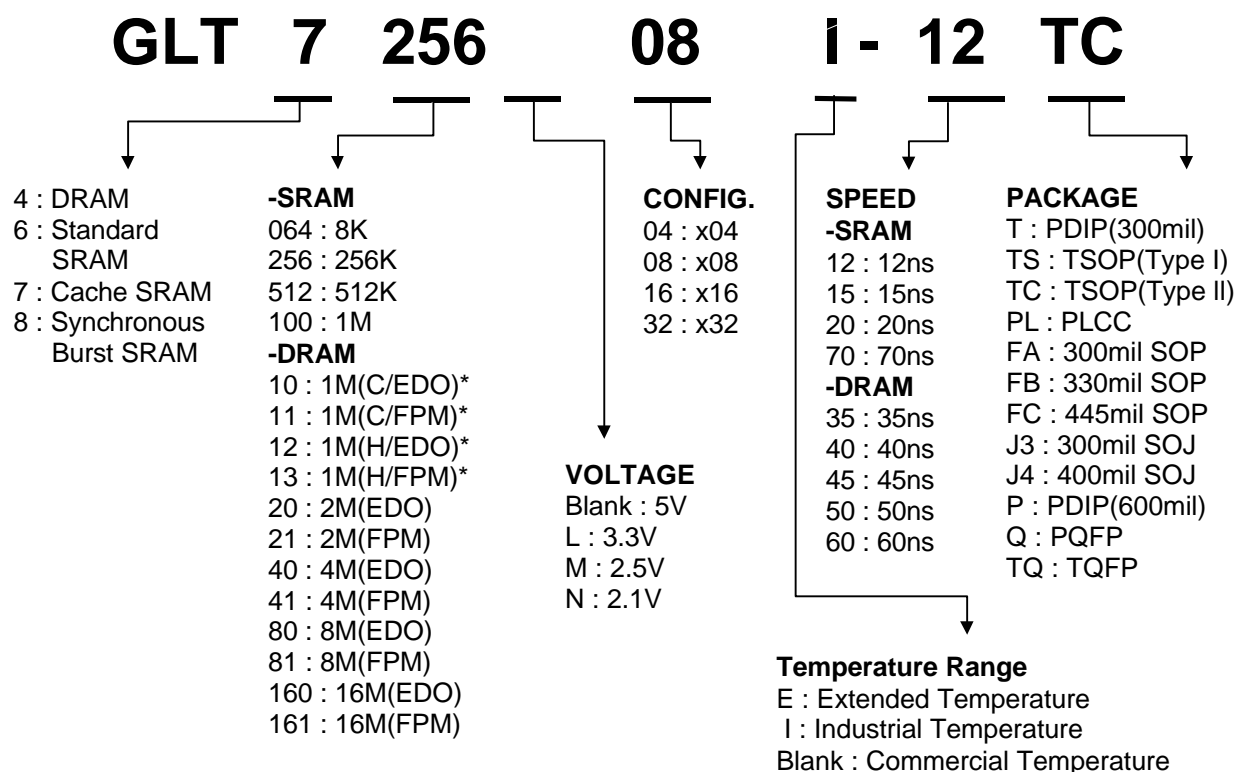
#### Note:

1.  $\overline{WE}$  must be high during address transitions.
2. The internal write time of the memory is defined by the overlap  $\overline{CE}$  low and  $\overline{WE}$  low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3.  $T_{WR}$  is measured from the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high at the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the  $\overline{CE}$  low transition occurs simultaneously with the  $\overline{WE}$  low transitions or after the  $\overline{WE}$  transition, outputs remain in a high impedance state.
6.  $\overline{OE}$  is continuously low ( $\overline{OE} = V_{IL}$ ).
7.  $D_{OUT}$  is the same phase of write data of this write cycle.
8.  $D_{OUT}$  is the read data of next address.
9. If  $\overline{CE}$  is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured  $\pm 200\text{mV}$  from steady state with  $C_L = 5\text{pF}$ .
11.  $t_{CW}$  is measured from  $\overline{CE}$  going low to the end of write.

## Ordering Information

<b>Part Number</b>	<b>SPEED</b>	<b>POWER</b>	<b>PACKAGE</b>
GLT725608-12J3	12ns	Normal	SOJ 300mil 28L
GLT725608-15J3	15ns	Normal	SOJ 300mil 28L
GLT725608-20J3	20ns	Normal	SOJ 300mil 28L
GLT725608-12TS	12ns	Normal	TSOP 28L
GLT725608-15TS	15ns	Normal	TSOP 28L
GLT725608-20TS	20ns	Normal	TSOP 28L
GLT725608-12TC	12ns	Normal	TSOP II 28L
GLT725608-15TC	15ns	Normal	TSOP II 28L
GLT725608-20TC	20ns	Normal	TSOP II 28L
GLT725608-12FB	12ns	Normal	SOP 330mil 28L
GLT725608-15FB	15ns	Normal	SOP 330mil 28L
GLT725608-20FB	20ns	Normal	SOP 330mil 28L

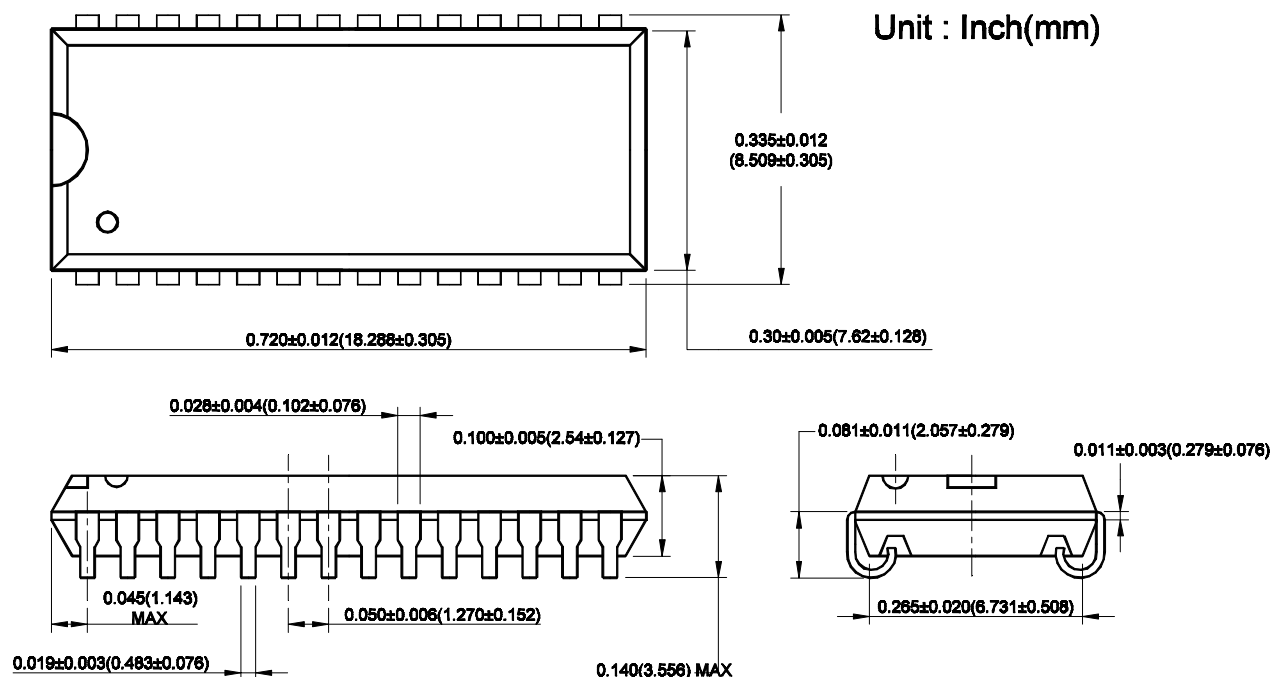
## Parts Numbers (Top Mark) Definition :



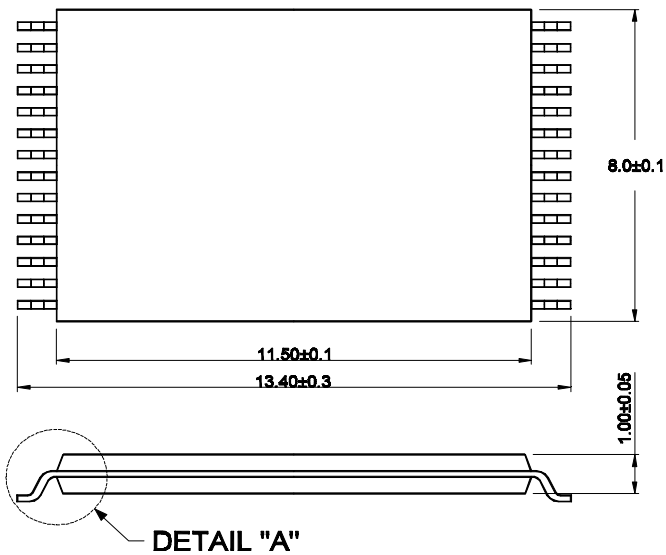


**Package Information**

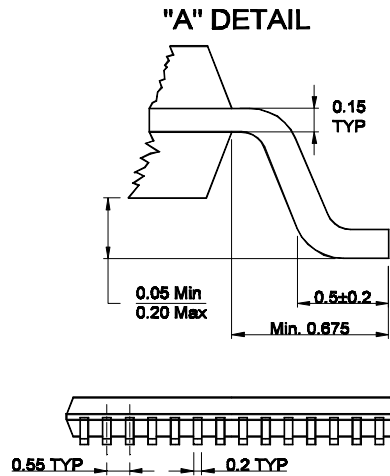
300mil 28 Lead Small Outline J-form Package (SOJ)



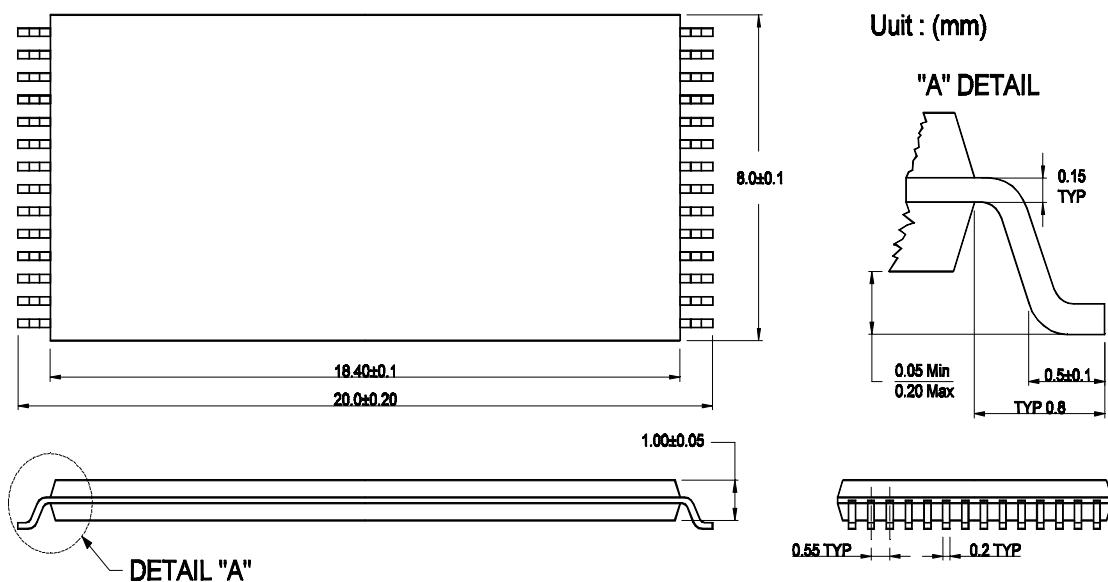
28L (8×13.4 mm) Thin Small Outline Package (TSOP) Type I



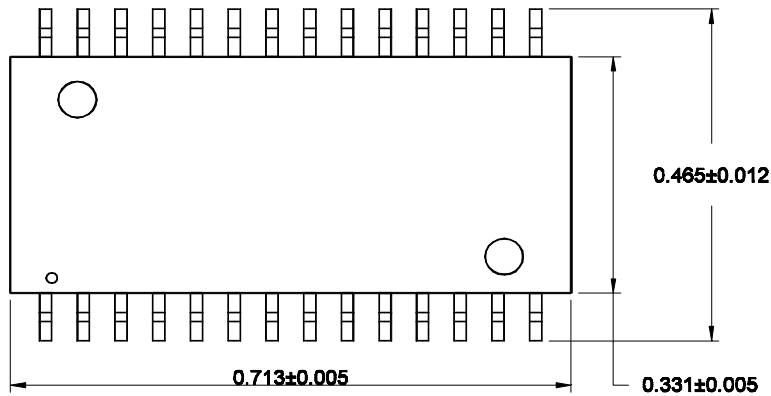
Unit : (mm)



28L (8x20mm) Thin Small Outline Package (TSOP) Type I



330mil 28 Lead Thin Small Outline (Gull-Wing) Package (SOP)



Unit :Inch

