

# PWRLITE LU1014D

## High Performance N-Channel *POWERJFET™* with PN Diode



### Features

- ❖ Superior gate charge x Rds on product (FOM)
- ❖ Trench Power JFET with low threshold voltage Vth.
- ❖ Device fully “ON” with Vgs = 0.7V
- ❖ Optimum for “Low Side” Buck Converters
- ❖ Excellent for high frequency dc/dc converters
- ❖ Optimized for Secondary Rectification in isolated DC-DC
- ❖ Low Rg and low Cds for high speed switching

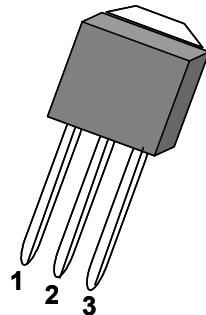
### Applications

- ❖ DC-DC Converters
- ❖ Synchronous Rectifiers
- ❖ PC Motherboard Converters
- ❖ Step-down power supplies
- ❖ VRM Modules

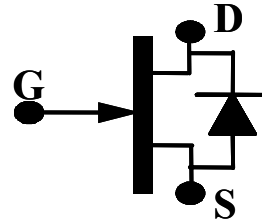
### Description

The Power JFET transistor from Lovoltech is a device that presents a Low Rds on allowing for improved efficiencies in DC-DC switching applications. The device is designed with a low threshold such that drivers can operate at 5V, which reduces the driver power dissipation and increases the overall efficiency. Lower threshold produces faster turn-on/turn-off, which minimizes the required dead time. A PN Diode is added for applications where a freewheeling diode is required. This product has tin plated leads.

### IPAK Lead-free Pin Assignments



Case TO251 (IPAK)



N – Channel PowerJFET  
with PN Diode

### Pin Definitions

Pin Number	Pin Name	Pin Function Description	Product Summary		
1	Gate	Gate. Transistor Gate	V <sub>DS</sub> (V)	R <sub>ds on</sub> (Ω)	I <sub>D</sub> (A)
2, 4	Drain	Drain. Transistor Drain	24V	0.0065	50 <sup>1</sup>
3	Source	Source. Transistor Source			

### Absolute Maximum Ratings

Parameter	Symbol	Ratings	Units
Drain-Source Voltage	V <sub>DS</sub>	24	V
Gate-Source Voltage	V <sub>GS</sub>	-12	V
Gate-Drain Voltage	V <sub>GD</sub>	-28	V
Continuous Drain Current	I <sub>D</sub>	50 <sup>1</sup>	A
Pulsed Drain Current	I <sub>D</sub>	100	A
Single Pulse Drain-to-Source Avalanche Energy at 25°C (V <sub>DD</sub> = 6V <sub>DC</sub> , I <sub>L</sub> =60A <sub>PK</sub> , L=0.3mH, R <sub>G</sub> =100 Ω)	E <sub>AS</sub>	200	mJ
Junction Temperature	T <sub>J</sub>	-55 to 150°C	°C
Storage Temperature	T <sub>STG</sub>	-65 to 150°C	°C
Lead Soldering Temperature, 10 seconds	T	260°C	°C
Power Dissipation (Derated at 25°C)	P <sub>D</sub>	69	W

## Thermal Resistance

Symbol	Parameter		DPAK Ratings		Units
$R\Theta_{JA}$	Thermal Resistance Junction-to-Ambient		90		°C/W
$R\Theta_{JC}$	Thermal Resistance Junction-to-Case		1.8		°C/W

## Electrical Specifications

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

The  $\phi$  denotes a specification which apply over the full operating temperature range.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
	Static						
BV <sub>DSX</sub>	Breakdown Voltage Drain to Source	I <sub>D</sub> = 0.5 mA V <sub>GS</sub> = -4 V		24	28		V
BV <sub>GDO</sub>	Breakdown Voltage Gate to Drain	I <sub>G</sub> = -50μA			-32	-28	V
BV <sub>GSO</sub>	Breakdown Voltage Gate to Source	I <sub>G</sub> = -50μA			-14	-12	V
R <sub>DS(ON)</sub>	Drain to Source On Resistance <sup>2</sup>	I <sub>G</sub> = 40 mA, I <sub>D</sub> =10A I <sub>G</sub> = 10 mA, I <sub>D</sub> =10A I <sub>G</sub> = 5 mA, I <sub>D</sub> =10A			4.6 4.8 4.9	6.5 7.0	mΩ mΩ
V <sub>GS(TH)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =0.1 V, I <sub>D</sub> =250μA			-1		V
TCV <sub>GSTH</sub>	Temperature Coefficient of Gate Threshold Voltage	V <sub>DS</sub> =0.1 V, I <sub>D</sub> =250μA			-2.6		mV/°C
	Dynamic						
Q <sub>Gsync</sub>	Total Gate Charge Sync JFET	ΔV <sub>Drive</sub> =5V, V <sub>DS</sub> =0.1V (Fig. 2)			9.8		nC
Q <sub>G</sub>	Total Gate Charge	ΔV <sub>Drive</sub> =5V, I <sub>D</sub> =10A, V <sub>DS</sub> =15V			12.4		nC
Q <sub>GD</sub>	Gate to Drain Charge	V <sub>DS</sub> =13.5V to V <sub>DS</sub> =1.5V			8.1		nC
Q <sub>GS</sub>	Gate to Source Charge	V <sub>GS</sub> =-4.5V to V <sub>DS</sub> =13.5V			4.3		nC
Q <sub>SW</sub>	Switching Charge	V <sub>GS</sub> =-2V to V <sub>DS</sub> =1.5V			9.1		nC
R <sub>G</sub>	Gate Resistance				0.7		Ω
T <sub>D(ON)</sub>	Turn-on Delay Time	V <sub>DD</sub> =15V, I <sub>D</sub> =10A V <sub>Drive</sub> = 5 V Resistive Load			5.5		ns
T <sub>R</sub>	Rise Time				12.6		
T <sub>D(OFF)</sub>	Turn-off Delay				10.3		
T <sub>F</sub>	Fall Time				6.6		
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =10V, V <sub>GS</sub> = -5 V, 1MHz. (see Fig. 4)			1147		pF
C <sub>OSS</sub>	Output Capacitance				467		
C <sub>GS</sub>	Gate-Source Capacitance				784		
C <sub>GD</sub>	Gate-Drain Capacitance				363		
C <sub>DS</sub>	Drain-Source Capacitance				104		
	PN Diode						
I <sub>R</sub>	Reverse Leakage	V <sub>R</sub> =20V, V <sub>gs</sub> = -4V				0.3	mA
V <sub>F</sub>	Forward Voltage	I <sub>F</sub> = 1 A			812		mV
V <sub>F</sub>	Forward Voltage	I <sub>F</sub> = 10 A			932		mV
V <sub>F</sub>	Forward Voltage	I <sub>F</sub> = 20 A			1010		mV
Q <sub>rr</sub>	Reverse Recovery Charge	I <sub>s</sub> = 10 A di/dt = 100A/us,			7		nC
T <sub>rr</sub>	Reverse Recovery Time	I <sub>s</sub> = 10 A di/dt = 100A/us,			13.3		ns

### Notes:

- Current is limited by bondwire; with an  $R_{thjc} = 1.8^\circ\text{C/W}$  the chip is able to carry 80A.
- Pulse width  $\leq 500\mu\text{s}$ , duty cycle  $\leq 2\%$

## Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

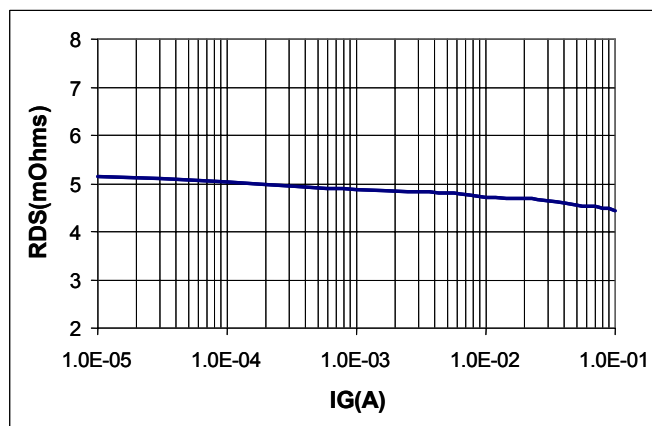


Figure 1 –  $R_{DS(on)}$  vs Gate Current at  $I_D = 10\text{A}$

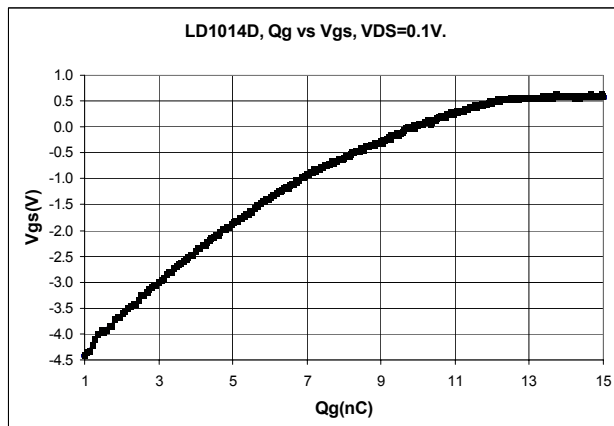


Figure 2 – Gate Charge  $Q_{g_{sync}}$  for  $V_{DS} = 0.1\text{V}$

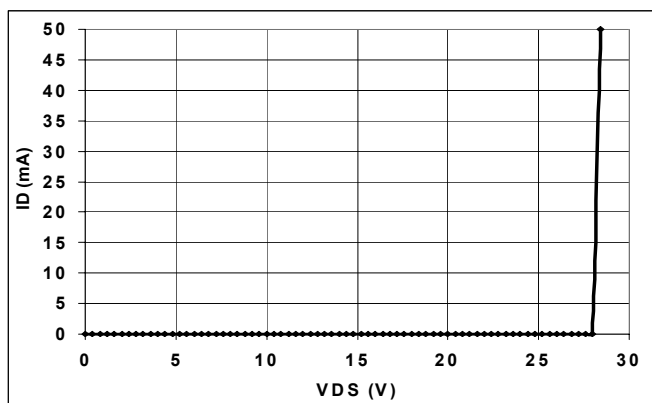


Figure 3 – Breakdown Voltage  $V_{DS}$  vs  $I_D$

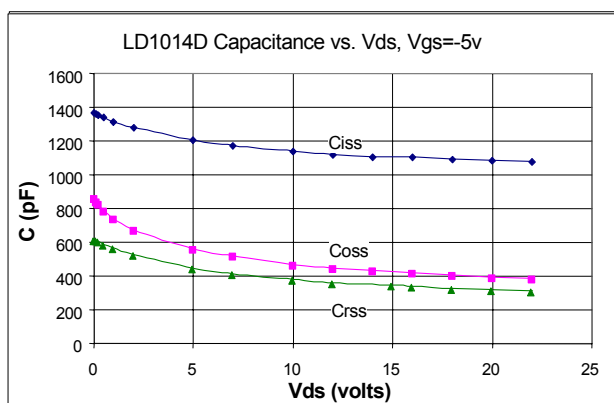


Figure 4 – Capacitance vs Drain Voltage  $V_{DS}$

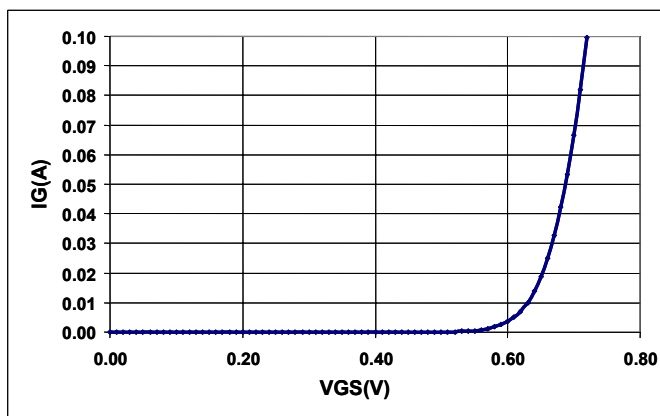


Figure 5 –  $I_G$  vs Gate Voltage  $V_{GS}$

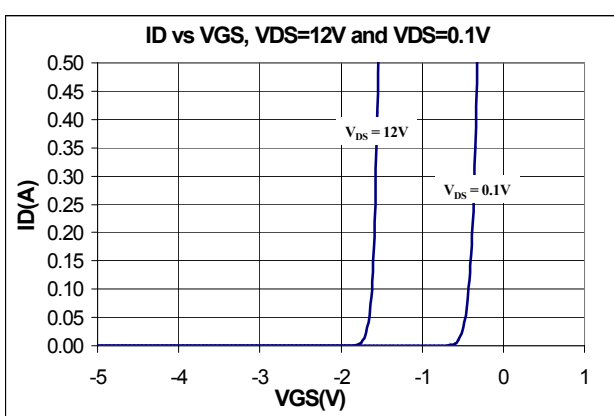
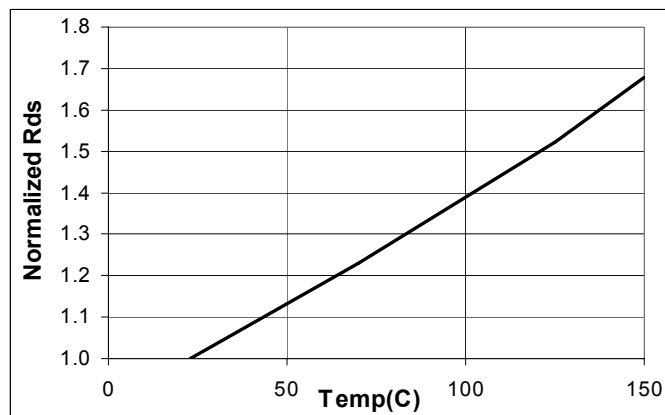


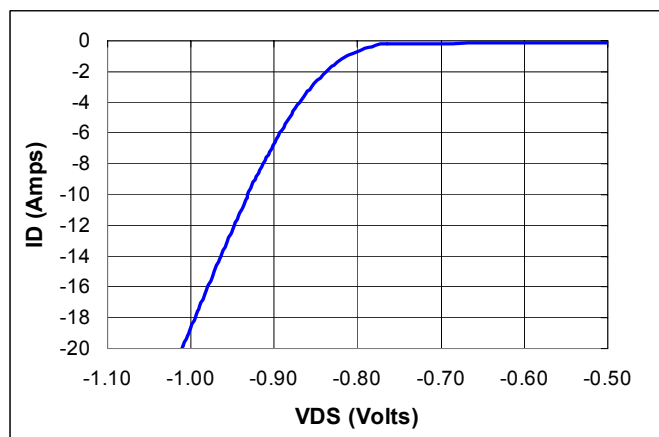
Figure 6 – Transfer Characteristic

## Typical Operating Characteristics

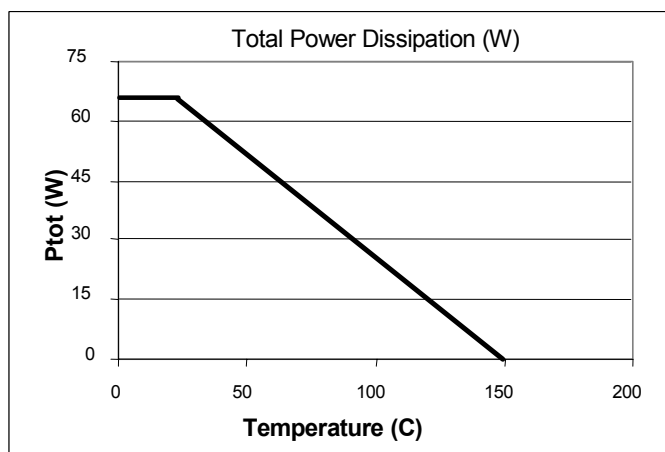
( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



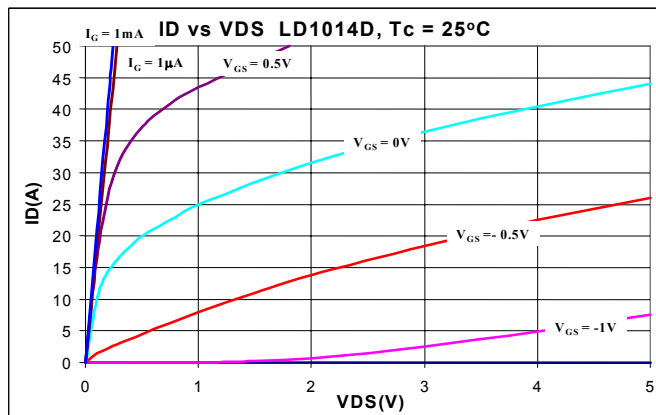
**Figure 7 –  $R_{DS(on)} = f(T)$ ;  $I_D = -10\text{A}$ ;  $I_G = 40\text{mA}$**



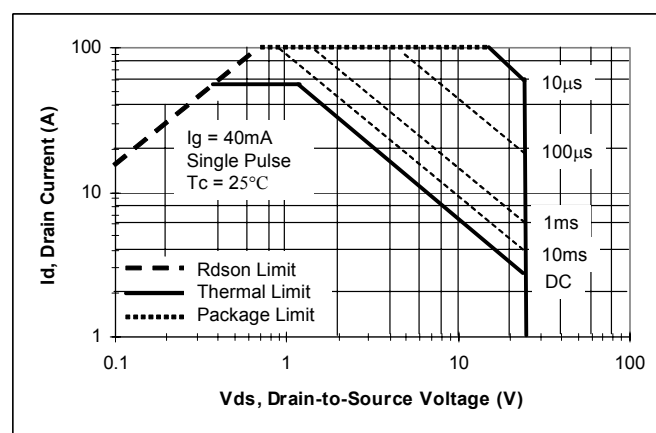
**Figure 9 – PN Diode Voltage vs Current**



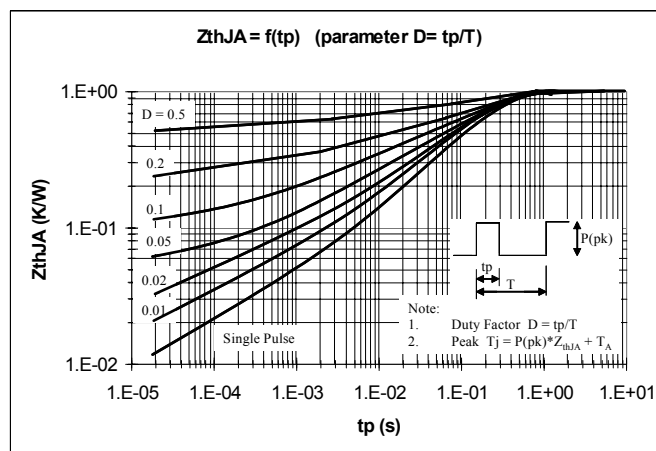
**Figure 11 – Total Power Dissipation**



**Figure 8 –  $I_D$  vs  $V_{DS}$  Characteristics**



**Figure 10 – Safe Operating Area**



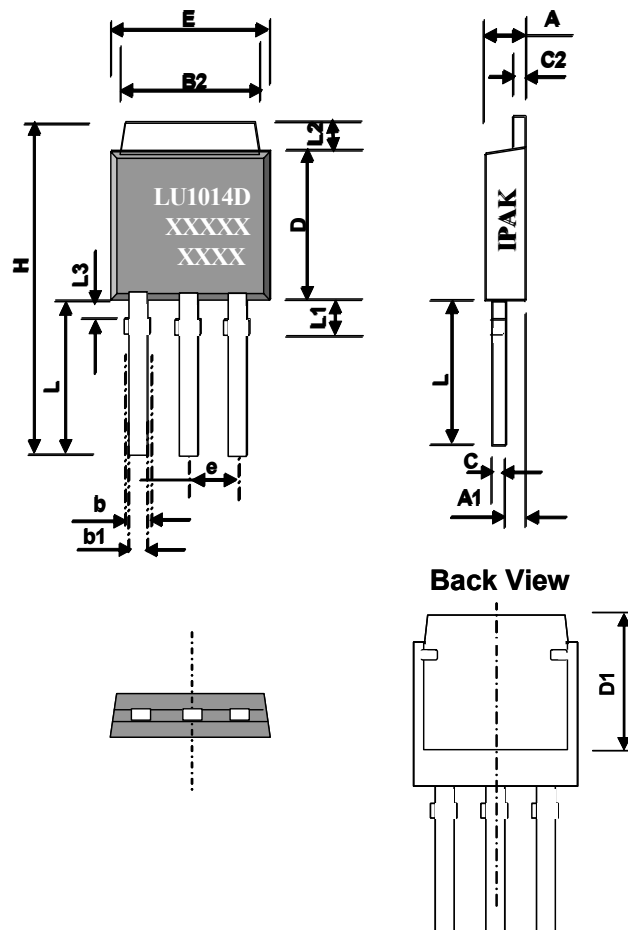
**Figure 12 – Normalized Thermal Response**

## Ordering Information

Product Number	PN Marking	Package	Notes:
LU1014D	LU1014D	TO251 (IPAK)	<b>This product is Pb-Free and has Tin Plated leads</b>

## Package and Marking Information

DIMENSIONS						
DIM.	mm.			inch		
	TYP.	MIN.	MAX.	TYP.	MIN.	MAX.
A		2.19	2.40		0.086	0.094
A1		0.89	1.14		0.035	0.045
b		0.76	1.14		0.030	0.045
b1		0.64	0.90		0.025	0.035
B2		5.20	5.46		0.205	0.215
C		0.45	0.60		0.017	0.023
C2		0.45	0.60		0.017	0.023
D		5.97	6.22		0.235	0.244
D1	5.64			0.222		
E		6.35	6.73		0.250	0.265
e	2.28			0.090		
H	13.19	13.06	13.32		0.514	0.525
L		5.95	7.6		0.234	0.300
L1		2.03	2.29		0.079	0.090
L3		0.63	1.14		0.025	0.045



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- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Datasheet Identification	Product Status	Definition
Advance Information	In definition or in Design	This datasheet contains the design specifications for product development. Specifications may change without notice.
Preliminary	Initial Production	This datasheet contains preliminary data; additional and application data will be published at a later date. Lovoltech, Inc. reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	In Production	This datasheet contains final specifications. Lovoltech reserves the right to make changes at any time without notice in order to improve the design.