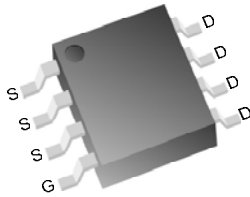


# LVS2100N N-Channel PowerJFET®

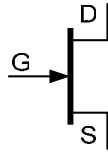
## Product Summary

	Typical	Max	
$V_{DS}$		24	V
$R_{DS(ON)} @ 0 V_{GS}$	11.5	14	mΩ

## Pinouts



SO-8



## Features

- Device is fully on @  $V_{GS} = 0V$ .
- Bidirectional blocking when off (no body diode)

## Applications

- Notebook battery switch:  
Each JFET replaces 2 P-Channel series MOSFETs

## Absolute Maximum Ratings

Absolute maximum ratings are the values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Symbol	Parameter	Conditions	Rating	Units
$V_{DSS}$	Drain to Source voltage		24	V
$V_{GS}$	Gate to Source voltage		-12	V
$V_{DG}$	Drain to Gate voltage		-28	V
$I_D$	Drain Current	Continuous, $T_C = 25^\circ C$	11	A
		Pulsed, 300μS	50	A
$T_J$	Junction Temperature		-55 to 150	°C
$T_{STG}$	Storage Temperature		-65 to 150	°C
	Lead Soldering Temperature	10 seconds, 1.6mm from case	260	°C
$P_D$	Power Dissipation	$T_A = 25^\circ C$ , Note 1	2.5	W
		$T_A = 25^\circ C$ , Note 2	1.3	W

## Thermal Resistance

Symbol	Resistance from:	Conditions	Rating	Units
$R_{\theta JA}$	Junction to Ambient	Note 1	50	°C/W
		Note 2	96	°C/W
$R_{\theta JC}$	Junction to Case		25	°C/W

Note 1. Mounted on 1 in.<sup>2</sup>, 2 oz copper on FR-4

Note 1. Mounted on 0.05 in.<sup>2</sup>, 0.5 oz. copper on FR-4

## Electrical Specifications @T<sub>J</sub> = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Static</b>						
BV <sub>DSX</sub>	Breakdown Voltage Drain to Source	I <sub>D</sub> = 0.5 mA, V <sub>GS</sub> = -4 V	24	28		V
BV <sub>GDO</sub>	Breakdown Voltage Gate to Drain	I <sub>G</sub> = -50μA		-32	-28	V
BV <sub>GSO</sub>	Breakdown Voltage Gate to Source	I <sub>G</sub> = -50μA		-14	-12	V
R <sub>DS(ON)</sub>	Drain to Source On Resistance	V <sub>GS</sub> = 0V, I <sub>D</sub> = -7A		11.5	14	mΩ
		V <sub>GS</sub> = 0V, I <sub>D</sub> = 7A		13	17	mΩ
V <sub>GS(OFF)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = 16 V, I <sub>D</sub> = 250μA		-2.5		V
<b>Dynamic</b>						
Q <sub>G</sub>	Total Gate Charge	ΔV <sub>GS</sub> = 5V, V <sub>DS</sub> = 15V		9.3		nC
Q <sub>GD</sub>	Gate to Drain charge	ΔV <sub>DS</sub> = 12V		6.1		nC
Q <sub>GS</sub>	Gate to Source Charge			3.2		nC
R <sub>G</sub>	Gate resistance			3		Ω
T <sub>D(ON)</sub>	Turn-on Delay	I <sub>D</sub> =15A Circuit of Figure 1		4		nS
T <sub>D(OFF)</sub>	Turn-off Delay			9		
T <sub>R</sub>	Rise Time			2		
T <sub>F</sub>	Fall Time			7		
C <sub>ISS</sub>	Input Capacitance			860		pF
C <sub>OSS</sub>	Output Capacitance			350		pF
C <sub>GS</sub>	Gate-Source Capacitance			588		pF
C <sub>GD</sub>	Gate-Drain Capacitance			272		pF
C <sub>DS</sub>	Drain-Source Capacitance			15		pF

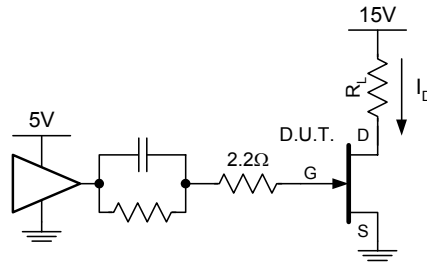


Figure 1. Switching test circuit.

## Typical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

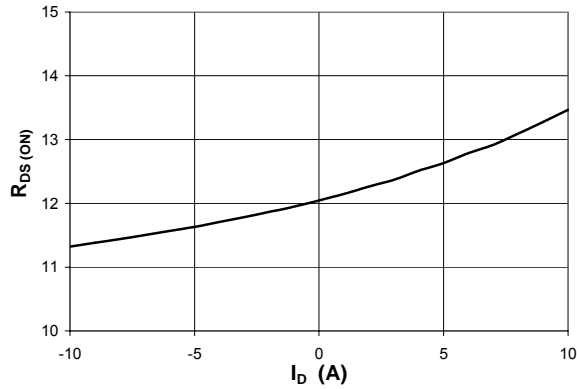


Figure 2.  $R_{DS(ON)}$  vs. Drain Current @  $V_{GS} = 0V$

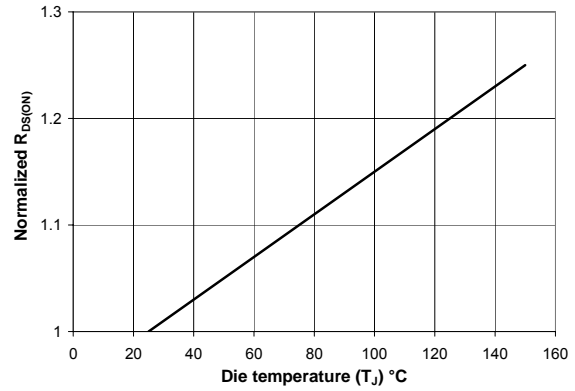


Figure 3. Normalized  $R_{DS(ON)}$  vs. junction temperature @  $I_D = -7A$

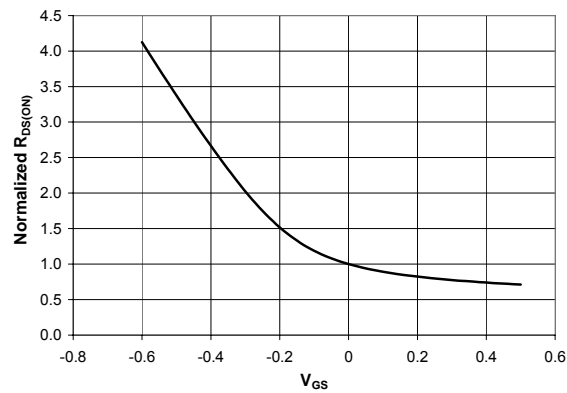
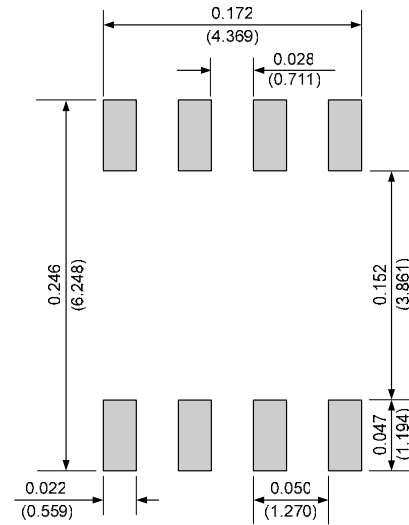
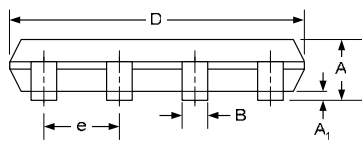
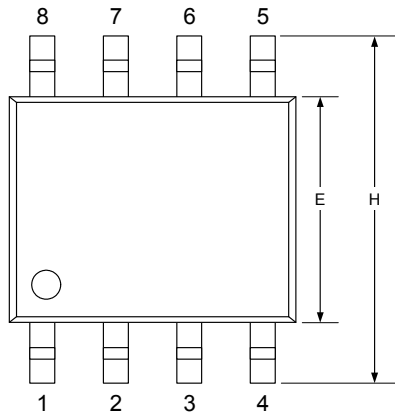


Figure 4. Normalized  $R_{DS(ON)}$  vs. @  $I_D = -7A$

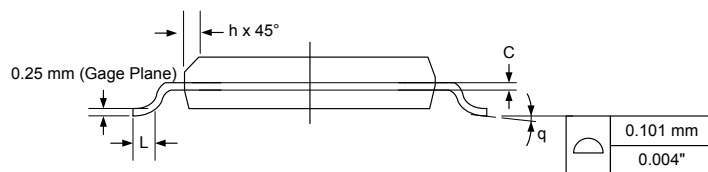
## Dimensional Outline Drawing

### SO-8 8-lead narrow SOIC

Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.0530	0.0690
A <sub>1</sub>	0.10	0.20	0.0040	0.0080
B	0.35	0.51	0.0140	0.0200
C	0.19	0.25	0.0075	0.0100
D	4.80	5.00	0.1890	0.1960
E	3.80	4.00	0.1500	0.1570
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.2280	0.2440
h	0.25	0.50	0.0100	0.0200
L	0.50	0.93	0.0200	0.0370
q	0°	8°	0°	8°



**Recommended minimum pad layout**  
dimensions in inches (mm)



Conforms to JEDEC part number MS-012

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**Ordering Information**

Part Number	Package	Packing
LVS2001N	SO-8	13" Tape and Reel, 2500 units / reel

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