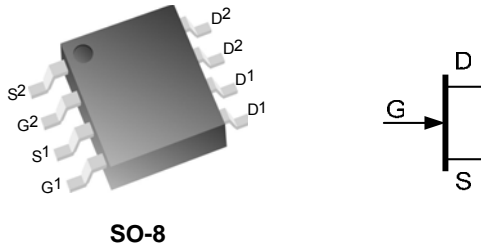


LVS2201N Dual N-Channel PowerJFET®

Product Summary

	Typical	Max	
V_{DS}		24	V
$R_{DS(ON)} @ 0 V_{GS}$	15.5	18	mΩ

Pinouts



Features

- Device is fully on @ $V_{GS} = 0V$.
- Bidirectional blocking when off (no body diode)

Applications

- Notebook battery switch:
Each JFET replaces 2 P-Channel series MOSFETs

Absolute Maximum Ratings

Absolute maximum ratings are the values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Symbol	Parameter	Conditions	Rating	Units
V_{DSS}	Drain to Source voltage		24	V
V_{GS}	Gate to Source voltage		-12	V
V_{DG}	Drain to Gate voltage		-28	V
I_D	Drain Current (note 1)	Continuous, $T_C = 25^\circ C$	7.5	A
		Pulsed, 300μS	20	A
T_J	Junction Temperature		-55 to 150	°C
T_{STG}	Storage Temperature		-65 to 150	°C
	Lead Soldering Temperature	10 seconds, 1.6mm from case	260	°C
P_D	Power Dissipation (single operation)	$T_A = 25^\circ C$, note 1	1.6	W
		$T_A = 25^\circ C$, note 2	1.2	W

Thermal Resistance

Symbol	Resistance from:	Conditions	Rating	Units
$R_{\theta JA}$	Junction to Ambient	note 1	78	°C/W
		note 2	105	°C/W
$R_{\theta JC}$	Junction to Case		40	°C/W

Note 1. Mounted on 1 in.², 2 oz copper on FR-4

Note 1. Mounted on 0.05 in.², 0.5 oz. copper on FR-4

Electrical Specifications @T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Static						
BV _{DSX}	Breakdown Voltage Drain to Source	I _D = 0.5 mA, V _{GS} = -4 V	24	28		V
BV _{GDO}	Breakdown Voltage Gate to Drain	I _G = -50μA		-32	-28	V
BV _{GSO}	Breakdown Voltage Gate to Source	I _G = -50μA		-14	-12	V
R _{DS(ON)}	Drain to Source On Resistance	V _{GS} = 0V, I _D = -4A		15.5	18	mΩ
		V _{GS} = 0V, I _D = 5A		18	22	mΩ
V _{GS(OFF)}	Gate Threshold Voltage	V _{DS} = 16 V, I _D = 250μA		-2.5		V
Dynamic						
Q _G	Total Gate Charge	ΔV _{GS} = 5V, V _{DS} = 15V		6.9		nC
Q _{GD}	Gate to Drain charge	ΔV _{DS} = 12V		4.5		nC
Q _{GS}	Gate to Source Charge			2.4		nC
R _G	Gate resistance			3		Ω
T _{D(ON)}	Turn-on Delay	I _D =15A Circuit of Figure 1		4		nS
T _{D(OFF)}	Turn-off Delay			9		
T _R	Rise Time			2		
T _F	Fall Time			7		
C _{ISS}	Input Capacitance			640		pF
C _{OSS}	Output Capacitance			260		pF
C _{GS}	Gate-Source Capacitance			437		pF
C _{GD}	Gate-Drain Capacitance			202		pF
C _{DS}	Drain-Source Capacitance			11		pF

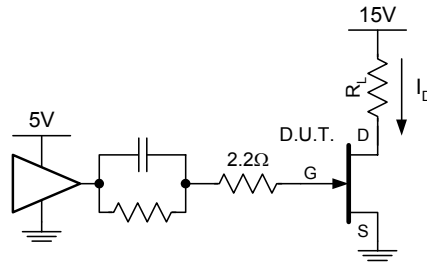


Figure 1. Switching test circuit.

Typical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

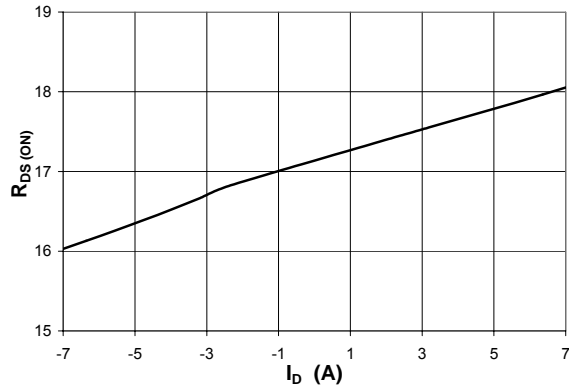


Figure 2. $R_{DS(on)}$ vs. Drain Current @ $V_{GS} = 0V$

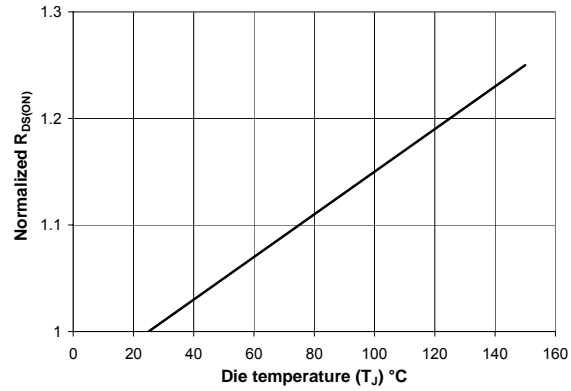


Figure 3. Normalized $R_{DS(on)}$ vs. junction temperature @ $I_D = -5A$

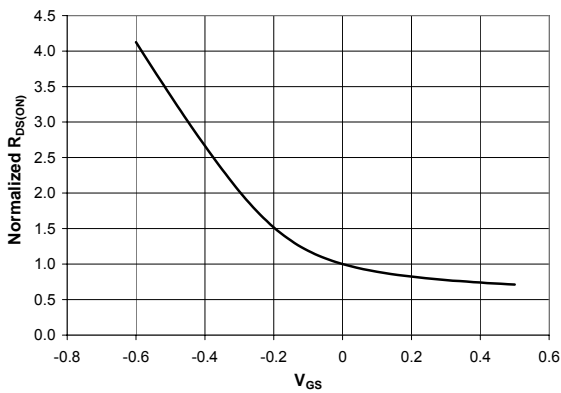
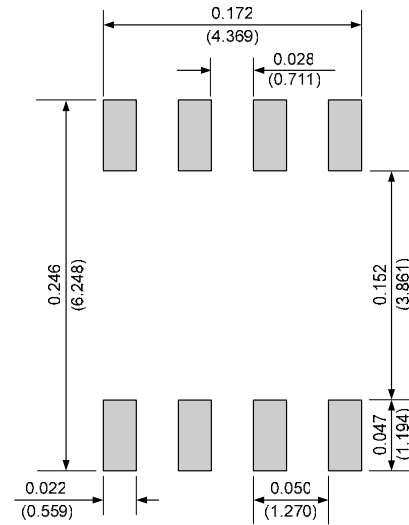
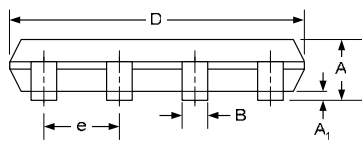
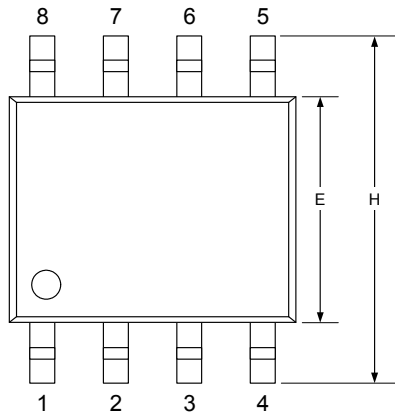


Figure 4. Normalized $R_{DS(on)}$ vs. @ $I_D = -5A$

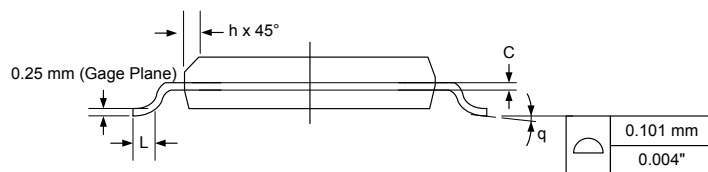
Dimensional Outline Drawing

SO-8 8-lead narrow SOIC

Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.0530	0.0690
A ₁	0.10	0.20	0.0040	0.0080
B	0.35	0.51	0.0140	0.0200
C	0.19	0.25	0.0075	0.0100
D	4.80	5.00	0.1890	0.1960
E	3.80	4.00	0.1500	0.1570
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.2280	0.2440
h	0.25	0.50	0.0100	0.0200
L	0.50	0.93	0.0200	0.0370
q	0°	8°	0°	8°



Recommended minimum pad layout
dimensions in inches (mm)



Conforms to JEDEC part number MS-012

Ordering Information

Part Number	Package	Packing
LVS2201N	SO-8	13" Tape and Reel, 2500 units / reel

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