

T-45-19-05

**SP8665B** 1000MHz + 10

**SP8668B** 1500MHz + 10

The SP8665/8 are asynchronous ECL counters which provide ECL compatible outputs. They feature an ECL compatible input inhibit which simplifies the design of frequency counters and other instrumentation.

#### FEATURES

- ECL Compatible Output
- AC Coupled Input
- Clock Inhibit Input

#### QUICK REFERENCE DATA

- Supply Voltage: -6.8V
- Power Consumption: 500mW
- Temperature Range: 0°C to +70°C

#### ABSOLUTE MAXIMUM RATINGS

|                           |                 |
|---------------------------|-----------------|
| Supply voltage            | -8V             |
| Output current            | 20mA            |
| Storage temperature range | -55°C to +150°C |
| Max. junction temperature | +175°C          |
| Max. clock I/P voltage    | 2.5V p-p        |

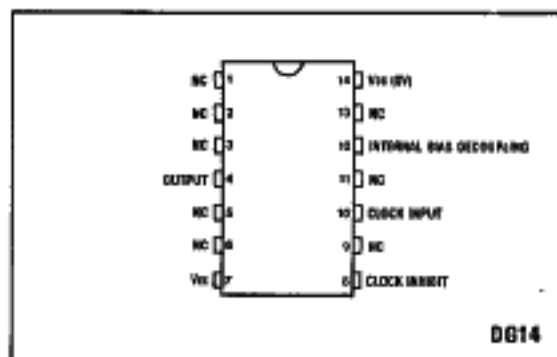


Fig. 1 Pin connections - top view

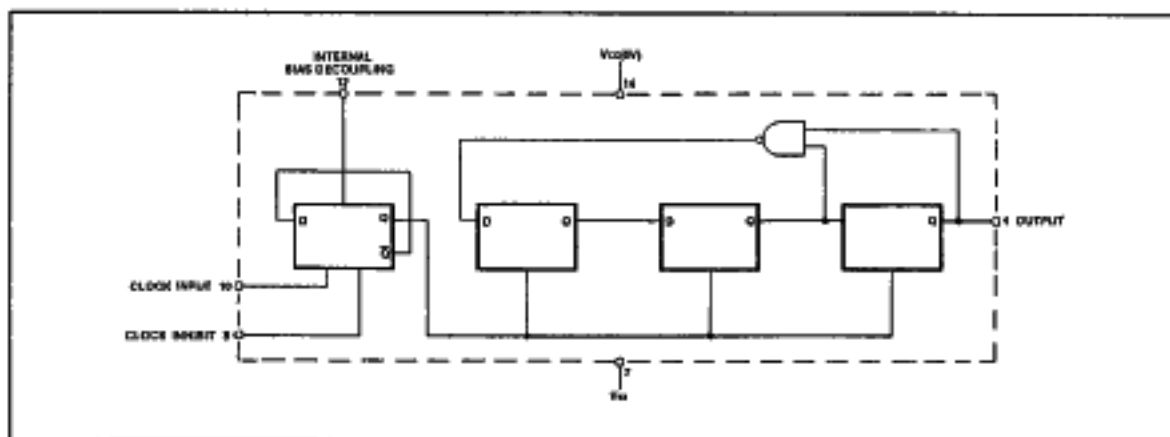


Fig. 2 Functional diagram

# ELECTRICAL CHARACTERISTICS

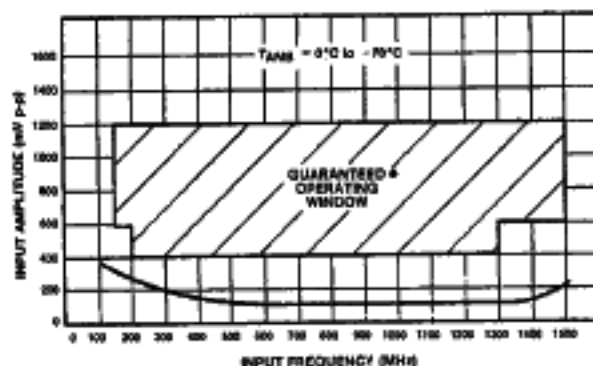
Supply voltage:  $V_{CC} = 0V$   $V_{EE} = -6.8V \pm 0.3V$   
 $T_{amb}$  (B grade) =  $0^{\circ}C$  to  $+70^{\circ}C$

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| Characteristic                       | Symbol    | Value |       | Units | Grade   | Conditions              | Notes  |
|--------------------------------------|-----------|-------|-------|-------|---------|-------------------------|--------|
|                                      |           | Min.  | Max.  |       |         |                         |        |
| Maximum frequency(sine wave I/P)     | $f_{max}$ | 1.0   |       | GHz   | SP6665B | Input = 400-1200mV p-p  | Note 5 |
|                                      |           | 1.5   |       | GHz   | SP6666B | Input = 600-1200mV p-p  | Note 5 |
| Minimum frequency(sine wave I/P)     | $f_{min}$ |       | 150   | MHz   | All     | Input = 600-1200mV p-p  | Note 6 |
| Current consumption                  | $I_{CC}$  |       | 105   | mA    | All     | $V_{EE} = -6.8V$        | Note 6 |
| Output low voltage                   | $V_{OL}$  | -1.87 | -1.5  | V     | All     | $V_{EE} = -6.8V$ (25°C) |        |
| Output high voltage                  | $V_{OH}$  | -0.87 | -0.7  | V     | All     | $V_{EE} = -6.8V$ (25°C) |        |
| Minimum output swing                 | $V_{OUT}$ | 500   |       | mV    | All     |                         | Note 5 |
| Clock inhibit high threshold voltage | $V_{INH}$ | -0.96 |       | V     | All     | $V_{EE} = -6.8V$ (25°C) |        |
| Clock inhibit low threshold voltage  | $V_{INL}$ |       | -1.62 | V     | All     | $V_{EE} = -6.8V$ (25°C) |        |

## NOTES

1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.8.
3. The temperature coefficient of  $V_{OH} = +1.3mV/^{\circ}C$  and  $V_{OL} = +0.5mV/^{\circ}C$  but these are not tested.
4. The temperature coefficient of  $V_{INH} = +0.8mV/^{\circ}C$  but this is not tested.
5. Tested at 25°C and 70°C only.
6. Tested at 25°C only.



\* Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic SP6658. The SP6665 operating window is similar except for the maximum operating frequency

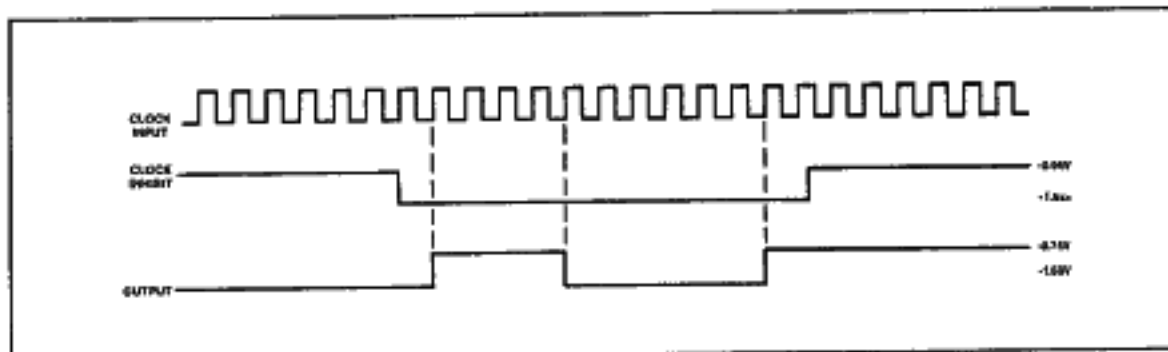


Fig.4 Timing diagram(N.B. output waveform is asymmetric)

## OPERATING NOTES

1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to  $V_{EE}$  (i.e. Pin 10 to Pin 7). This will reduce the input sensitivity by approximately 100mV.
3. The clock inhibit input is compatible with standard ECL III/10K using a common 0V. A 6k pulldown resistor is included on the chip. The input should be left open to DC

when not in use, but should be bypassed for RF signals with a 1nF capacitor to ensure maximum noise immunity.

4. Input impedance is a function of frequency. See Fig. 5.
5. The emitter follower output includes an internal 3k pulldown resistor and is compatible with ECL II, but can be interfaced with ECL III/10K by the inclusion of two resistors. See Fig. 7.

6. Note that all components should be suitable for the frequency in use.

7. The circuit will operate to DC but the input slewrate must be 200V/ $\mu$ s or greater.

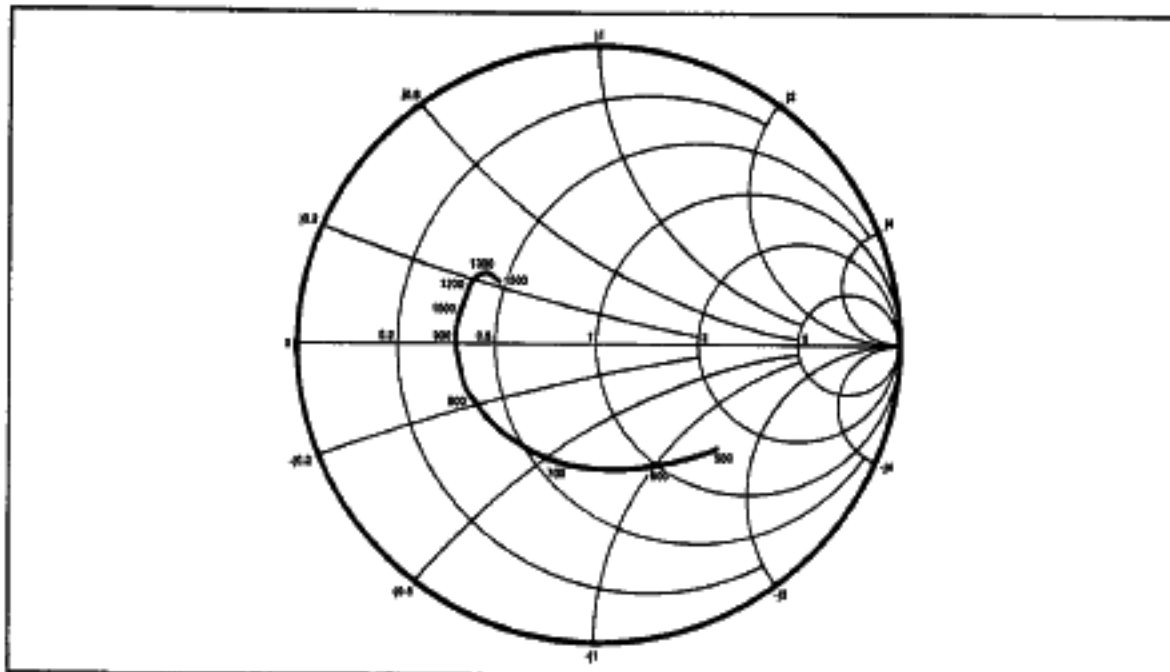


Fig.5 Typical Input Impedance. Test conditions: supply voltage -6.8V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

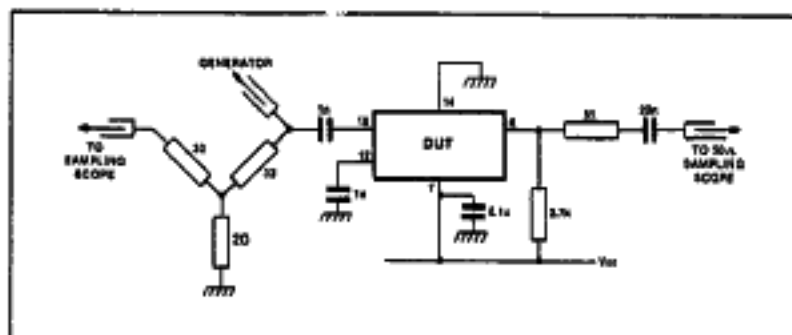


Fig.6 Test circuit

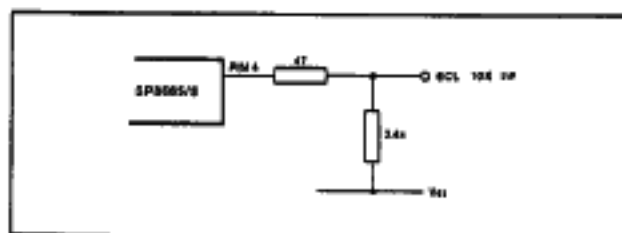


Fig.7 SP8885/8 to ECL 10K interface

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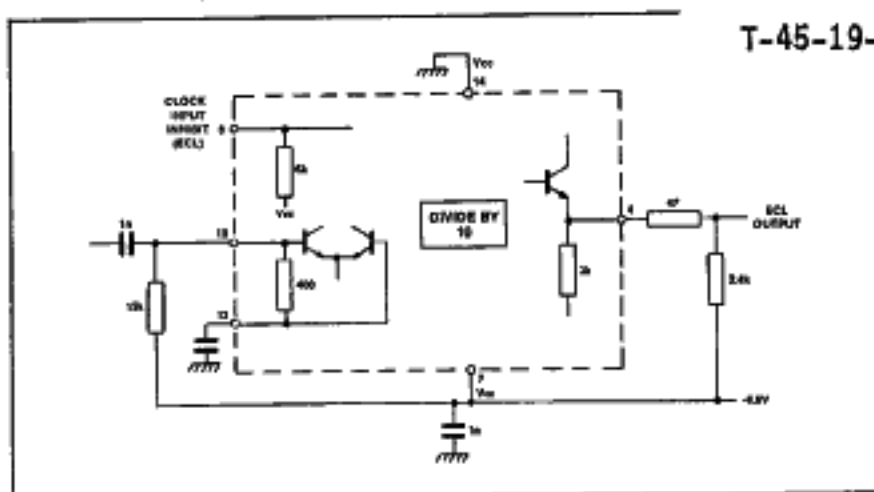


Fig.8 Typical application showing interfacing