



SPDS106A

Voice Engine

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Version 1.0

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VOICE ENGINE

1. GENERAL DESCRIPTION

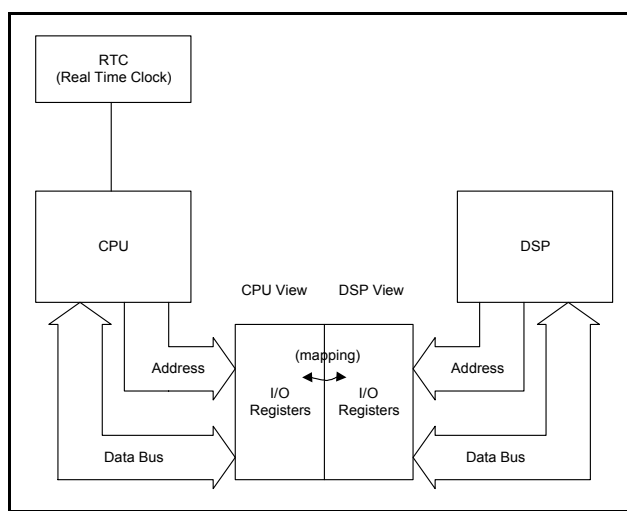
SPDS106A, a single chip contains an 8-bit RISC microprocessor (CPU) and a 16-bit digital signal processor (DSP), is applied for constituting long duration audio applications. The CPU transmits commands and data to DSP by the means of memory-mapped (parallel interface). The CPU employs 23 general I/Os to access external devices. The 256K x 8 ROM hold the system control program, audio processing program and audio data. The DSP receives the commands and data from CPU and finally runs the decompressing algorithm. Both CPU and DSP share a PWM output for audio.

2. FEATURES

- 8-bit RISC microprocessor (CPU) with 256K bytes ROM for program and audio data.
- CPU with 128 working RAM
- 23 general I/Os
- 7 interrupt sources
- Key change wake up
- 2Hz, 1sec, 2sec, 10sec, 30sec, 1min, 2min or 4min programmable RTC wake up and interrupt.
- Shared D/A converter supports three PWM modes:
 - 10-bit Push-Pull mode
 - 10-bit Single-pin double-ended mode
 - 9-bit single-pin single-ended mode
- Single clock: Crystal OSC or ROSC 20MHz to DSP and 20MHz divided by N to CPU, where $N = 2, 4, 6, 8, 10, 12, 14$
- Volume control function
- Serial interface I/O
- CPU with two 12-bit timers/counters
- Low voltage reset
- Sleep mode for power saving
- Multi-phase for remote control application
- Max. CPU clock: 5.0MHz @ 2.4V - 5.5V
- SACM_S480, SACM_S720, SACM_S240, SACM_A2400/A3200 and FM synthesizer

3. BLOCK DIAGRAM

The integration method of CPU and DSP is using a shared memory block in between two processors and each register or I/O in CPU will correspond to specified register in DSP. The following diagram simply describes the access between CPU and DSP.



4. APPLICATION FIELDS

- Long Duration Audio System
- Intelligent Talking Toys
- Talking Instructions
- Kid-Story Books
- And relevant applications

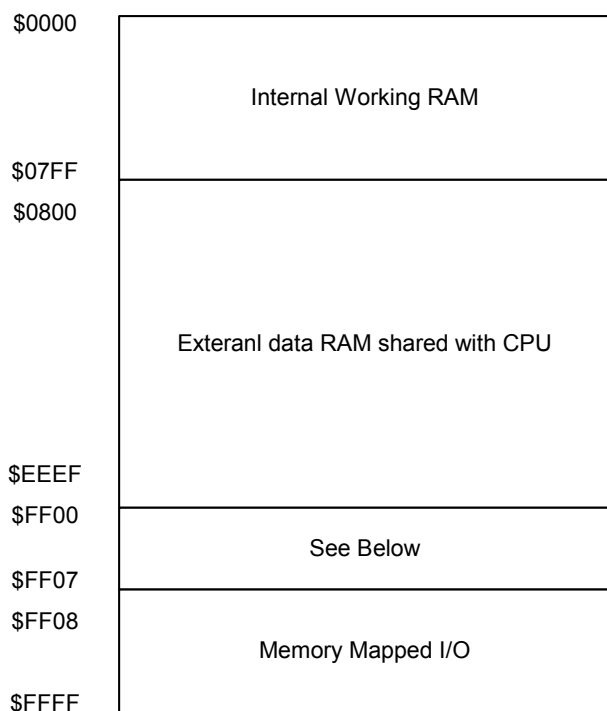
5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
VDD	8, 16	I	Power for chip except shared PWM (Two VDD pins)
VSS	7, 23	I	Ground for chip except shared PWM (Two VSS pins)
XI/R	21	I	X'TAL OSC input or ROSC
XO	22	O	X'TAL OSC output
AUDP	2	O	Push-Pull and single pin PWM output (shared)
AUDN	4	O	Push-Pull PWM output (shared)
TEST1	24	I	Test input, internal pull low, NC
TEST2	19	I	Test input, internal pull low, NC
RESET	20	I	Reset input (Active low), internal pull high
IOA3 - 0	37 - 40	I/O	Programmable I/O pin
IOB3 - 0	33 - 36	I/O	Programmable I/O pin
IOC6 - 0	9 - 15	I/O	Programmable I/O pin
IOD7 - 0	25 - 32	I/O	Programmable I/O pin
VDD1	1, 5	I	Power for AUDP and AUDN (Two VDD1 pins)
VSS1	3	I	Ground for AUDP and AUDN
TEST3	6	O	TEST pin, NC
X32I	18	I	32768Hz X'TAL input (for RTC function)
X32O	17	O	32768Hz X'TAL output (for RTC function)

6. FUNCTIONAL DESCRIPTIONS

6.1. Data RAM Mapping

6.1.1. DSP



FF00: PWM_WR

FF01: PWM_SET

FF02: TM1_WR & TM1_RD

FF03: TM2_WR & TM2_RD

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6.2. PWM

SPDS106A offers one set of PWM output for CPU and DSP. Three PWM modes include Push-Pull, Single-pin Double-ended and Single-pin Single-ended.

6.3. SPC Mapping

*I/O PORT:

- PORT IOA \$0002
- IOB \$0003
- IOC \$0004
- IOD \$0005
- I/O CONFIG \$0000
- \$0001

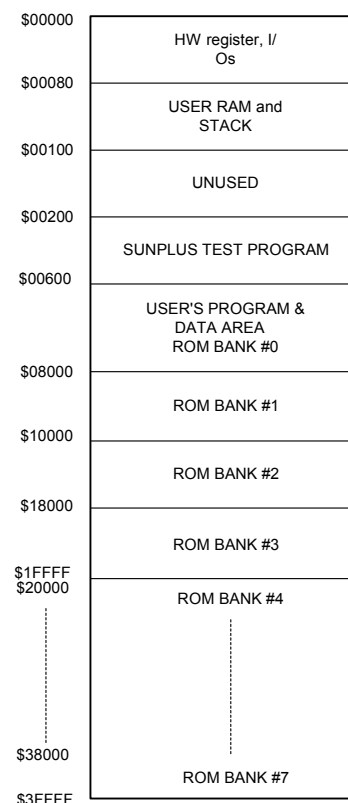
*NMI SOURCE:

- INTA (from TIMER A)

*INT SOURCE:

- INTA (from TIMER A)
- INTB (from TIMER B)
- RTC
- CPU CLK / 1024
- CPU CLK / 8192
- CPU CLK / 65536
- EXT INT

*MEMORY MAP (From ROM view)



6.4. RTC (Real Time Clock)

Some applications require a real time clock for time tracking. SPDS106A provides a RTC based on 2Hz, 1sec, 2sec, 10sec, 30sec, 1min, 2min or 4min programmable frequency. The SPDS106A provides programmable 1/2-second, 1-second, 2-second, 10-second, 30-second, 1-minute, 2-minute and 4-minute wake-up sources, the system wakes up every specified wake-up source and users can use it as the time tracking resource. In addition, SPDS106A supports 32768 OSC strong mode and auto mode. With strong mode, 32768 OSC always runs in the highest power. With auto mode, the first 2-second is strong mode and then switch to weak mode to save power.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

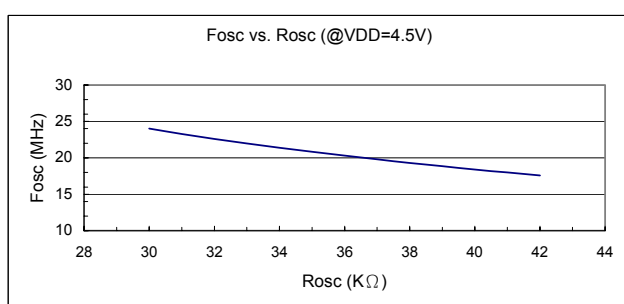
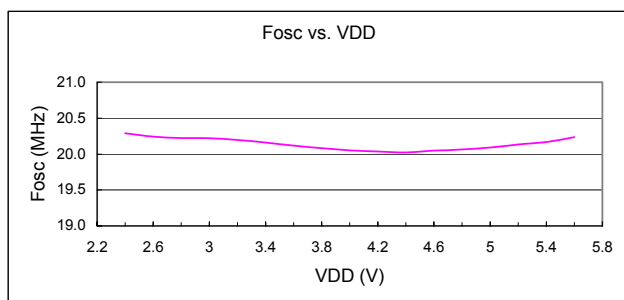
Rating	Symbol	Value		Unit
Supply Voltage	VDD	+0.0	to <7.0	V
Input voltage	V _{IN}	-0.3	to VDD +0.3	V
Operating Temperature	T _A	0	to 55	°C
Storage Temperature	T _{STG}	-55	to 125	°C

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

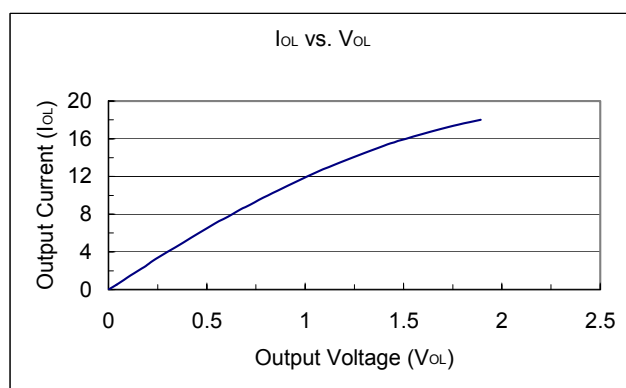
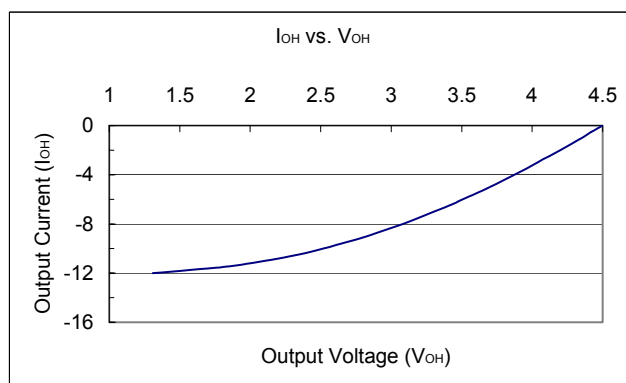
7.2. DC Characteristics (VDD = 4.5V, T_A = 25°C)

Characteristics	Symbol	Limit			Unit	Test condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	5.5	V	
Operating Current	I _{OP}	-	17	-	mA	F _{OSC} = 20MHz @ 4.5V, no load
Standby Current	I _{STB}	-	-	2.0	μA	VDD = 4.5V
Oscillation Resistor	R _{OSC}	-	36.5	-	KΩ	VDD = 4.5V, F _{SYS} = 20MHz
System Clock	F _{SYS}	-	20	-	MHz	
CPU Clock	F _{CPU}	1.4	-	5.0	MHz	
Input High Voltage	V _{IH}	0.7*VDD	-	VDD	V	
Input Low Voltage	V _{IL}	VSS	-	0.2*VDD	V	
Output High Current (IOA - IOD)	I _{OH}	-	-3.0	-	mA	VDD = 4.5V V _{OH} = 4.0V
Output Low Current (IOA - IOD)	I _{OL}	-	7.5	-	mA	VDD = 4.5V V _{OH} = 0.6V
Input Pull High Resistor (IOA)	R _{INH}	-	64	-	KΩ	VDD = 4.5V V _{IN} = 0.7*VDD = 3.15V
Input Pull Low Resistor (IOD)	R _{INL}	-	24	-	KΩ	VDD = 4.5V V _{IN} = 0.2*VDD = 0.9V

7.3. The Relationship between the R_{OSC} and the System Clock (F_{OSC})

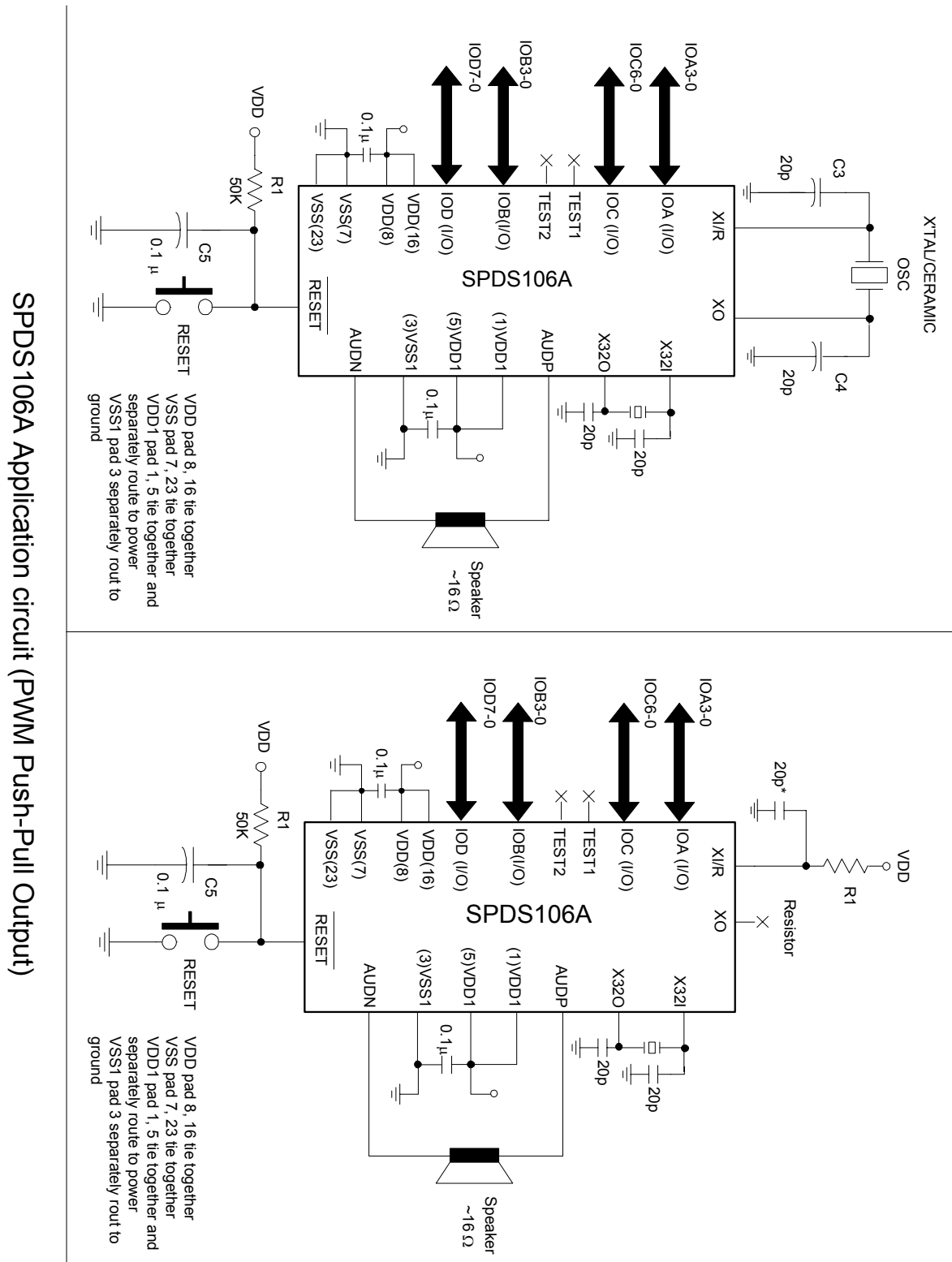


7.4. IOA, IOB, IOC, IOD I/O Driving Characteristic



8. APPLICATION CIRCUITS

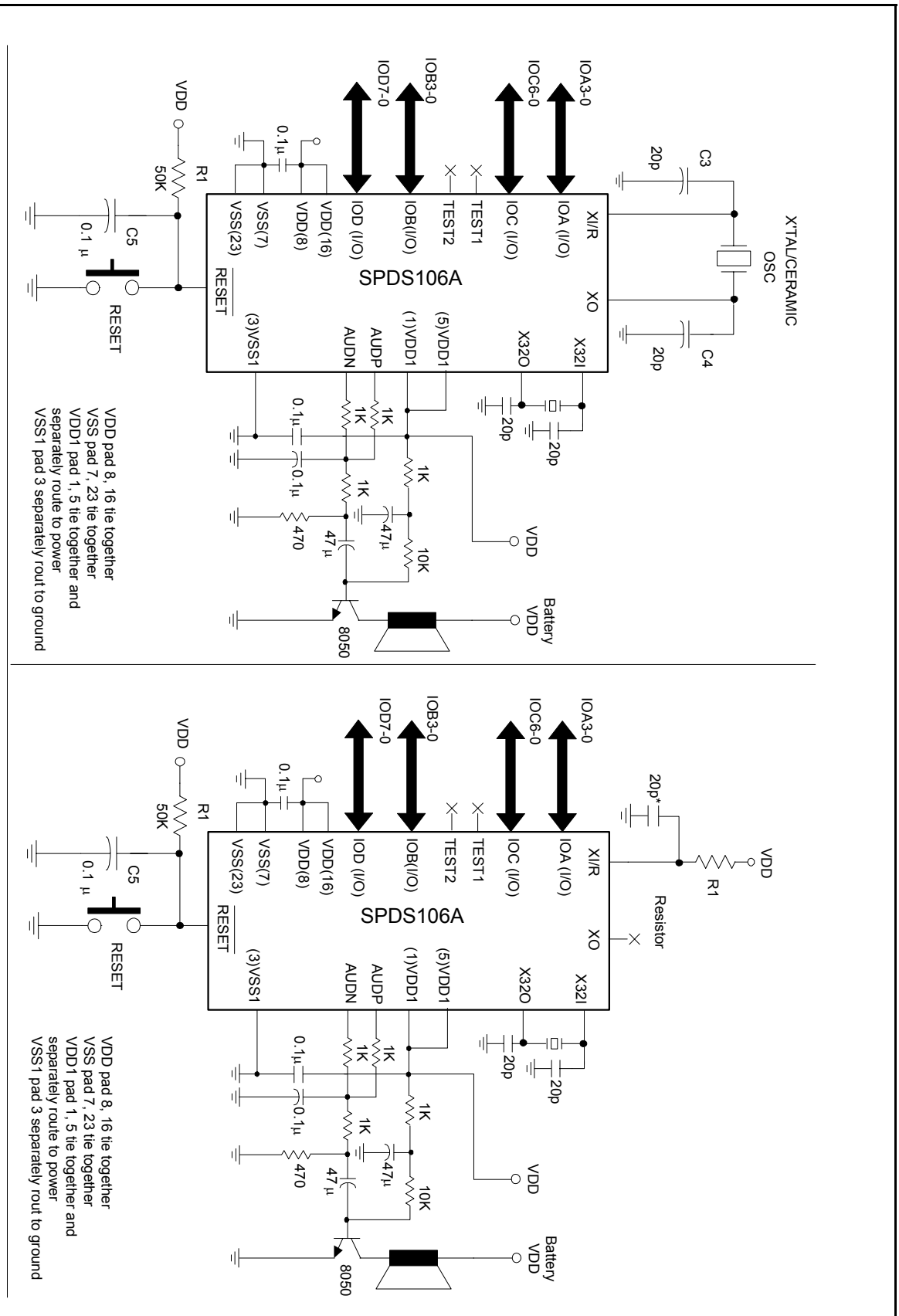
8.1. Application Circuit - (1)



Note: Capacitor may be increased if necessary. (Cmax = 120p)

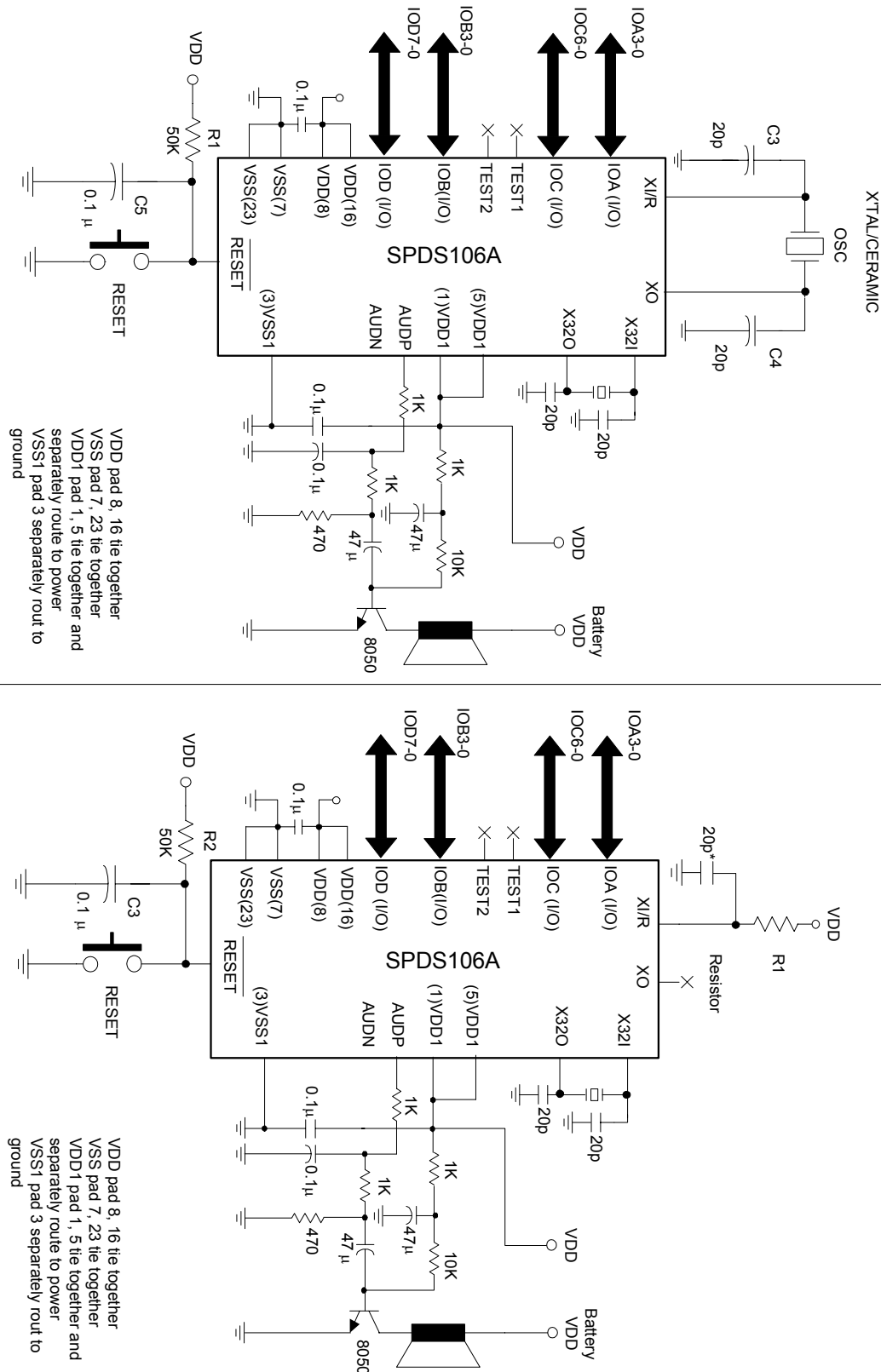
8.2. Application Circuit - (2)

SPDS106A single-pin double-ended mode application circuit



Note: *Capacitor may be increased if necessary. (Cmax = 120p)

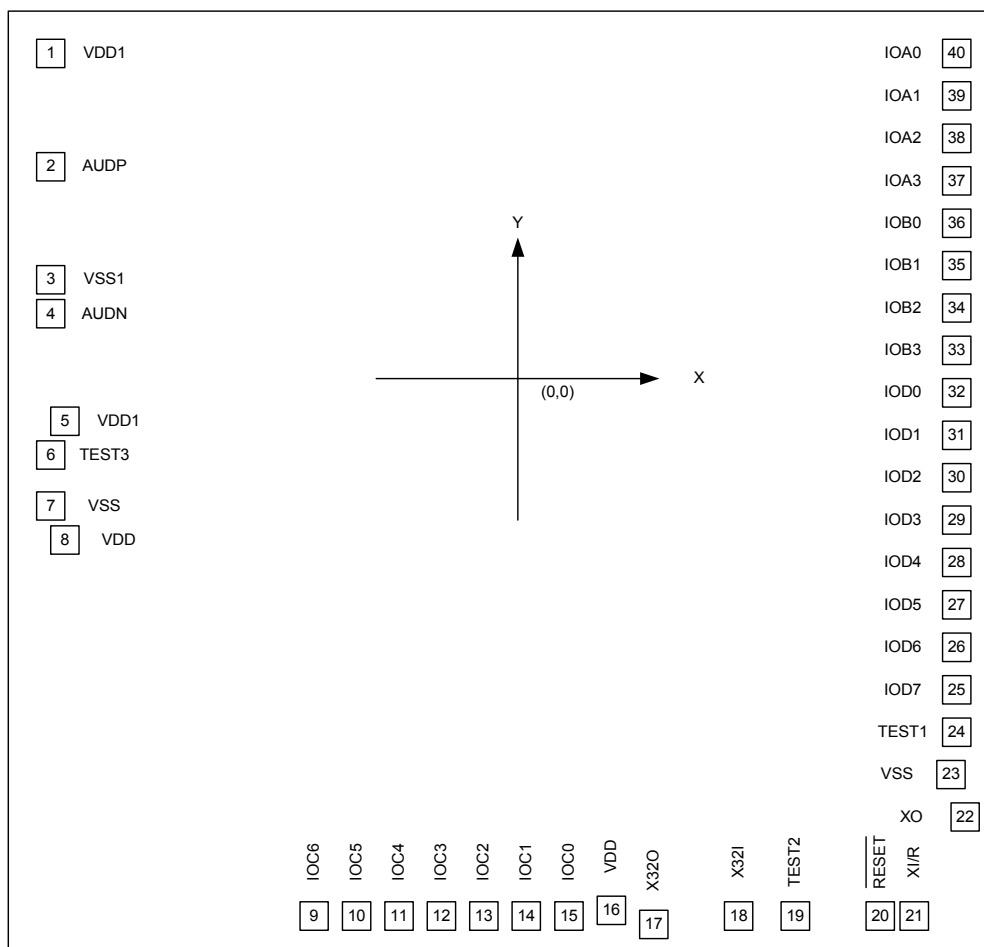
8.3. Application Circuit - (3)



Note: *Capacitor may be increased if necessary. (Cmax = 120p)

9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip Size: 3160μm x 3510μm

This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

Note3: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
SPDS106A-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (A = A - Z).

9.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	VDD1	-1360	1573	21	XI/R	1216	-1535
2	AUDP	-1378	1123	22	XO	1389	-1178
3	VSS1	-1378	708	23	VSS	1370	-1047
4	AUDN	-1378	583	24	TEST1	1386	-917
5	VDD1	-1360	133	25	IOD7	1386	-766
6	TEST3	-1378	7	26	IOD6	1386	-607
7	VSS	-1378	-156	27	IOD5	1386	-456
8	VDD	-1360	-276	28	IOD4	1386	-297
9	IOC6	-857	-1515	29	IOD3	1386	-146
10	IOC5	-706	-1518	30	IOD2	1386	13
11	IOC4	-552	-1517	31	IOD1	1386	164
12	IOC3	-401	-1517	32	IOD0	1386	323
13	IOC2	-246	-1517	33	IOB3	1386	474
14	IOC1	-94	-1517	34	IOB2	1386	632
15	IOC0	61	-1517	35	IOB1	1386	784
16	VDD	214	-1486	36	IOB0	1386	942
17	X32O	384	-1534	37	IOA3	1386	1094
18	X32I	639	-1534	38	IOA2	1386	1249
19	TEST2	849	-1535	39	IOA1	1386	1400
20	RESET	1096	-1536	40	IOA0	1386	1555

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
JAN. 29, 2000	0.1	Original	
SEP. 22, 2000	0.2	1. 4 interrupt source -> 7 interrupt sources 2. Delete Watchdog timer 3. CPU with 12-bit timers -> CPU with 12-bit timers/counters 4. Operating voltage 2.4V - 5.5V -> 3.6V -> 5.5V 5. Add Volume control function, serial interface I/O, Low voltage reset function	
MAY. 15, 2001	0.3	1. Add PIN#5 to VDD1. 2. Add "Note3: The 0.1μF capacitor between VDD and VSS ..." 3. Add " <u>REVISION HISTORY</u> " 4. Renew to a new document format	3 9 11
SEP. 05, 2001	1.0	1. Delete " <u>PRELIMINARY</u> " 2. Modify operating voltage: 3.6V - 5.5V -> 2.4V - 5.5V 2. Connect VDD1 to VDD2, and indicate the pin number. 3. Connect VSS1 to VSS2, and indicate the pin number. 4. Origin: Each VDD (total of two) and VSS (total of two) are connected to 0.1μF capacitors individually. Modification: Connect two VDD together and similarly, connect two VSS and indicate the pin number. The number of capacitor is reduced to one. 5. Disconnet the VDD and speaker where is reindicated as "Battery VDD". 6. Add note in all application circuits 7. Correct chip size 8. Add Note1 in the " <u>9.1 PAD Assignment</u> " 9. Renew to a new document format	1, 6 8 - 10 8 - 10 8 - 10 8 - 10 8 - 10 11 11