



GENERAL DESCRIPTION

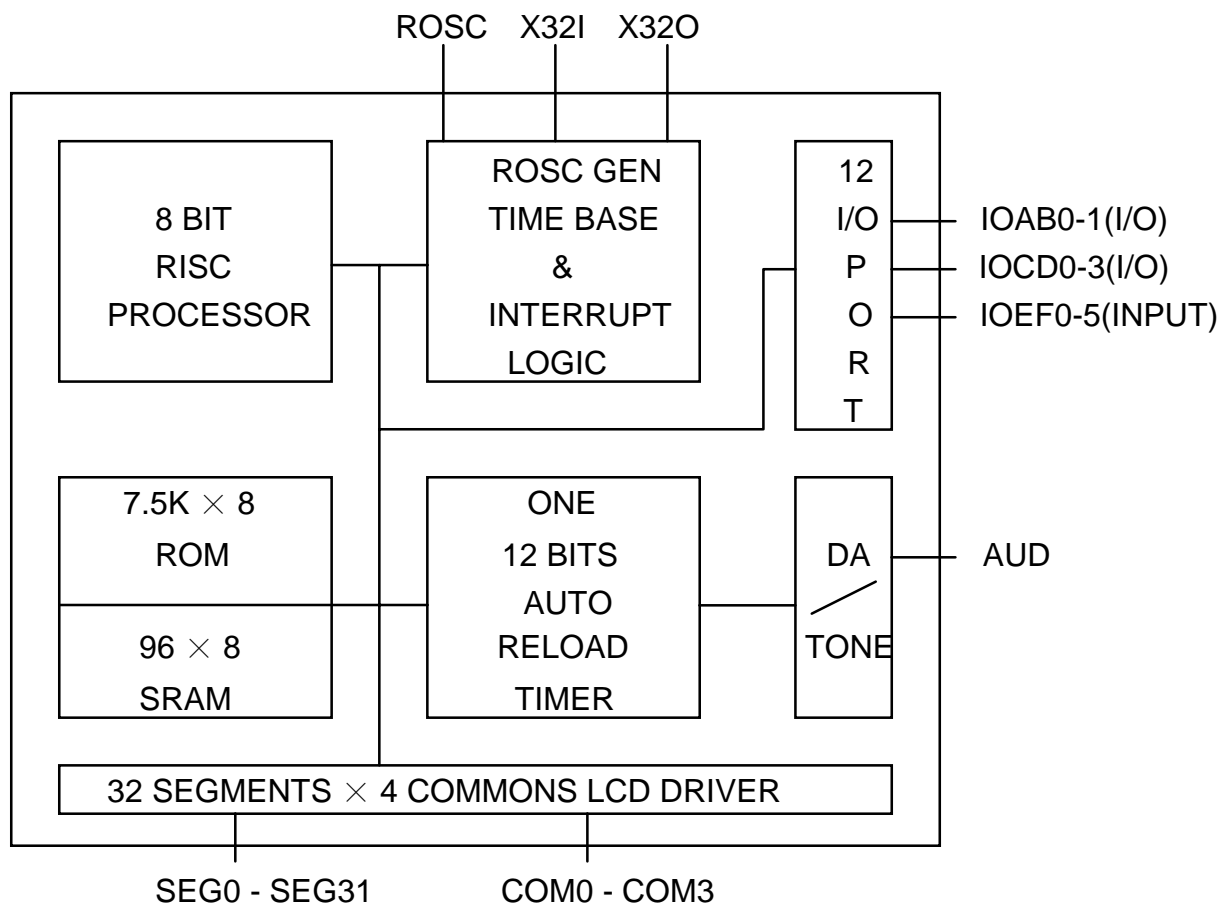
The SPL10A1 is a CMOS 8-bit single chip micro-controller which contains LCD drivers, ROM, SRAM, I/O, timer/counter and audio output on a single chip.

The SPL10A1 is designed to drive LCD directly and perform efficient controller function as well as arithmetic function. With the on chip crystal oscillator, the clock function is easily realized. For power saving, a software controllable standby switch is also built-in. The SPL10A1 is widely used in electronic products requiring very low power operation, for example, multi-function watch, calendar, calculator, thermometer or LCD game with audio output.

FEATURES

- CPU: 8-bit SUNPLUS RISC CPU
- Operating voltage: 2.4V to 5.5V
- Maximum CPU clock: 2 MHz @ 3V
- ROM capacity: 7.5 K x 8 bits
- RAM capacity: 96 x 8 bits
- Direct Driver for LCD : 4 Commons X 32 Segments
(1/2, 1/3 bias, 1/2, 1/3, 1/4 duty)
- Input Port : 6 input pins with key wakeup function
with 4 different configurations (mask option)
- I/O Port : 2 general I/O pins and 4 special I/O pins
that can implement thermometer and..
- Timer/Counter: one 12-bit timer/counter
- 6 Interrupt sources : External Interrupt
Timer Interrupt
2 KHz Interrupt
LCD Service Interrupt (in LCD share mode)
128 Hz Interrupt
2 Hz Interrupt
- Dual Clock System : One built-in RC oscillator (only one resistor is needed)
for CPU and one built-in crystal oscillator or RC
oscillator (mask option) for LCD scanning.
- Audio or Tone Output : One 7-bit DA single tone melody or speech that can
drive transistor or Tone output that can drive buzzer.
- Low Operating Current : Typical current < 3 μ A @ 3V for timepiece product

BLOCK DIAGRAM



PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
SEG0 - SEG31	O	LCD driver segment output
COM0 - COM3	O	LCD driver common output
IOAB0 - IOAB1	I/O	I/O port
IOEF0 - IOEF5	I	INPUT port (also for key wake input)
IOCD0 - IOCD3	I/O	I/O port
ROSC	I	R-osc input, connect to VDD through resistor
RESET	I	System reset input
AUD	O	Current DA output /Tone output
X32I	I	32.768KHz crystal input/R oscillator input (provide LCD frequency)
X32O	O	32.768KHz crystal output
TEST	I	Test input
VDD	I	Power input
VSS	I	Ground input
VDD1	I	Inputs for setting LCD bias
VDD2	I	Inputs for setting LCD bias
CUP1	I	Input for maintaining 1/3 Bias LCD
CUP2	I	Input for maintaining 1/3 Bias LCD

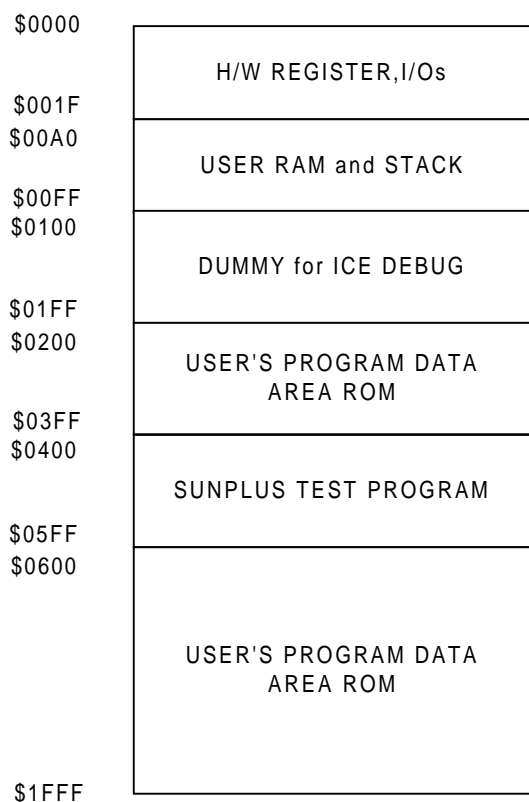
FUNCTION DESCRIPTION
■ROM

The SPL10A1 has 7.5K bytes ROM size. The user can has 7K bytes for program and data. The other 0.5K bytes are for SUPLUS internal test use. The ROM address is from \$0200 to \$1FFF.

■RAM

The SPL10A1 has 96 bytes RAM size. This area is all for data storage. The RAM address is from \$00A0 to \$00FF.

■ MEMORY and I/O MAP

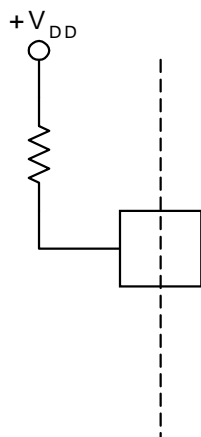


■ OSCILLATORS

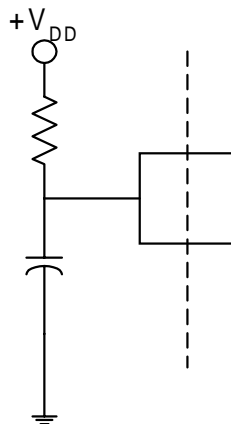
The SPL10A1 has dual clock system that one is for the CPU and system and the other is for the LCD scanning and interrupt sources.

1. R Oscillator for the CPU and system clock

1.1 Normal case

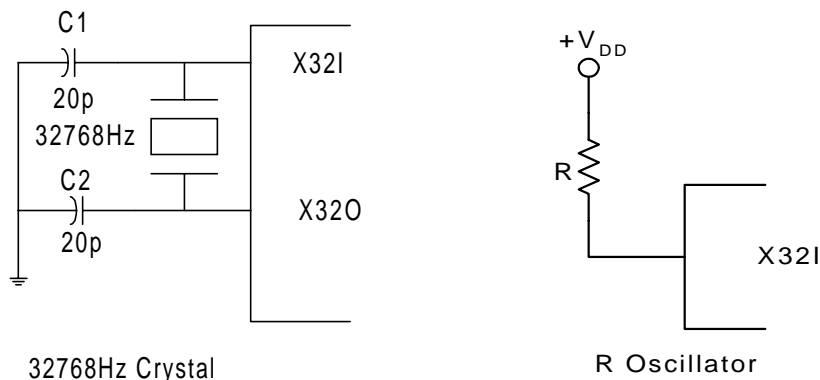


1.2 Noise Environment



Note: Length of the wiring for ROSC pin should be minimized because the oscillator frequency varies due to coupling from other signal lines.

2. 32768Hz crystal oscillator or R oscillator (mask option) for LCD scanning and interrupt sources (2 KHz, LCDL for LCD service, 128 Hz, 2Hz). It is suggested to enable 32768Hz crystal in strong mode for a few seconds and then switch to weak mode when reset occurs.



Note: Length of the wiring for X32I and X32O should be as short as possible.

■STOP CLOCK MODE

The SPL10A1 supports the power saving mode for those applications needed very low standby current. The user can simply enable the wake-up sources then stop the CPU clock by writing the STOP CLOCK register (\$09). The CPU will go to stand-by and the RAM and I/O remains their previous states until wake-up. There are three sources of wake-up in this chip, PORT IOEF wake-up, TIMER 0 wake-up and 2 Hz wake-up. After the chip being waken up, the internal CPU will go to the RESET state the RAM and I/O are not affected by the wake-up reset. The standby current of timepiece product typically is less than 3 μA @3V by using this mode and 32768Hz clock source in weak mode.

For non-timepiece products, 32768Hz crystal driver or R oscillator (mask option) that generates the 32768Hz clock source also can be turned off, then the whole chip stops. The standby current of the SPL10A1 is less than 1 μA @3V. In this mode, IOEF port can be used to wake up this chip.

■TIMER/COUNTER

The SPL10A1 contains one 12-bit timer/counter, TM0. In timer mode, TM0 is reloadable up-counter. When timer overflows from 0FFF to 0000, the carry signal will generate the INTERRUPT signal if the corresponding bit is enabled in INT ENABLE register (\$0D), and the timer will be auto reloaded to the user's setup value and upcount again. If TM0 being specified as a counter, the user may reset the counter by loading 0 into register \$14 and \$1C. After the counter being activated, the count value can also be read from above registers on-the-fly, the read instruction will not affect the counter's value or reset it.

The clock source of the timer/counter are selectable as the following:

TIMER/COUNTER		ADDR.	CLOCK SOURCE
TM0	12 BIT TIMER	\$0014 \$001C	CPU CLOCK (T) or T/4
	12 BIT COUNTER	\$0014 \$001C	T/128, T/256, T/2048 or EXT CLK
MODE SELECT REGISTER		\$000B	Select TM0 timer or counter
TIMER CLOCK SELECTOR		\$001C	Select T or T/4

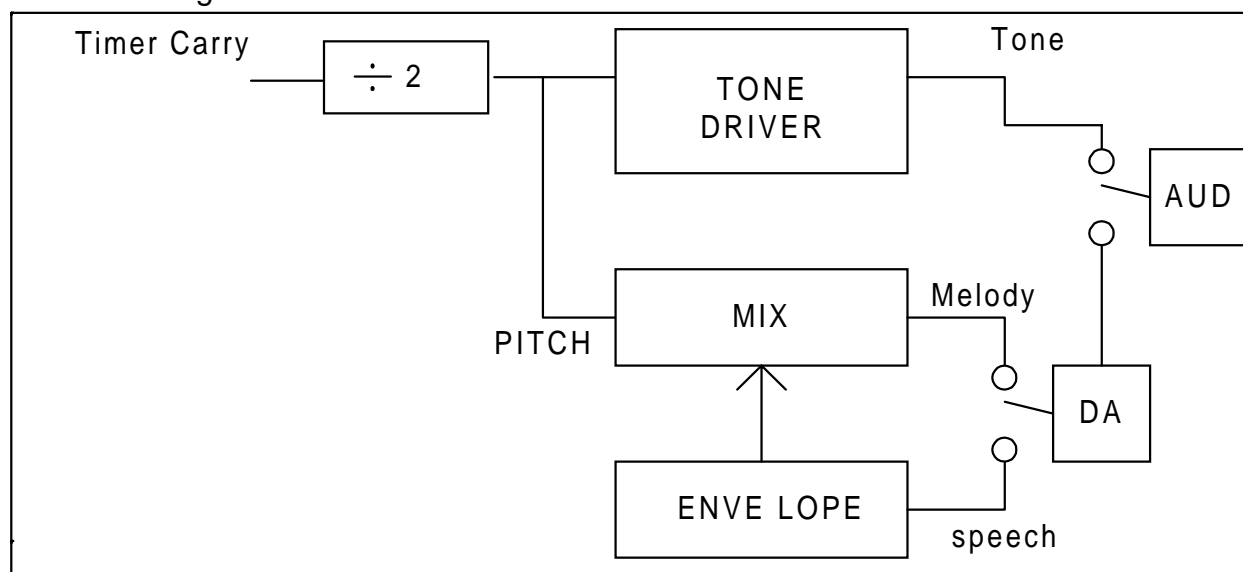
■INTERRUPTS

The SPL10A1 has six interrupt sources. They are INT0 (interrupt fromTIMER 0), 2 KHz INT, LCDL INT (LCD service in share mode, due to LCD registers is shared with the TIMER/COUNTER), 128 Hz INT, EXT INT (external INTERRUPT from IOCD1), 2 Hz INT. The 2KHz INT, LCDL INT (256 Hz in 1/3, 1/4 bias;128 Hz in 128 Hz), 128 Hz INT, 2Hz INT, all are divided from 32768 Hz Crystal Oscillator.

■AUDIO (MELODY/SPEECH) / TONE OUTPUT

The SPL10A1 provides both speech and single tone melody output in current DA type that can drive SPEAKER through transistor. Also, the SPL10A1 provides TONE output that can directly drive BUZZER. The two modes, current DA and tone, share the same AUD pin. In current DA mode, it should smoothly switch current DA output current to zero by using speech mode to reduce noise to turn off current DA. The current DA should be turned off when not used due to the current consumption. The TONE output is a full-swing (VDD and VSS) signal and its frequency source is the frequency of TIMER Carry divided by 2.

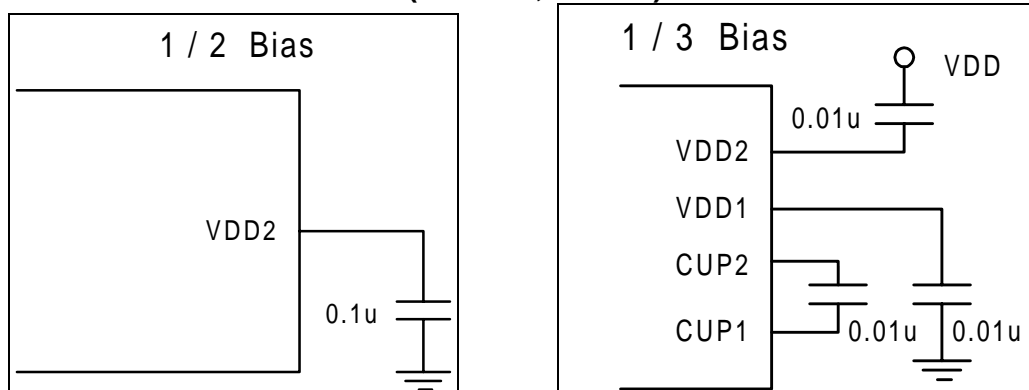
The block diagram is shown as below:



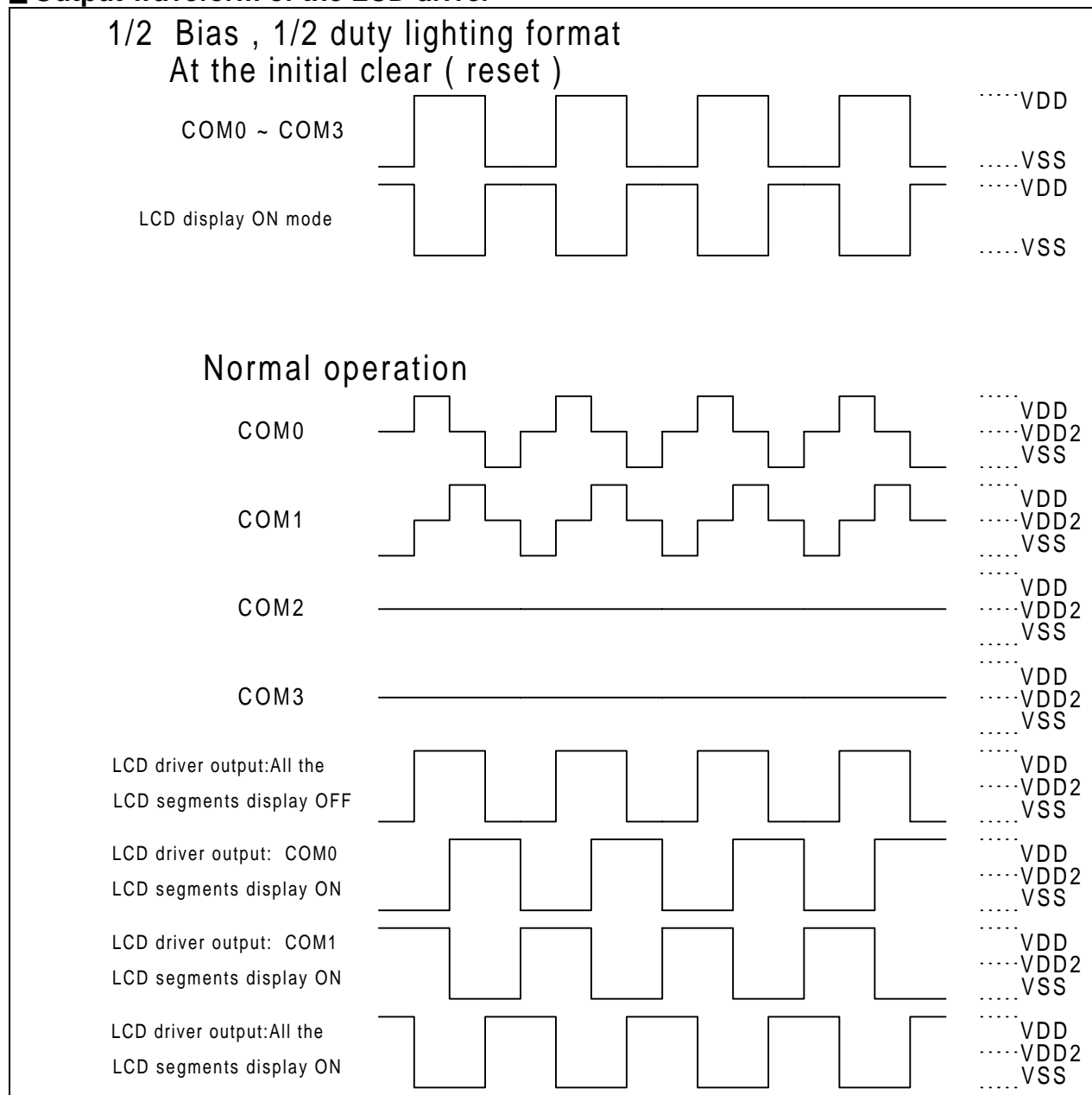
■ LIQUID CRYSTAL DISPLAY

The SPL10A1 can directly drive the liquid crystal display (LCD) panel of 1/2 duty, 1/3 duty, and 1/4 duty with 1/2 bias or 1/3 bias. It has 4 commons and 32 segments signal pins. In share mode (Timer/Counter is used), the LCD being refresh by LCDL interrupt. The INT routine will read the number of common which is under serving, and send the next common's pattern to LCD port (\$10 - \$13) from RAM buffer. If the Timer/the Counter is not used, hardware mechanism will auto refresh the LCD after writing OPTION register (\$1F).

The power connections for LCD (1/2 bias, 1/3bias) are shown as below:

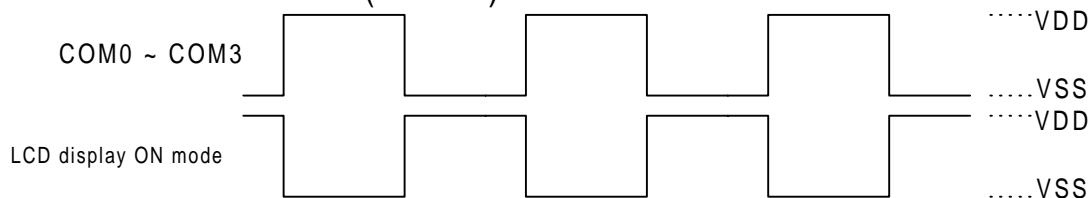


■ Output waveform of the LCD driver

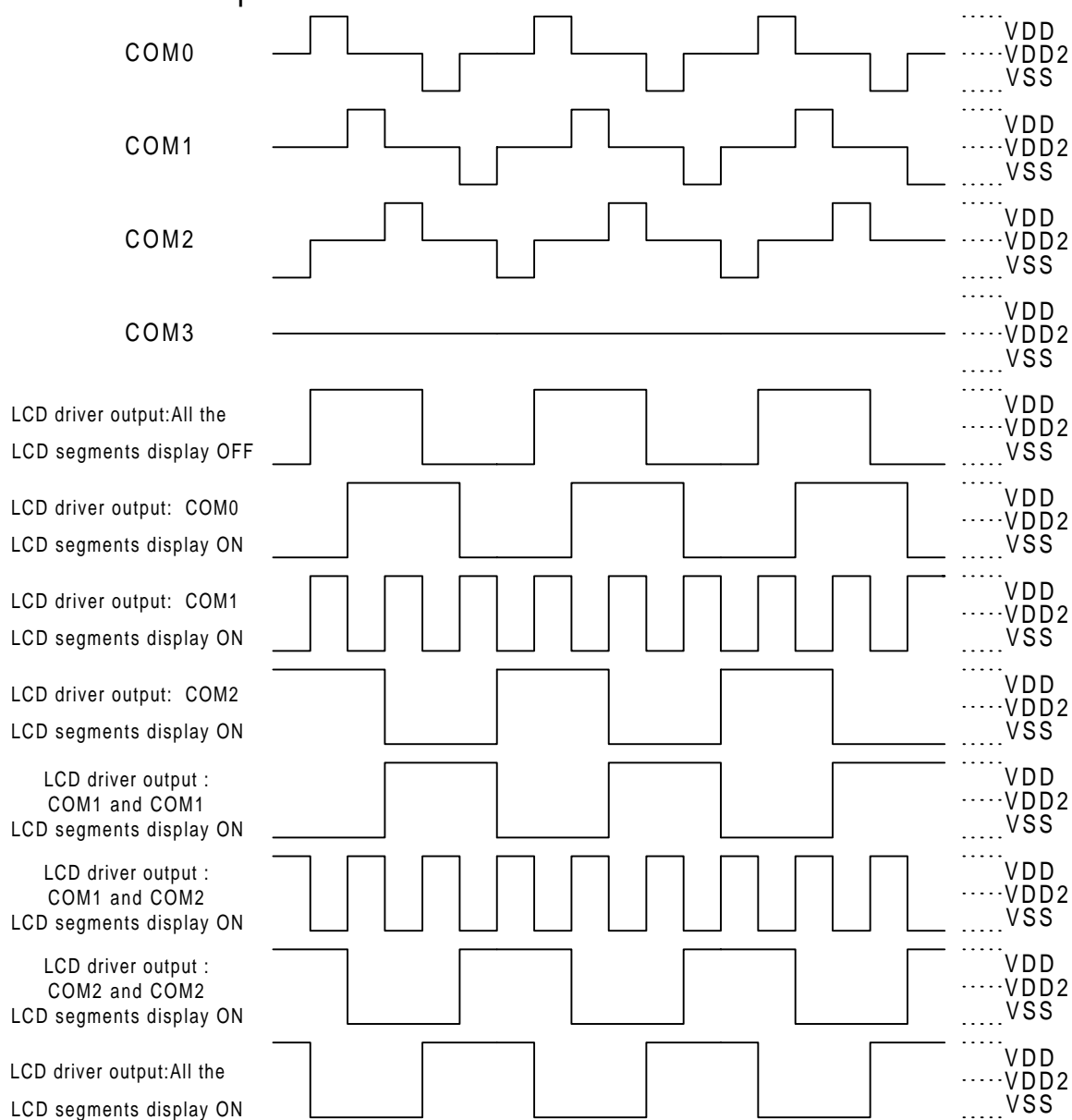




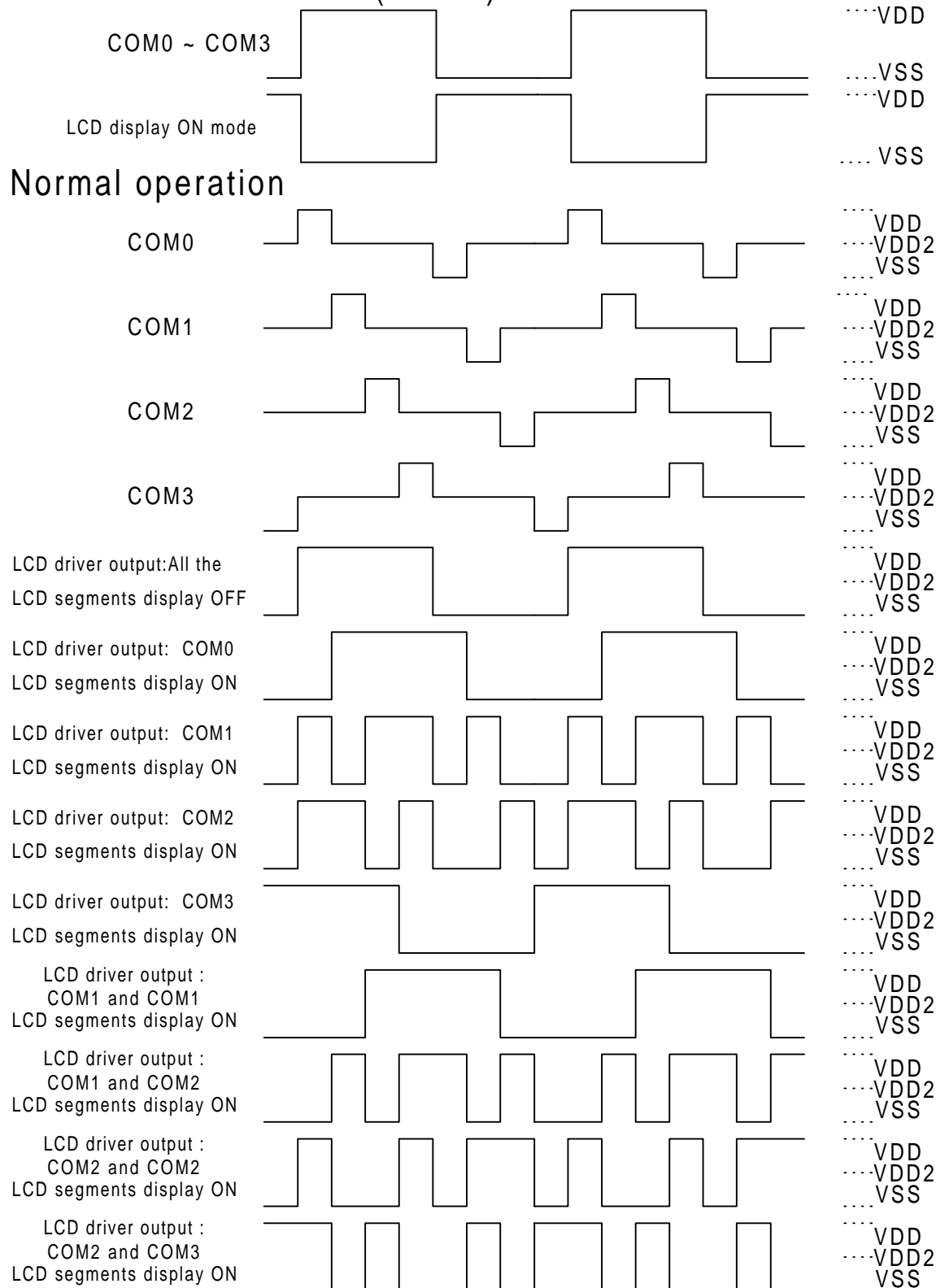
1/2 Bias , 1/3 duty lighting format
At the initial clear (reset)



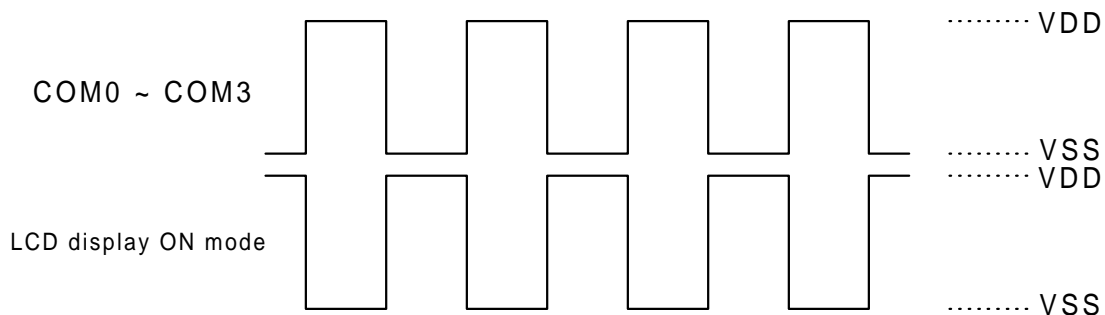
Normal operation



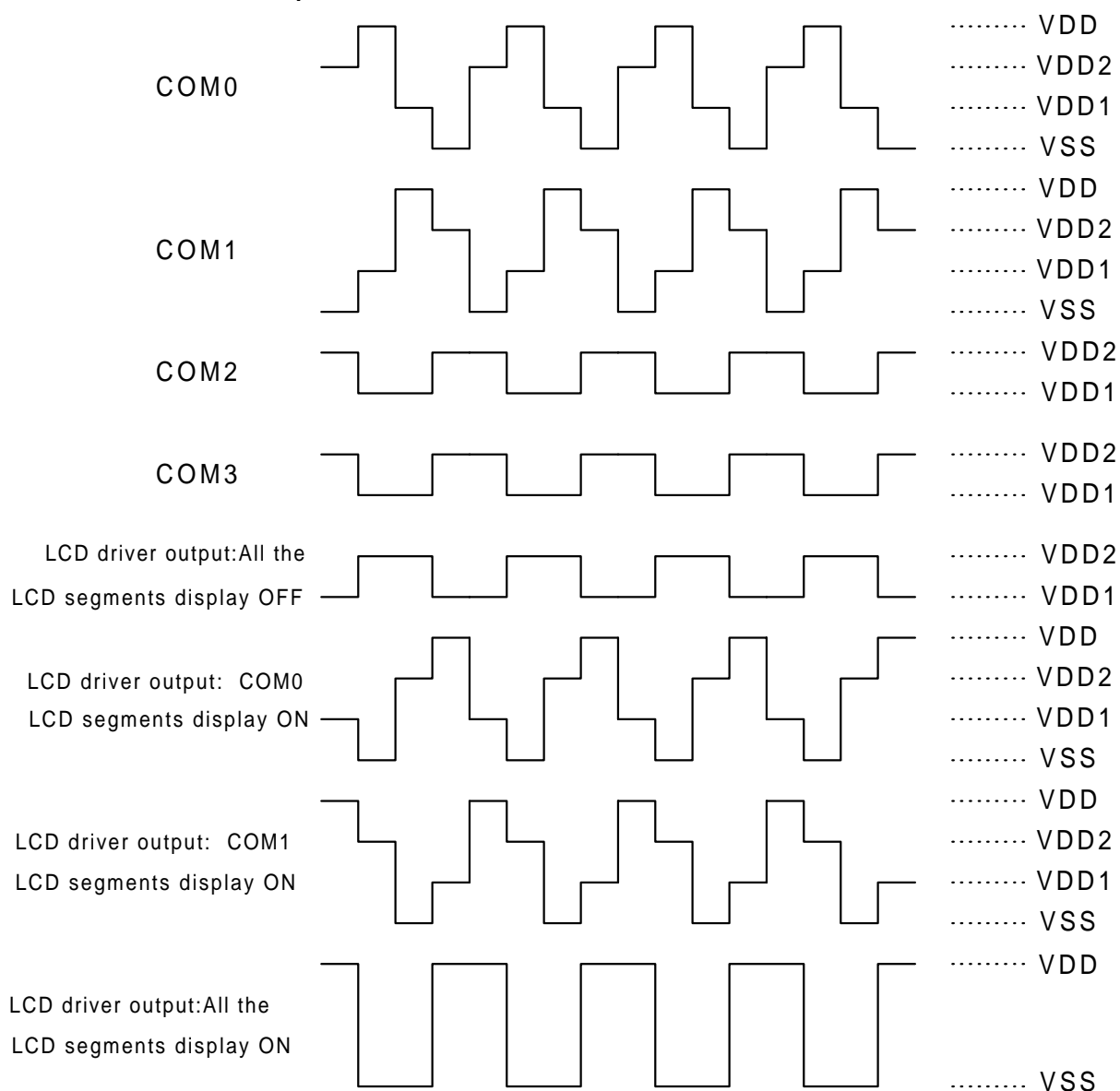
1/2 Bias , 1/4 duty lighting format
At the initial clear (reset)



1/3 Bias , 1/2 duty lighting format
At the initial clear (reset)



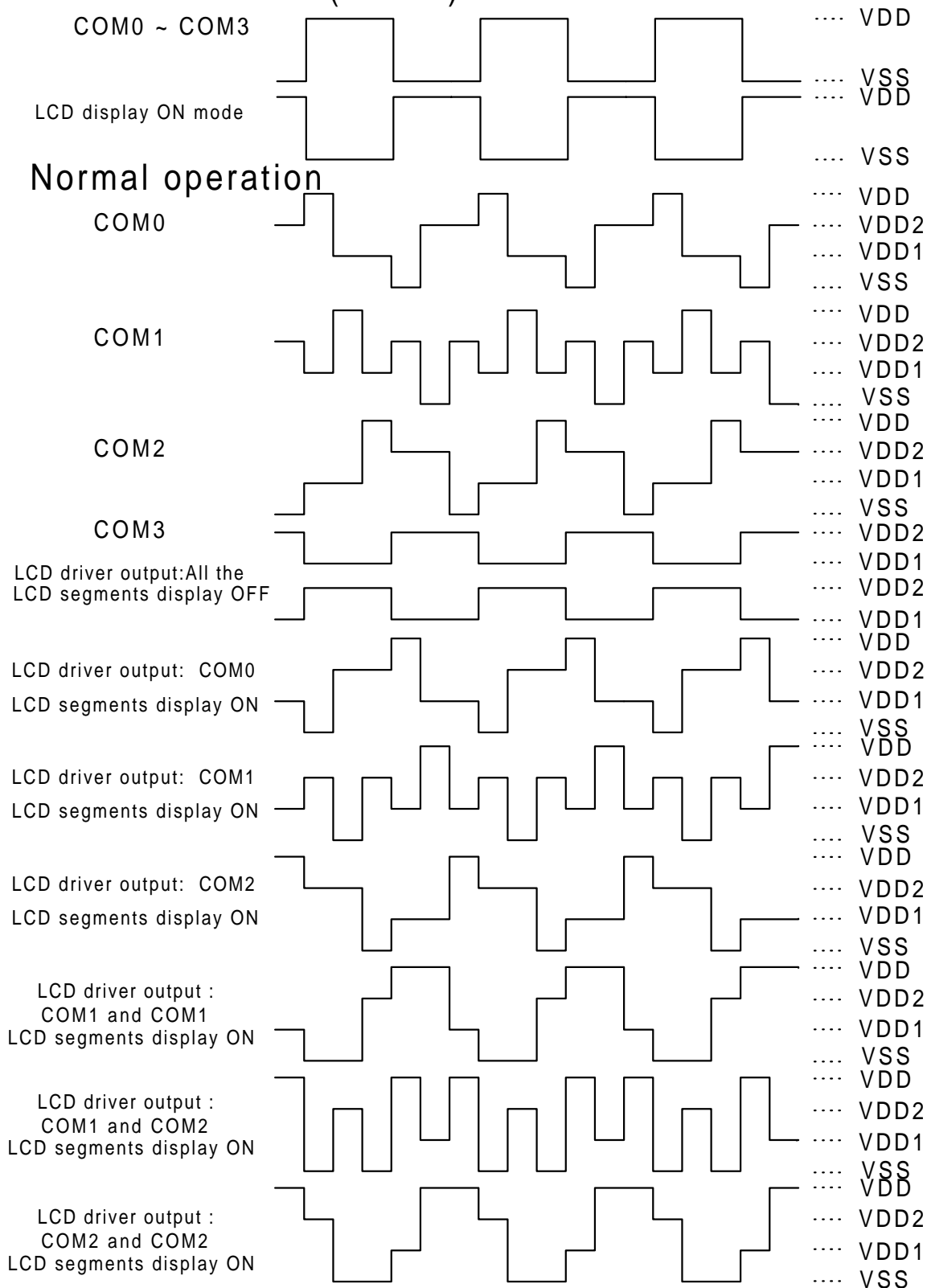
Normal operation





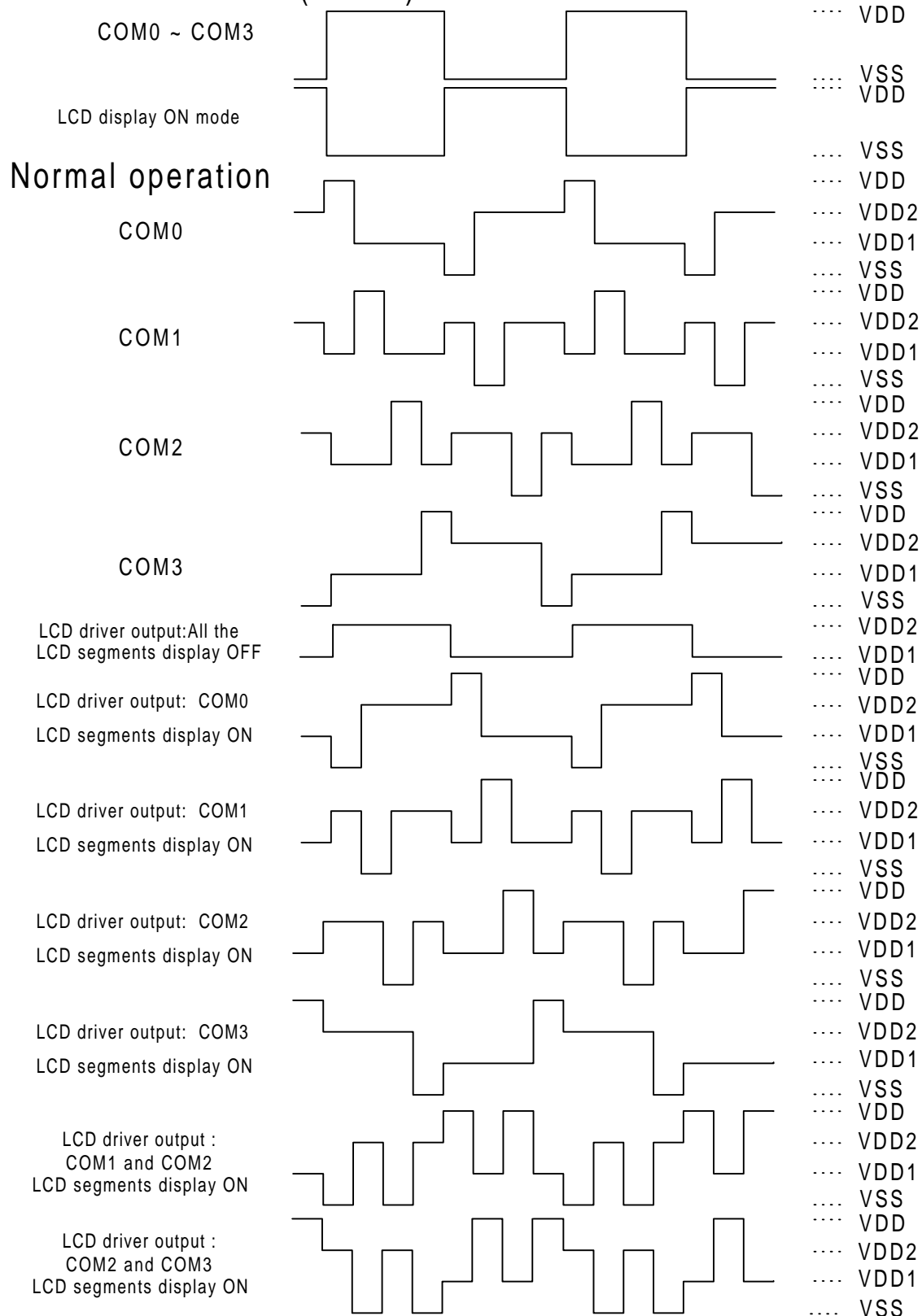
1/3 Bias , 1/3 duty lighting format

At the initial clear (reset)





1/3 Bias , 1/4 duty lighting format
At the initial clear (reset)



■ RESET FUNCTION

The SPL10A1 can be reset by setting the RESET pin to ground voltage and its operation starts when this pin is set to power voltage. Also an automatic reset function (internal reset function) operates when power is turned on.

■ WATCH DOG FUNCTION

The SPL10A1 provides a watch dog timer. The watch dog timer must be reset when 2 Hz wake-up by writing \$0F, otherwise it will reset the system.

■ MASK OPTION

The following type mask option is available.

IOEF0 to IOEF5 Select one of A, B, C, D(Refer to INPUT/OUTPUT)

- A. Without Fixed Pull Low Resistor 200K Ω , with Feedback MOS
- B. With Fixed Pull Low Resistor 200K Ω , without Feedback MOS
- C. With Fixed Pull Low Resistor 200K Ω , with Feedback MOS
- D. Without Fixed Pull Low Resistor 200K Ω , without Feedback MOS

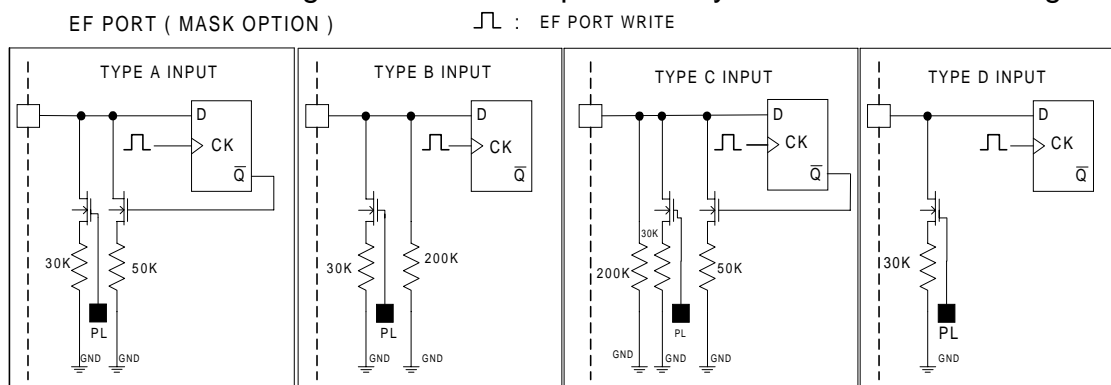
32768 Hz clock source Select one of A, B (Refer to R oscillator)

- A. 32768 Crystal Oscillator
- B. R Oscillator

I/O PORT CONFIGURATION

INPUT IOEF PORT: IOEF0 to IOEF5

There are 4 different configurations in IOEF port. They are shown as following:

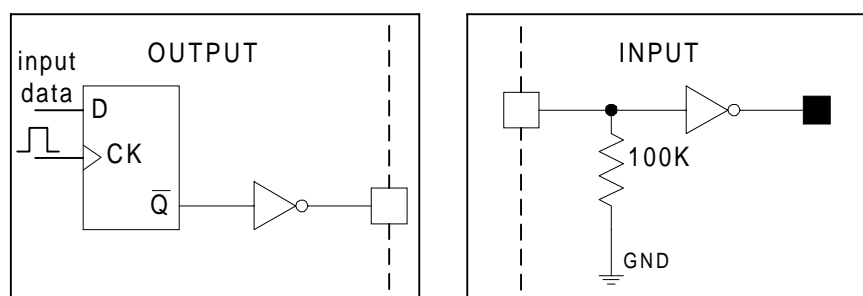


INPUT/OUTPUT IOAB PORT: IOAB0 and IOAB1

These two ports can be programmed to be INPUT or OUTPUT pins.

The configurations are shown as below:

AB PORT  : AB PORT WRITE

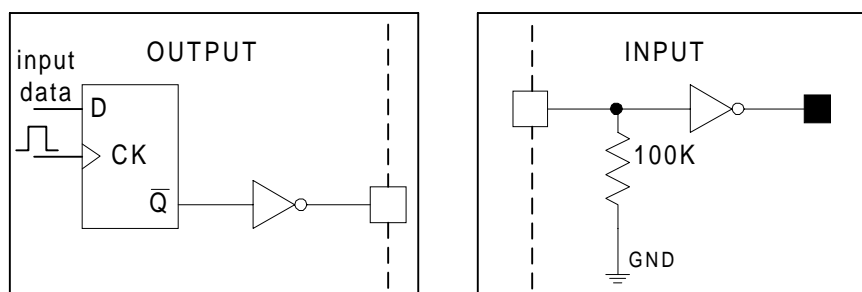


* INPUT/OUTPUT IOCD PORT: IOCD0 to IOCD3

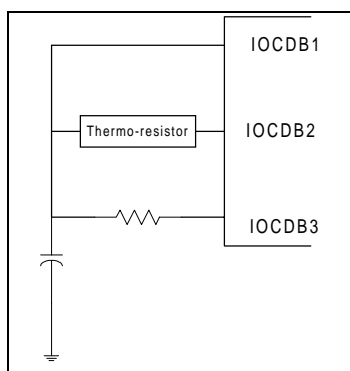
These four IOCD ports can be programmed to be INPUT or OUTPUT

pins independently. These pins also can be used to implement a thermometer by sense mode. Their configurations are shown as belows:

CD PORT  : CD PORT WRITE



The application circuit for sense mode:



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Ratings
DC supply Voltage	V+	< 7V
Input Voltage Range	V _{IN}	-0.5V to V+ + 0.5V
Operating Temperature	T _A	0 °C to +60 °C
Storage Temperature	T _{STO}	-50 °C to +150 °C

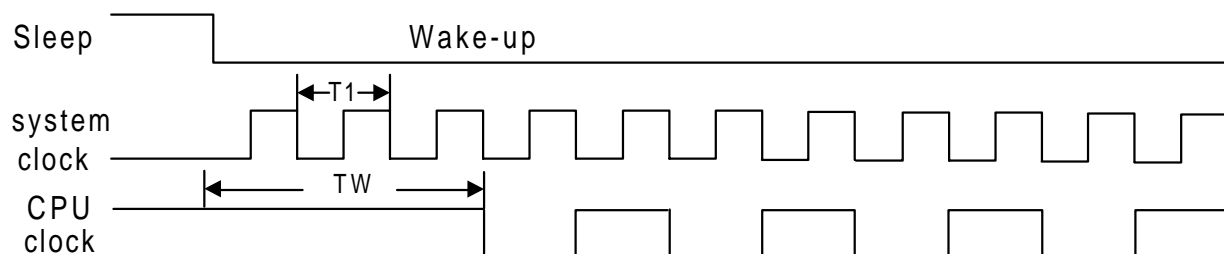
DC CHARACTERISTICS

Characteristics	Symbol	Limit			Unit	Test Condition
		Min	Typ	Max		
Operating Voltage	VDD	2.4	-	5.0	V	
Operating Current	I _{OP}	-	350	-	μA	F _{CPU} = 600KHz/3.0V
Standby Current	I _{STBY}	-	-	1	μA	VDD = 3.0 V
Current DA output	I _{OH}	-	-1	-	mA	VDD = 3.0 V
Input High Level	V _{IH}	2.0	-	-	V	VDD = 3.0 V
Input Low Level	V _{IL}	-	-	0.8	V	VDD = 3.0 V
Output High I (I/O)	I _{OH}	-300	-	-	μA	VDD = 3.0 V, V _{OH} = 2.4V
Output Sink I (I/O)	I _{OL}	600	-	-	μA	VDD = 3.0 V, V _{OL} = 0.8V
LCD Display Voltage	V _{LCD}	-	-	VDD	V	
LCD Drive Output Voltage	VDD	2.8	-	3.0	V	V _{LCD} =3V, I _o = - 6μA
	VDD2	1.8	-	2.2	V	V _{LCD} =3V, I _o = ± 3.5μA
	VDD1	0.8	-	1.2	V	V _{LCD} =3V, I _o = ± 3.5μA
	VSS	0	-	0.2	V	V _{LCD} =3V, I _o = + 6μA
OSC Resistor	R _{osc}	-	50K	-	ohm	

AC CHARACTERISTICS

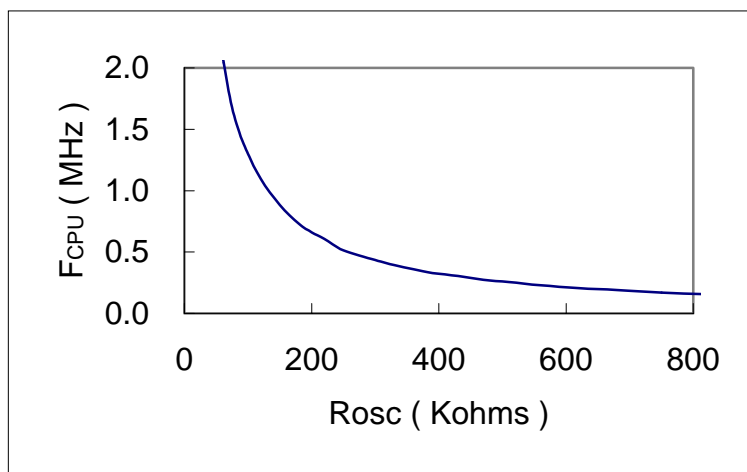
Characteristics	Symbol	Limits			Unit	Test condition
		Min	Typ	Max		
OSC frequency	F _{OSC}	-	-	4.0	MHz	VDD = 3.0 V
CPU clock	F _{CPU}	0.01	-	2.0	MHz	F _{CPU} =F _{OSC} /2@3V
Frame frequency of the LCD drive	F _{fm1}	-	64	-	Hz	1/2 duty
		-	85	-	Hz	1/3 duty
		-	64	-	Hz	1/4 duty
Wake-up time	T _w	6T ₁	-	-	Hz	

$T_1 = 1/(F_{osc})$, $T_w = 3 \times T_1$, $F_{CPU} = F_{OSC}/2$

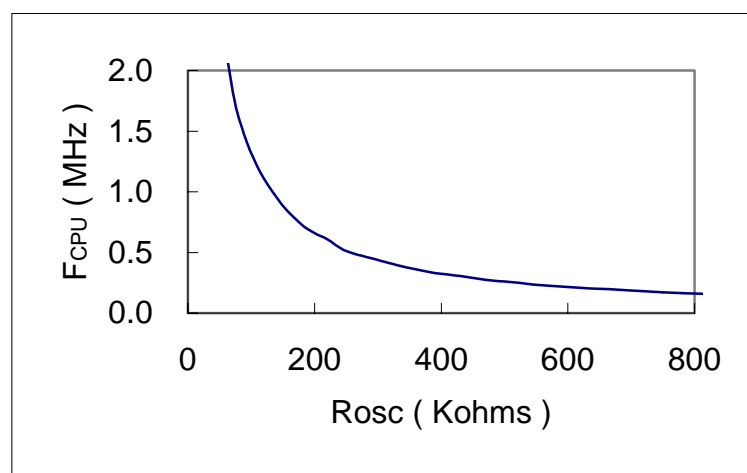


The relationship between the R_{osc} and the F_{CPU}

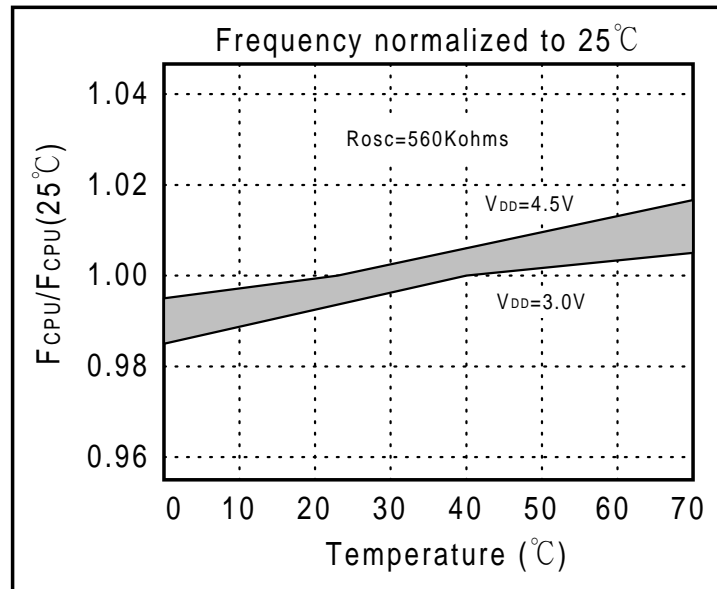
$V_{DD} = 3.0V$, $T_a = 25\text{ }^{\circ}\text{C}$



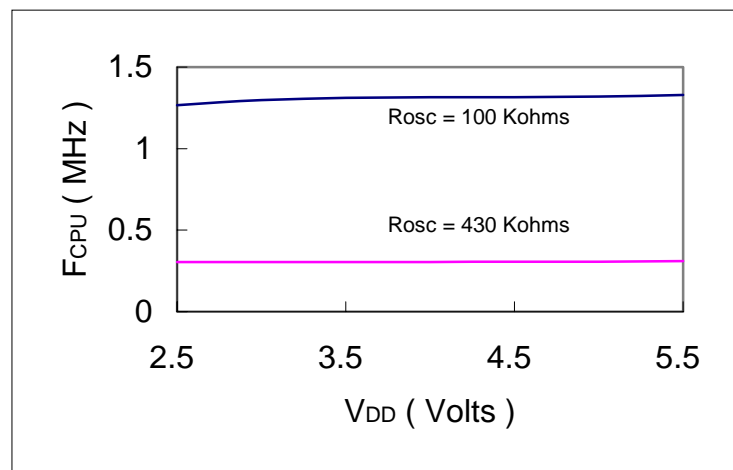
$V_{DD} = 4.5V$, $T_a = 25\text{ }^{\circ}\text{C}$



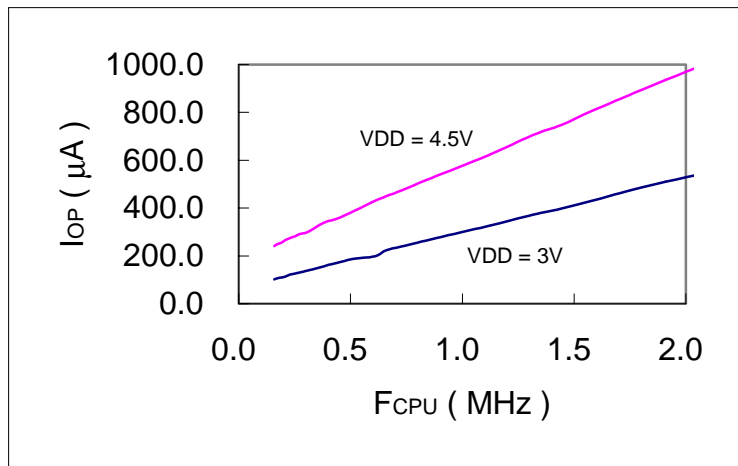
Frequency vs. Temperature



Frequency vs. V_{DD}



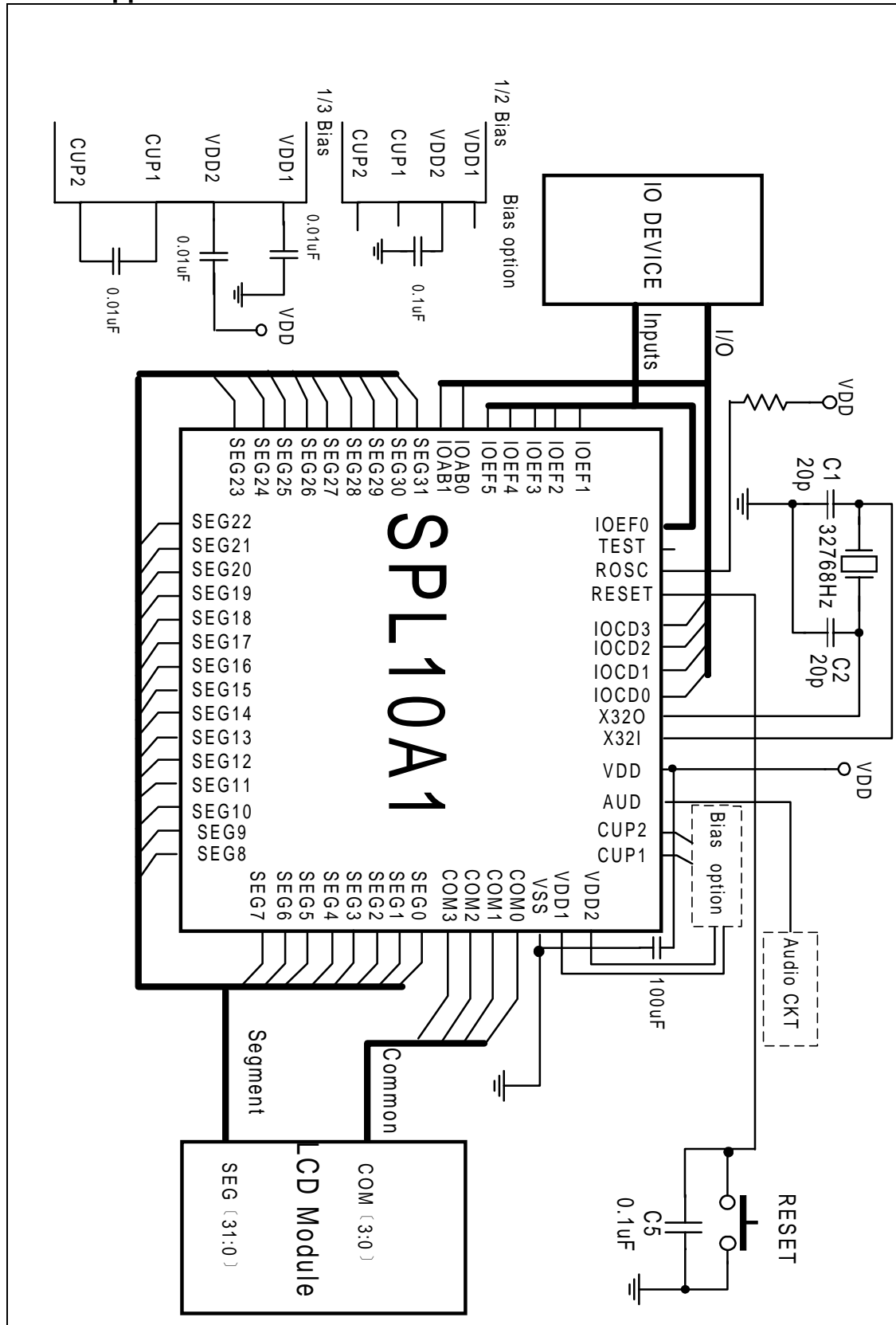
Operating current vs. Frequency vs. V_{DD}



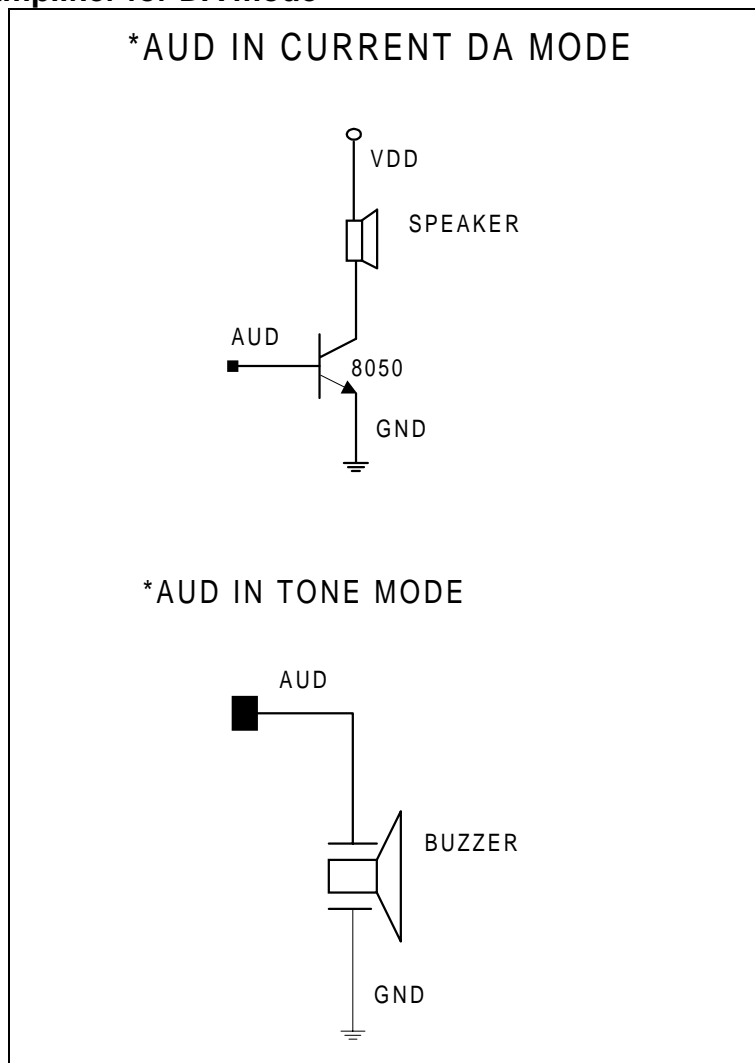


APPLICATION NOTES

■ SPL10A1 Application circuit

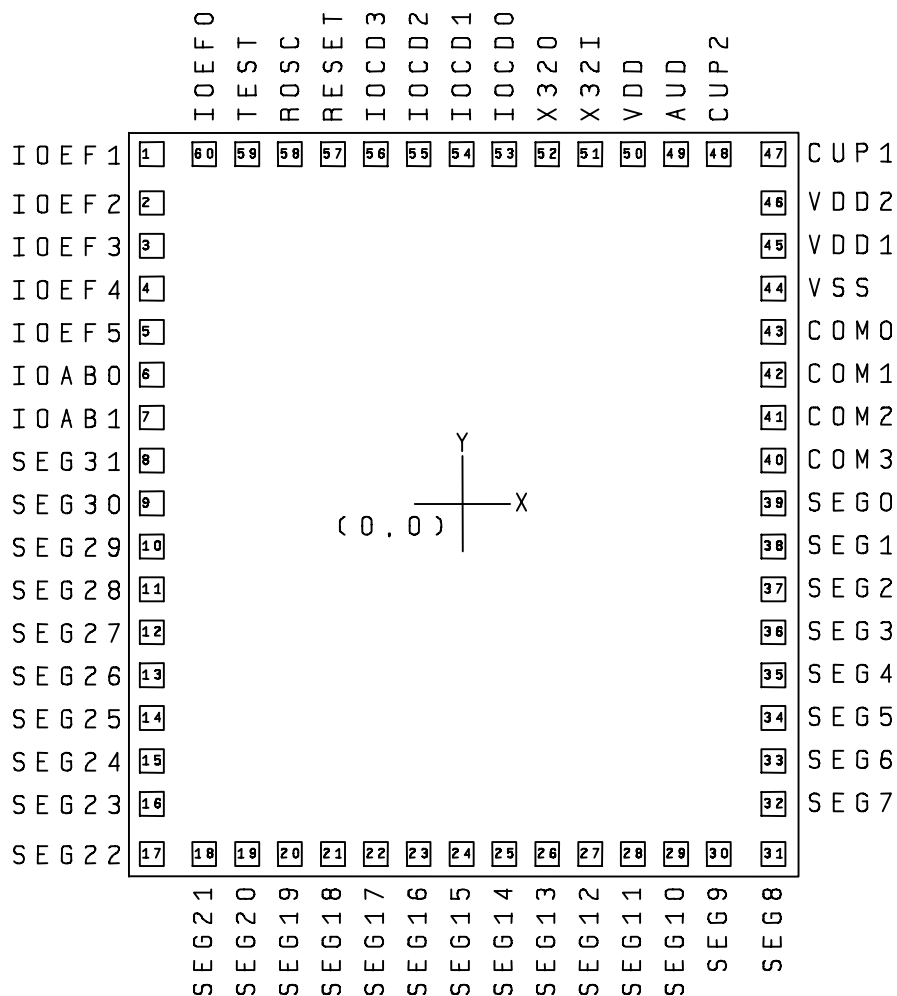


■ Audio driver/amplifier for DA mode



PAD ASSIGNMENT AND LOCATIONS

■ Pad assignment



Chip Size: 2100 μm x 2380 μm

This IC substrate should be connected to VSS

Ordering Information

Product number	Package type
SPL10A1-nnnnV-C	Chip form

Note: 1.Code number (nnnnV) is assigned for customer.

2.Code number (nnnn = 0000 ~ 9999); version (V = A ~ Z).

■ Pad locations

Pad No	Pad Name	X	Y	Pad No	Pad Name	X	Y
1	IOEF1	-913	1028	31	SEG8	912	-1028
2	IOEF2	-913	882	32	SEG7	912	-881
3	IOEF3	-913	756	33	SEG6	912	-755
4	IOEF4	-913	630	34	SEG5	912	-629
5	IOEF5	-913	504	35	SEG4	912	-503
6	IOAB0	-913	378	36	SEG3	912	-377
7	IOAB1	-913	252	37	SEG2	912	-251
8	SEG31	-913	126	38	SEG1	912	-125
9	SEG30	-913	0	39	SEG0	912	0
10	SEG29	-913	-125	40	COM3	912	125
11	SEG28	-913	-251	41	COM2	912	251
12	SEG27	-913	-377	42	COM1	912	377
13	SEG26	-913	-503	43	COM0	912	503
14	SEG25	-913	-629	44	VSS	912	629
15	SEG24	-913	-755	45	VDD1	912	755
16	SEG23	-913	-881	46	VDD2	912	881
17	SEG22	-913	-1028	47	CUP1	912	1028
18	SEG21	-759	-1028	48	CUP2	752	1028
19	SEG20	-633	-1028	49	AUD	626	1028
20	SEG19	-507	-1028	50	VDD	500	1028
21	SEG18	-381	-1028	51	X32I	374	1028
22	SEG17	-255	-1028	52	X32O	248	1028
23	SEG16	-129	-1028	53	IOCD0	122	1028
24	SEG15	-3	-1028	54	IOCD1	-3	1028
25	SEG14	122	-1028	55	IOCD2	-129	1028
26	SEG13	248	-1028	56	IOCD3	-255	1028
27	SEG12	374	-1028	57	RESET	-381	1028
28	SEG11	500	-1028	58	ROSC	-507	1028
29	SEG10	626	-1028	59	TEST	-633	1028
30	SEG9	752	-1028	60	IOEF0	-759	1028