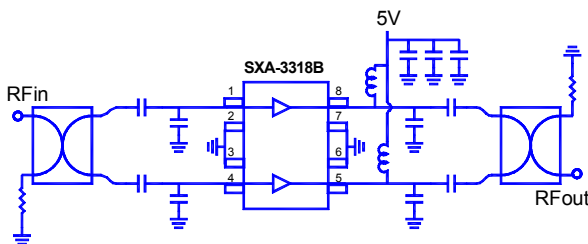


Product Description

Sirenza Microdevices' SXA-3318B amplifier is a high efficiency GaAs Heterojunction Bipolar Transistor (HBT) MMIC housed in a low-cost surface-mountable plastic package. These HBT MMICs are fabricated using molecular beam epitaxial growth technology which produces reliable and consistent performance from wafer to wafer and lot to lot.

These amplifiers are specially designed for use as driver devices for infrastructure equipment in the 400-2500 MHz cellular, ISM, WLL, PCS, W-CDMA applications.

Its high linearity makes it an ideal choice for multi-carrier as well as digital applications.



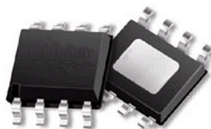
Preliminary

SXA-3318B

400-2500 MHz

Balanced $\frac{1}{2}$ W Medium Power

GaAs HBT Amplifier with Active Bias



Product Features

- On-chip Active Bias Control
- Balanced for excellent input/output VSWR and minimized reflections
- High OIP₃ : +47 dBm typ.
- High P_{1dB} : +28 dBm typ.
- Patented High Reliability GaAs HBT Technology
- Surface-Mountable Power Plastic Package

Applications

- W-CDMA, PCS, Cellular Systems
- High Linearity IF Amplifiers
- Multi-Carrier Applications

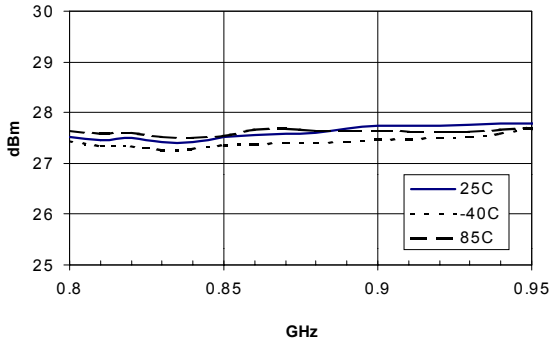
Symbol	Parameters: Test Conditions: $Z_0 = 50 \text{ Ohms}$, $T_a = 25^\circ\text{C}$		Units	Min.	Typ.	Max.
P_{1dB}	Output Power at 1dB Compression	$f = 850 \text{ MHz}$ $f = 1960 \text{ MHz}$ $f = 2140 \text{ MHz}$	dBm	27.0	27.5 28.0 28.0	
S_{21}	Small signal gain	$f = 850 \text{ MHz}$ $f = 1960 \text{ MHz}$ $f = 2140 \text{ MHz}$	dB	10.5	17.5 12.8 12.0	13.5
S_{11}, S_{22}	Input/Output VSWR	$f = 850 \text{ MHz}$ $f = 1960 \text{ MHz}$ $f = 2140 \text{ MHz}$	-		1.3:1 1.2:1 1.2:1	
OIP ₃	Output Third Order Intercept Point (P _{out} /Tone = +11 dBm, Tone spacing = 1 MHz)	$f = 850 \text{ MHz}$ $f = 1960 \text{ MHz}$ $f = 2140 \text{ MHz}$	dBm	45	47 47 48	
ACP	Adjacent Channel Power: IS-95 at $P_{OUT} = 19 \text{ dBm}$ IS-95 at $P_{OUT} = 19 \text{ dBm}$ W-CDMA at $P_{OUT} = 18 \text{ dBm}$	$f = 880 \text{ MHz}$ $f = 1960 \text{ MHz}$ $f = 2140 \text{ MHz}$	dBc		-55 -55 -50	
NF	Noise Figure	$f = 850 \text{ MHz}$ $f = 1960 \text{ MHz}$ $f = 2140 \text{ MHz}$	dB		4.5 5.1 5.1	
I_b	Device Current (120 mA per amplifier)	$V_{CC} = 5V$	mA		240	
$R_{\theta JA}$	Thermal Resistance (junction - lead) per amplifier *Note: 2 amplifiers per packaged part		$^\circ\text{C/W}$		70*	

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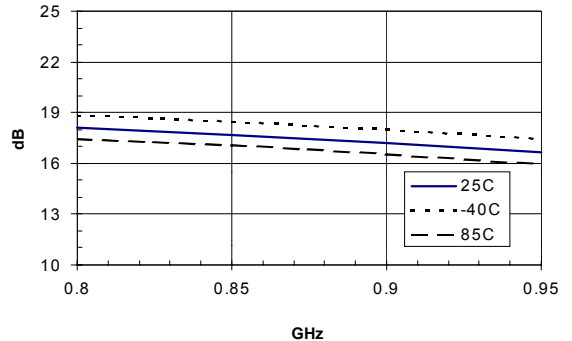
850 MHz Application Circuit Data, $V_{CC} = 5V$, $I_D = 240mA$

Note: Tested in Balanced Configuration shown in Application Circuit, tuned for Output IP3

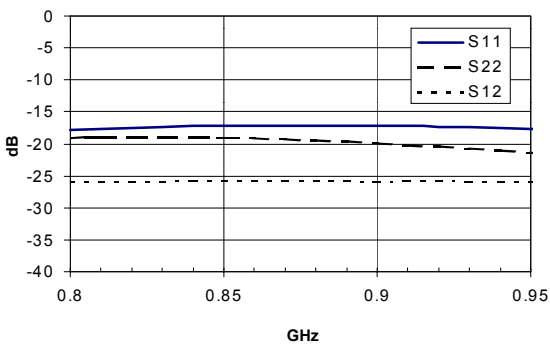
P1dB vs. Frequency



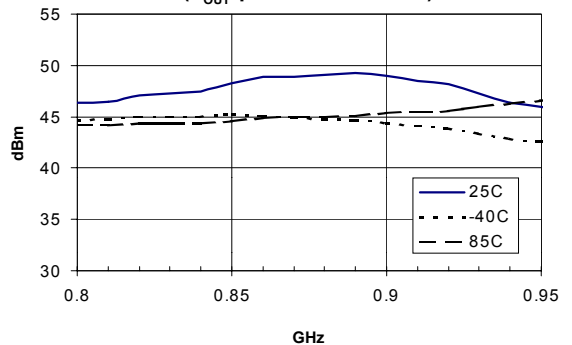
Gain vs. Frequency



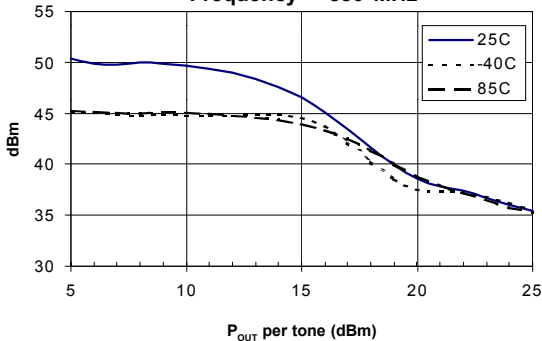
Input/Output Return Loss, Isolation vs. Frequency, T=25°C



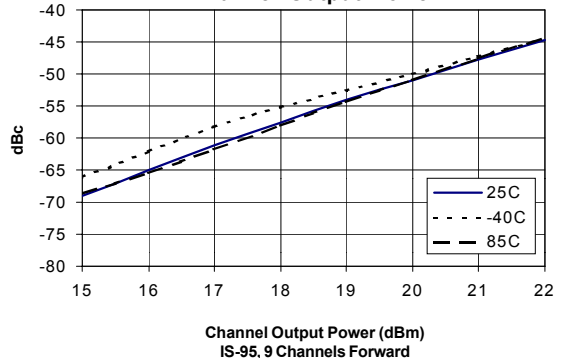
Third Order Intercept vs. Frequency (P_{OUT} per tone = 11dBm)



Third Order Intercept vs. Tone Power Frequency = 880 MHz

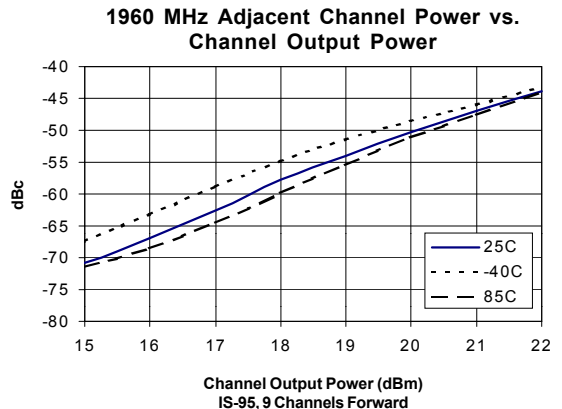
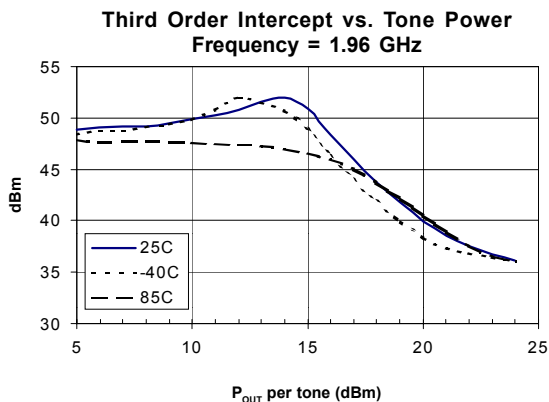
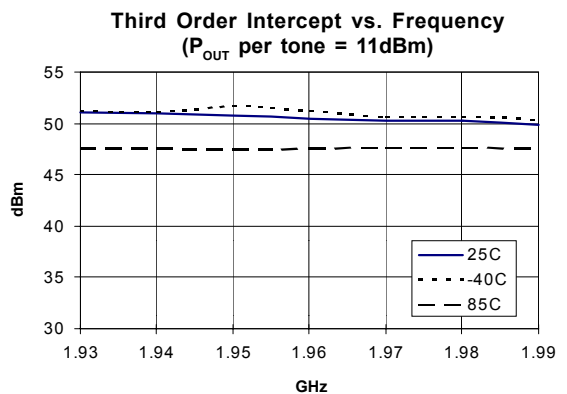
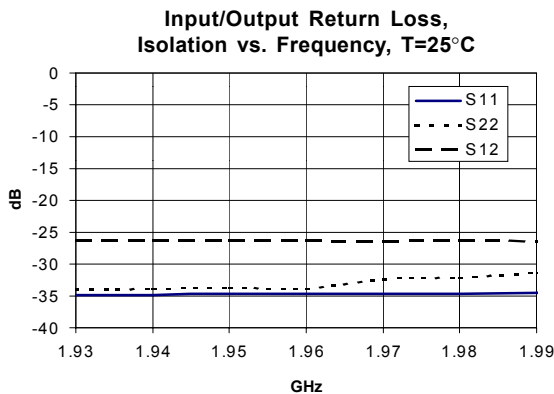
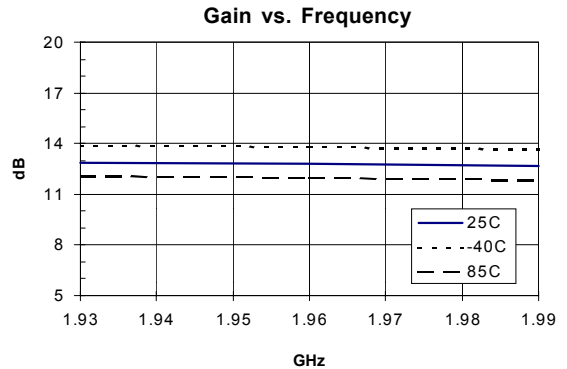
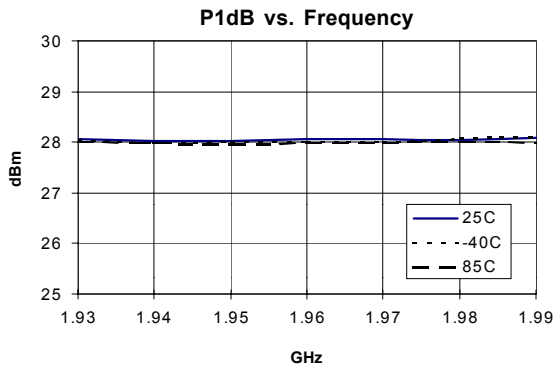


880 MHz Adjacent Channel Power vs. Channel Output Power



1960 MHz Application Circuit Data, $V_{CC} = 5V$, $I_D = 240mA$

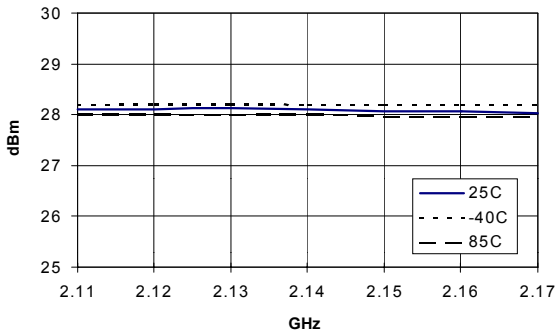
Note: Tested in Balanced Configuration shown in Application Circuit, tuned for Output IP3



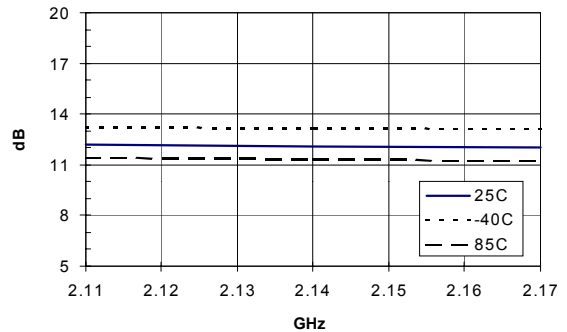
2140 MHz Application Circuit Data, $V_{CC} = 5V$, $I_D = 240mA$

Note: Tested in Balanced Configuration shown in Application Circuit, tuned for Output IP3

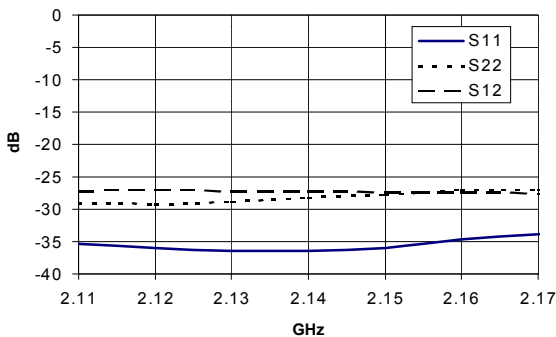
P1dB vs. Frequency



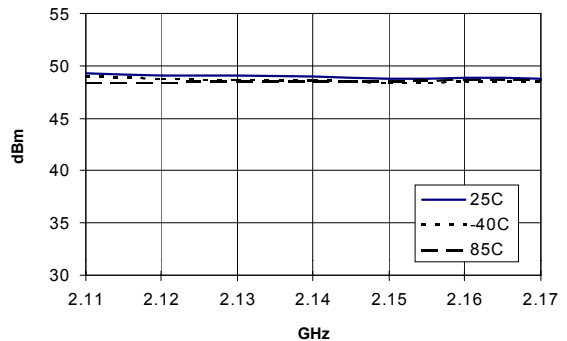
Gain vs. Frequency



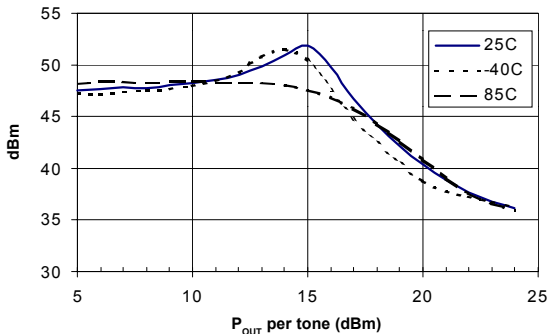
Input/Output Return Loss, Isolation vs. Frequency, T=25°C



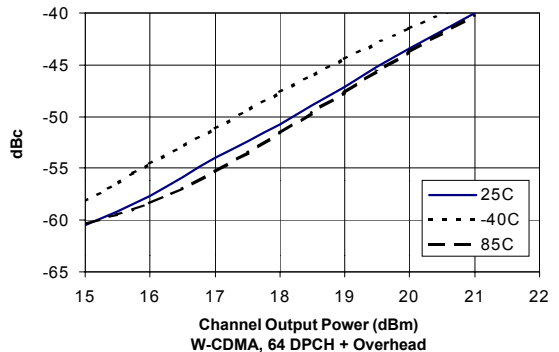
Third Order Intercept vs. Frequency (P_{OUT} per tone = 11dBm)



Third Order Intercept vs. Tone Power Frequency = 2.14 GHz



2140 MHz Adjacent Channel Power vs. Channel Output Power



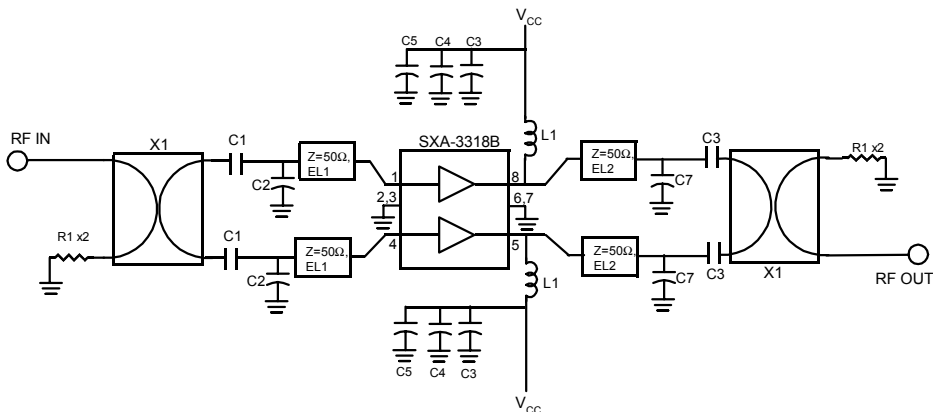
Application Schematic (650 MHz)

The schematic illustrates a balanced 650 MHz circuit using two SXA-3318B amplifiers. The input RF IN is connected to a balun (X1) and a matching network consisting of a series capacitor C1, a shunt capacitor C2 to ground, and a series inductor L1. This is followed by a series impedance Z=50Ω, EL1. The signal then splits into two parallel paths, each containing a series impedance Z=50Ω, EL2 and a series inductor L1, leading to the inputs of the two SXA-3318B amplifiers. The amplifiers are powered by VCC rails, with decoupling capacitors C3, C4, C5, and C6 connected to the supply and ground. The outputs of the amplifiers are connected to a matching network with a series impedance Z=50Ω, EL3, a shunt capacitor C7 to ground, and a series capacitor C3. The signals are then combined by a second balun (X1) and a series resistor R1 x2 to produce the RF OUT. Inductors L2 are connected between the amplifier outputs and the VCC rails.

Ref. Des.	Vendor Series	850 MHz
C1, C3	Rohm MCH18	47pF, 5%
C2	Rohm MCH18	3.9pF, ± 0.25 pF
C4	Rohm MCH18	1000pF, 5%
C5	Rohm TAJB104KLRH	0.1uF, 10%
C6	Rohm TAJB106K020R	10uF, 10%
C7	Rohm MCH18	3.3pF, ± 0.25 pF
L1	Toko LL1608-FS	1.2nH, ± 0.3 nH

Ref. Des.	Vendor Series	850 MHz
L2	Toko LL1608-FS	33nH, 5%
EL1	50 Ohms	9.9°
EL2	50 Ohms	4.4°
EL3	50 Ohms	11°
X1	Sirenza Coupler	AH03L
R1	Rohm MCR100J	100 Ohm, 5%

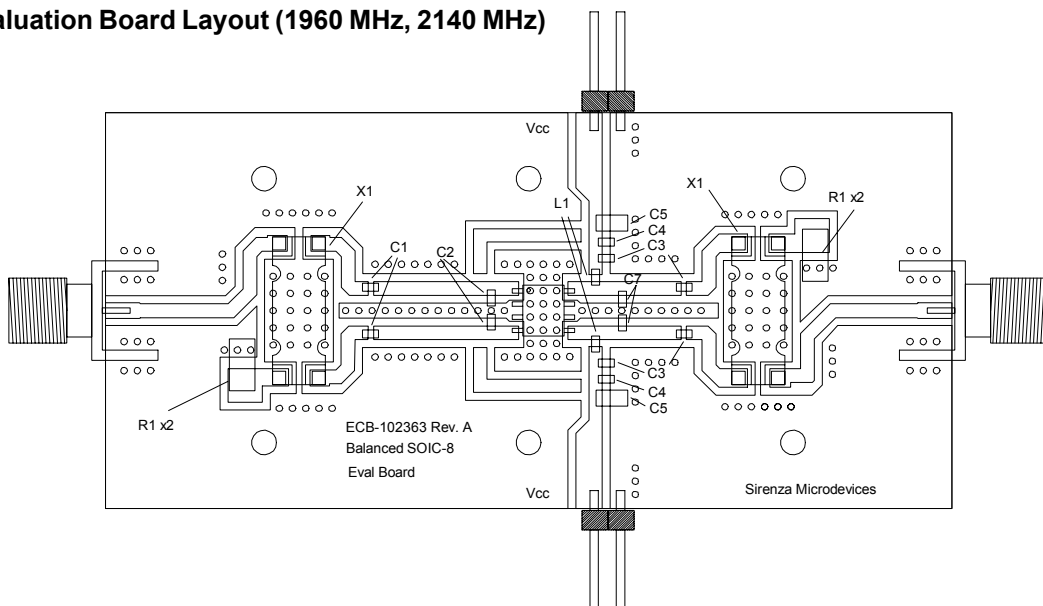
Application Schematic (1960 MHz, 2140 MHz)

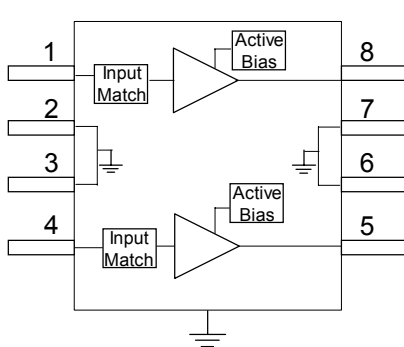


Ref. Des.	Vendor Series	1960 MHz	2140 MHz
C1, C3	Rohm MCH18	22pF, 5%	22pF, 5%
C2	Rohm MCH18	1.2pF, ± 0.25 pF	1.2pF, ± 0.25 pF
C4	Rohm MCH18	1000pF, 5%	1000pF, 5%
C5	Rohm TAJB104KLRH	0.1uF, 10%	0.1uF, 10%
C7	Rohm MCH18	1.0pF, ± 0.25 pF	1.0pF, ± 0.25 pF

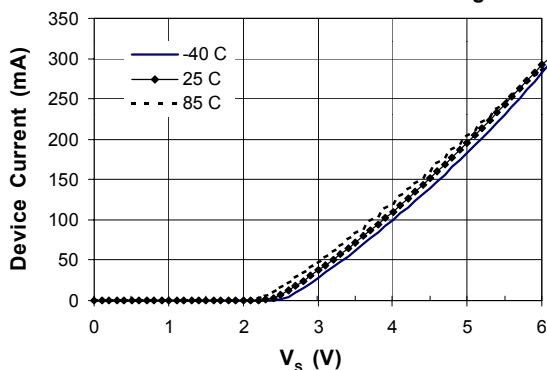
Ref. Des.	Vendor Series	1960 MHz	2140 MHz
L1	Toko LL1608-FS	18nH, 5%	18nH, 5%
EL1	50 Ohms	10.1°	11°
EL2	50 Ohms	20.9°	22.8°
X1	Sirenza Coupler	AM03M	AM03M
R1	Rohm MCR100J	100 Ohm, 5%	100 Ohm, 5%

Evaluation Board Layout (1960 MHz, 2140 MHz)



Pin #	Function	Description	Device Schematic
1, 4	RF In	RF input pin. This pin requires the use of an external DC blocking capacitor.	
2, 3, 6, 7	GND	Connection to ground. Use via holes to reduce lead inductance. Place vias as close to ground leads as possible.	
5, 8	RF Out/Vcc	RF output and bias pin. Bias should be supplied to this pin through an external RF choke. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see application schematic). The supply side of the bias network should be well bypassed. An output matching network is necessary for optimum performance.	
EPAD	GND	Exposed area on the bottom side of the package needs to be soldered to the ground plane of the board for thermal and RF performance. Several vias should be located under the EPAD as shown in the recommended land pattern (page 8).	

Device Current vs. Source Voltage



Absolute Maximum Ratings

Parameter	Absolute Limit
Max. Supply Current (I_b) per amplifier (2 amplifiers per packaged part)	240 mA
Max. Device Voltage (V_{cc})	6.0 V
Max. Power Dissipation per amplifier (2 amplifiers per packaged part)	1500 mW
Max. RF Input Power per amplifier (2 amplifiers per packaged part)	100 mW
Max. Junction Temp. (T_j)	+160 °C
Operating Lead Temp. (T_L)	-40 to +85 °C
Max. Storage Temp.	+150 °C

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page one.

Bias Conditions should also satisfy the following expression:
 $I_b V_{cc} (max) < (T_j - T_L) / R_{\theta JA}$

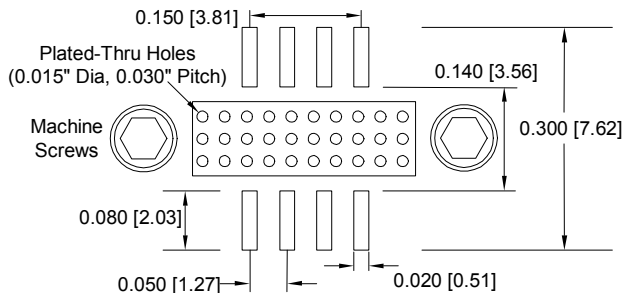

ESD: Class 1B (Passes 500V ESD pulse)

Appropriate precautions in handling, packaging and testing devices must be observed.

Moisture Sensitivity Level: Level 1 (MSL-1)

No special moisture packaging/handling is required during storage, shipment, or installation of the devices.

Recommended Land Pattern



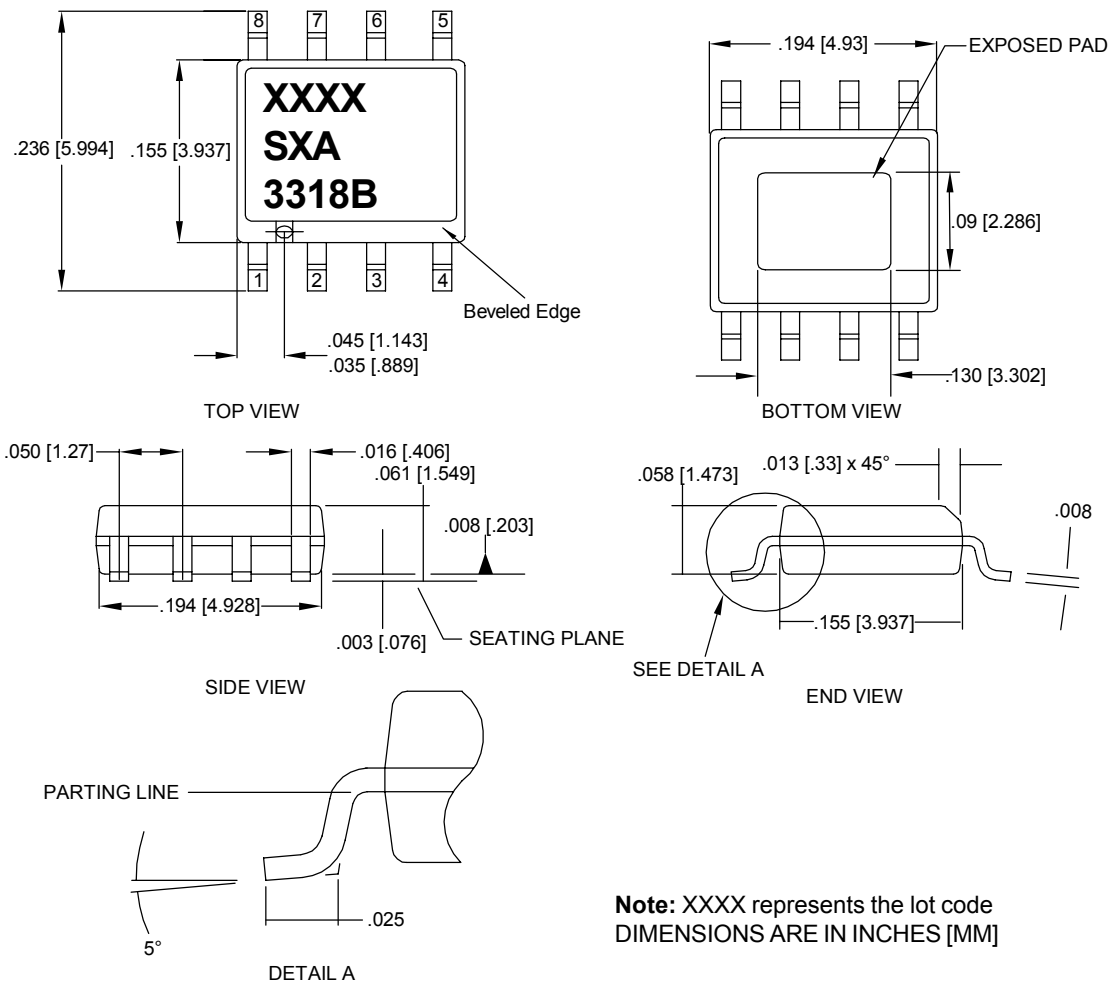
Part Number Ordering Information

Part Number	Devices Per Reel	Reel Size
SXA-3318B	500	7"

Part Symbolization

The part will be symbolized with a "SXA3318B" designator on the top surface of the package.

Package Outline Drawing (See SMDI MPO-101644 for tolerances)



Note: XXXX represents the lot code
DIMENSIONS ARE IN INCHES [MM]