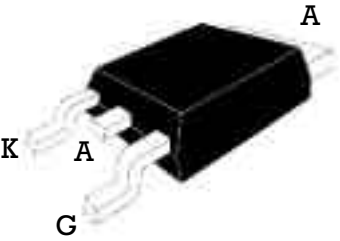


SURFACE MOUNT SCR

<p style="text-align: center;">DPAK (Plastic)</p> 	<table border="0" style="width: 100%;"> <tr> <td style="text-align: center; vertical-align: top;"> On-State Current 4 Amp </td><td style="text-align: center; vertical-align: top;"> Gate Trigger Current $< 200 \mu\text{A}$ </td></tr> <tr> <td colspan="2" style="text-align: center; vertical-align: top;"> Off-State Voltage $200 \text{ V} \div 600 \text{ V}$ </td></tr> </table> <p>These series of Silicon Controlled Rectifier use a high performance PNP technology.</p> <p>These parts are intended for general purpose applications where high gate sensitivity is required using surface mount technology.</p>	On-State Current 4 Amp	Gate Trigger Current $< 200 \mu\text{A}$	Off-State Voltage $200 \text{ V} \div 600 \text{ V}$	
On-State Current 4 Amp	Gate Trigger Current $< 200 \mu\text{A}$				
Off-State Voltage $200 \text{ V} \div 600 \text{ V}$					

Absolute Maximum Ratings, according to IEC publication No. 134

SYMBOL	PARAMETER	CONDITIONS	Min.	Max.	Unit
$I_{T(RMS)}$	On-state Current	180° Conduction Angle, $T_c = 115^\circ\text{C}$	4		A
$I_{T(AV)}$	Average On-State Current	Half Cycle, $\approx 180^\circ$, $T_c = 115^\circ\text{C}$	2.5		A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 60 Hz	33		A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 50 Hz	30		A
I^2t	Fusing Current	$t = 10 \text{ ms}$, Half Cycle	4.5		A^2s
V_{GRM}	Peak Reverse Gate Voltage	$I_{GR} = 10 \mu\text{A}$	8		V
I_{GM}	Peak Gate Current	20 μs max.		1.2	A
P_{GM}	Peak Gate Dissipation	20 μs max.		3	W
$P_{G(AV)}$	Gate Dissipation	20 ms max.		0.2	W
T_j	Operating Temperature		-40	+125	$^\circ\text{C}$
T_{stg}	Storage Temperature		-40	+150	$^\circ\text{C}$
T_{sld}	Soldering Temperature	10s max		260	$^\circ\text{C}$

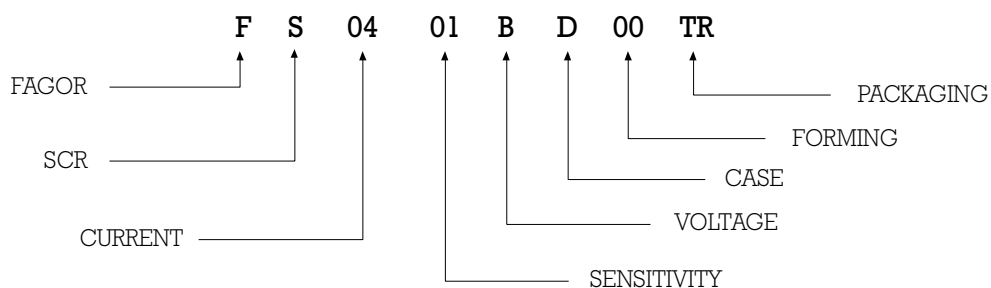
SYMBOL	PARAMETER	CONDITIONS	VOLTAGE			Unit
			B	D	M	
V_{DRM} V_{RRM}	Repetitive Peak Off State Voltage	$R_{GK} = 1 \text{ K}$	200	400	600	V

SURFACE MOUNT SCR

Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS		SENSITIVITY				Unit
				01	04	02	03	
I_{GT}	Gate Trigger Current	$V_D = 12 V_{DC}$, $R_L = 33 \Omega$, $T_j = 25^\circ C$	MIN MAX	1 20	15 50	 200	20 200	μA
I_{DRM} / I_{RRM}	Off-State Leakage Current	$V_D = V_{DRM}$, $R_{GK} = 220 \Omega$, $T_j = 125^\circ C$ $V_R = V_{RRM}$, $T_j = 25^\circ C$	MAX MAX	1 5				mA μA
V_{TM}	On-state Voltage	at $I_T = 8 \text{ Amp}$, $t_p = 380 \mu s$, $T_j = 25^\circ C$	MAX	1.6				V
V_{GT}	Gate Trigger Voltage	$V_D = 12 V_{DC}$, $R_L = 33 \Omega$, $T_j = 25^\circ C$	MAX	0.8				V
V_{GD}	Gate Non Trigger Voltage	$V_D = V_{DRM}$, $R_L = 3.3 K$, $R_{GK} = 220 \Omega$, $T_j = 125^\circ C$	MIN	0.1				V
I_H	Holding Current	$I_T = 50 \text{ mA}$, $R_{GK} = 1 K$, $T_j = 25^\circ C$	MAX	5				mA
I_L	Latching Current	$I_G = 1 \text{ mA}$, $R_{GK} = 1 K$, $T_j = 25^\circ C$	MAX	6				mA
dv / dt	Critical Rate of Voltage Rise	$V_D = 0.67 \times V_{DRM}$, $R_{GK} = 220 \Omega$, $T_j = 125^\circ C$	MIN	10	10	5	10	$V/\mu s$
di / dt	Critical Rate of Current Rise	$I_G = 2 \times I_{GT}$, $T_r = 100 \text{ ns}$, $F = 60 \text{ Hz}$, $T_j = 125^\circ C$	MIN	50				$A/\mu s$
$R_{th(j-c)}$	Thermal Resistance Junction-Case for DC			3				$^\circ C/W$
$R_{th(j-a)}$	Thermal Resistance Junction-Amb ($S=0.5 \text{ cm}^2$)			70				$^\circ C/W$

PART NUMBER INFORMATION



SURFACE MOUNT SCR

Fig. 1: Maximum average power dissipation versus average on-state current

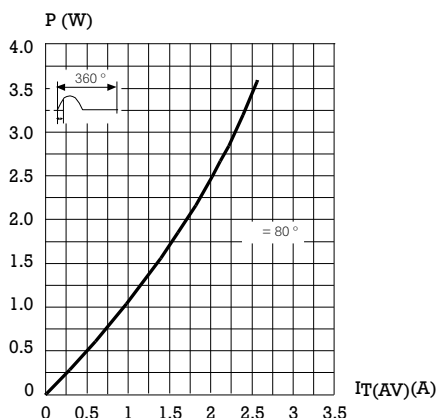


Fig. 3: Average and DC on-state current versus ambient temperature (device mounted on FR4 with recommended pad layout)

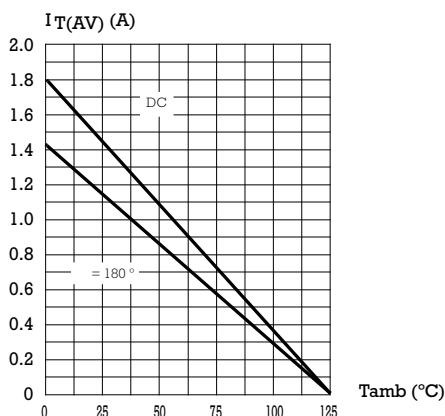


Fig. 4-2: Relative variation of thermal impedance junction to ambient versus pulse duration. (recommended pad layout)

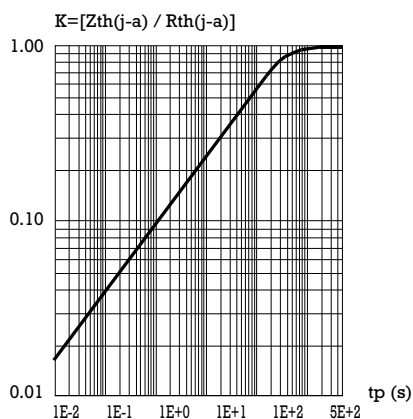


Fig. 2: Correlation between maximum average power dissipation and maximum allowable temperatures (T_{amb} and T_{case}) for different thermal resistances heatsink+contact.

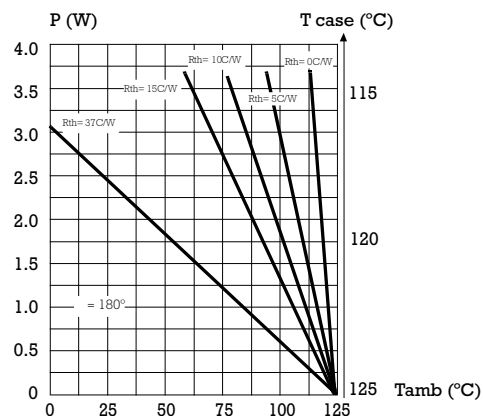


Fig. 4-1: Relative variation of thermal impedance junction to case versus pulse duration.

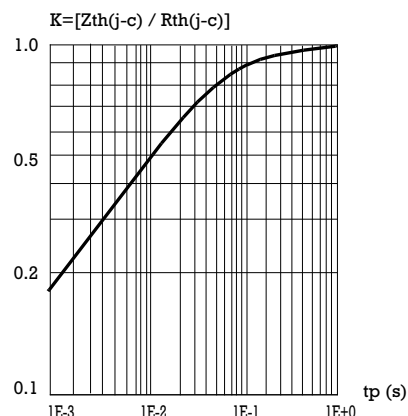
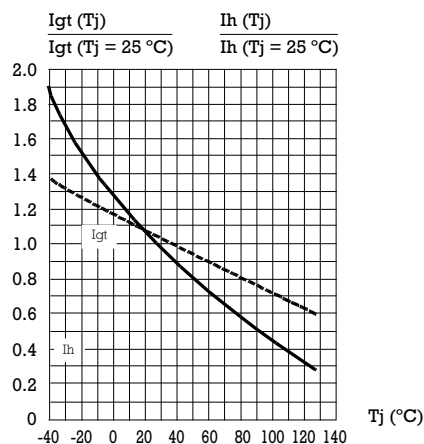


Fig. 5: Relative variation of gate trigger current and holding current versus junction temperature.



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Fig. 6: Non repetitive surge peak on-state current versus number of cycles.

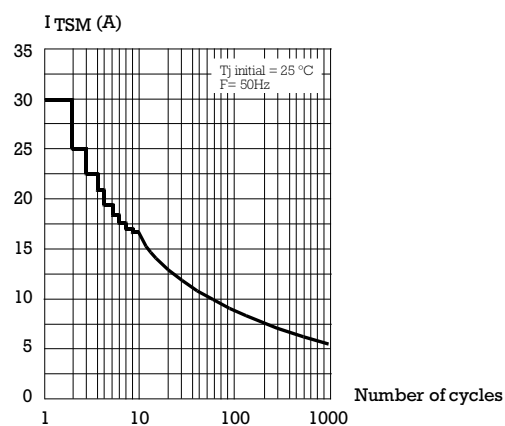


Fig. 7: Non repetitive surge peak on-state current for a sinusoidal pulse with width: $t_p < 10$ ms, and corresponding value of I^2t .

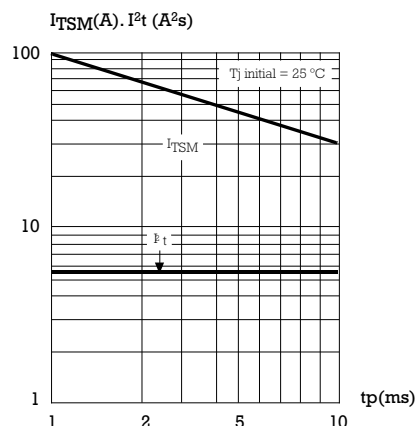


Fig. 8: On-state characteristics (maximum values).

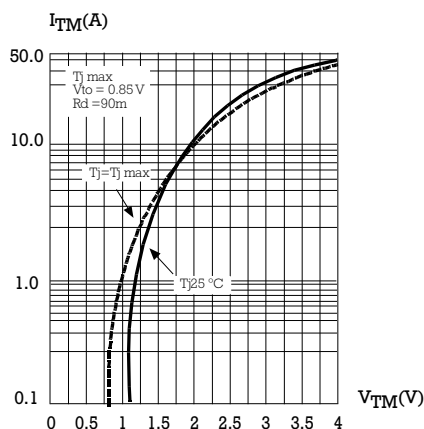


Fig. 9: Thermal resistance junction to ambient versus copper surface under tab (Epoxy printed circuit board FR4, copper thickness: 35 μ m).

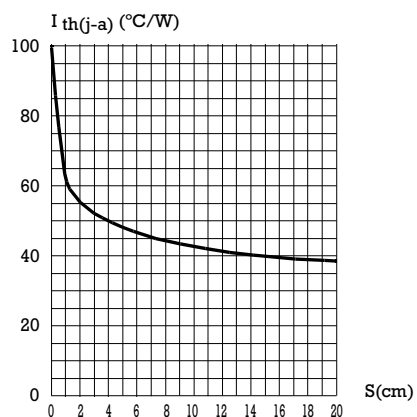
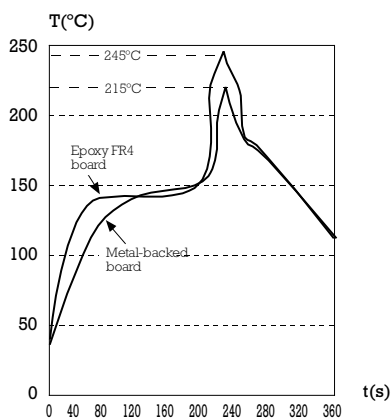
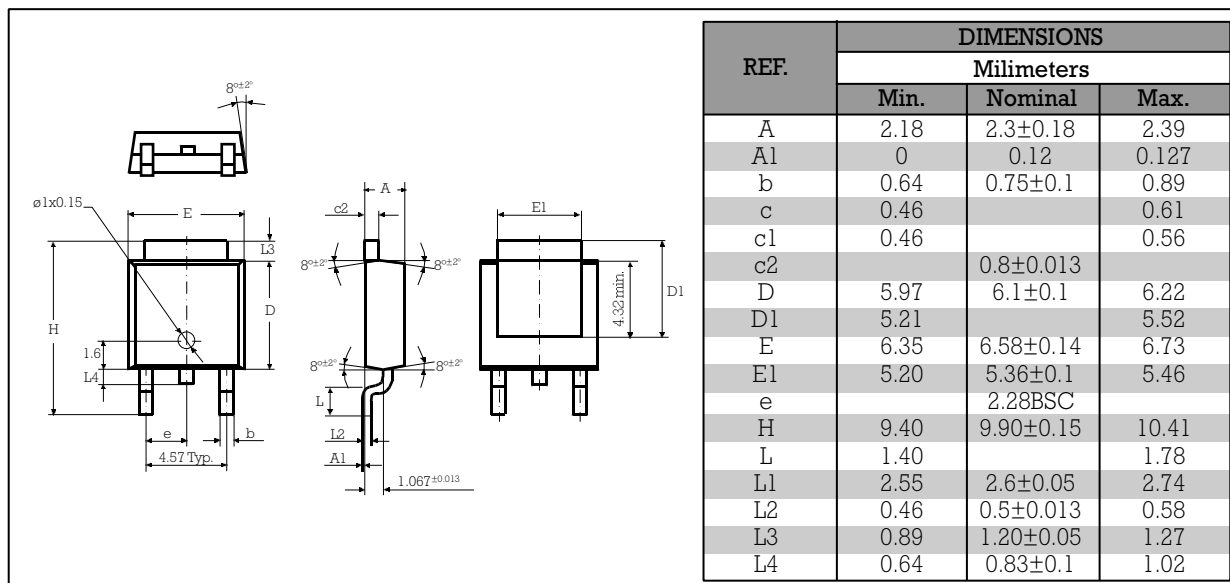


Fig. 10: Typical reflow soldering heat profile, either for mounting on FR4 or metal-backed boards.



SURFACE MOUNT SCR

PACKAGE MECHANICAL DATA



Marking: type number
Weight: 0.2 g

FOOT PRINT

