

74ALVC16721

Low Voltage 20-Bit D-Type Flip-Flops with 3.6V Tolerant Inputs and Outputs

General Description

The ALVC16721 contains twenty non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications.

The 74ALVC16721 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V.

The 74ALVC16721 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.8V–3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD} (CLK to O_n)
 - 4.0 ns max for 3.0V to 3.6V V_{CC}
 - 4.9 ns max for 2.3V to 2.7V V_{CC}
 - 8.8 ns max for 1.65V to 1.95V V_{CC}
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal (Note 1)
- Uses patented noise/EMI reduction circuitry
- Latchup conforms to JEDEC JED78
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V

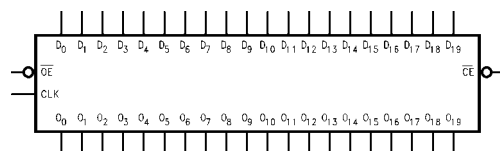
Note 1: To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74ALVC16721MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol

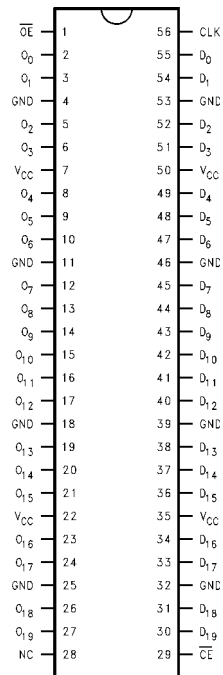


Pin Descriptions

Pin Names	Description
\overline{OE}	Output Enable Input (Active LOW)
CLK	Clock Input
D_0 – D_{19}	Inputs
O_0 – O_{19}	Outputs
\overline{CE}	Clock Enable Input (Active LOW)

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Connection Diagram



Truth Table

CLK	\overline{CE}	\overline{OE}	D ₀ -D ₁₉	O ₀ -O ₁₉
X	X	H	X	Z
X	H	L	X	O ₀
↗	L	L	L	L
↗	L	L	H	H
L or H	L	L	X	O ₀

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial (HIGH or LOW, inputs may not float)

Z = High Impedance

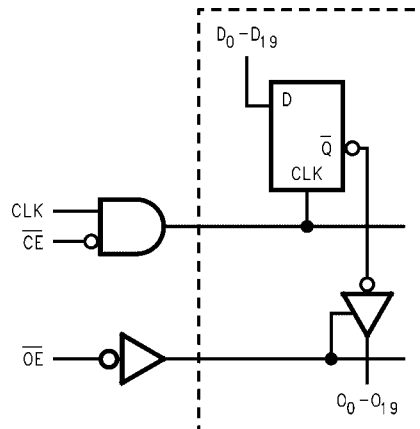
O₀ = Previous O₀ before LOW-to-HIGH transition of Clock

↗ = LOW-to-HIGH transition

Functional Description

The 74ALVC16721 contains twenty D-type flip-flops with 3-STATE standard outputs. The twenty flip-flops will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-HIGH Clock (CLK) transition, when the Clock-Enable (\overline{CE}) is LOW. The 3-STATE standard outputs are controlled by the Output Enable (\overline{OE}). When \overline{OE} is HIGH, the standard outputs are in high impedance mode but this does not interfere with entering new data into the flip-flops.

Logic Diagram



Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	-0.5V to +4.6V
DC Input Voltage (V_I)	-0.5V to 4.6V
Output Voltage (V_O) (Note 3)	-0.5V to V_{CC} +0.5V
DC Input Diode Current (I_{IK})	
$V_I < 0V$	-50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	-50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	± 50 mA
DC V_{CC} or GND Current per Supply Pin (I_{CC} or GND)	± 100 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C

Recommended Operating Conditions (Note 4)

Power Supply	
Operating	1.65V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Free Air Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
$V_{IN} = 0.8V$ to $2.0V$, $V_{CC} = 3.0V$	10 ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Floating or unused inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6	0.65 x V_{CC} 1.7 2.0		V
V_{IL}	LOW Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6		0.35 x V_{CC} 0.7 0.8	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	1.65 - 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -4$ mA	1.65	1.2		
		$I_{OH} = -6$ mA	2.3	2		
		$I_{OH} = -12$ mA	2.3	1.7		
			2.7	2.2		
			3.0	2.4		
V_{OL}	LOW Level Output Voltage	$I_{OH} = -24$ mA	3.0	2		V
		$I_{OL} = 100 \mu A$	1.65 - 3.6		0.2	
		$I_{OL} = 4$ mA	1.65		0.45	
		$I_{OL} = 6$ mA	2.3		0.4	
		$I_{OL} = 12$ mA	2.3		0.7	
			2.7		0.4	
		$I_{OL} = 24$ mA	3		0.55	
I_I	Input Leakage Current	$0 \leq V_I \leq 3.6V$	3.6		± 5.0	μA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$	3.6		± 10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		40	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	3 - 3.6		750	μA

AC Electrical Characteristics

Symbol	Parameter	T _A = -40°C to +85°C, R _L = 500Ω								Units
		C _L = 50 pF				C _L = 30 pF				
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2V		V _{CC} = 1.8V ± 0.15V		
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{MAX}	Maximum Clock Frequency	250		200		200		100		ns
t _{PHL} , t _{PLH}	Propagation Delay Bus to Bus	1.3	4.0	1.5	4.9	1.0	4.4	1.5	8.8	ns
t _{PZL} , t _{PZH}	Output Enable Time	1.3	4.3	1.5	5.4	1.0	4.9	1.5	9.8	ns
t _{PLZ} , t _{PHZ}	Output Disable Time	1.3	4.2	1.5	4.7	1.0	4.2	1.5	7.6	ns
t _W	Pulse Width	1.5		1.5		1.5		4.0		ns
t _S	Setup Time	1.5		1.5		1.5		2.5		ns
t _H	Hold Time	1.0		1.0		1.0		1.0		ns

Capacitance

Symbol	Parameter		Conditions	$T_A = +25^{\circ}\text{C}$		Units
				V_{CC}	Typical	
C_{IN}	Input Capacitance		$V_I = 0V \text{ or } V_{CC}$	3.3	6	pF
C_{OUT}	Output Capacitance		$V_I = 0V \text{ or } V_{CC}$	3.3	7	pF
C_{PD}	Power Dissipation Capacitance	Outputs Enabled	$f = 10\text{ MHz}, C_L = 50\text{ pF}$	3.3	20	pF
				2.5	20	

AC Loading and Waveforms

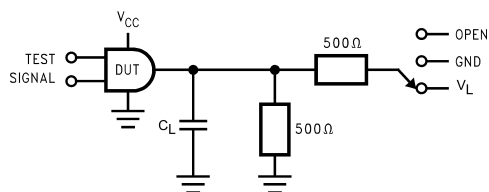


FIGURE 1. AC Test Circuit

TABLE 1. Values for Figure 1

TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	V_L
t_{PZH} , t_{PHZ}	GND

TABLE 2. Variable Matrix
(Input Characteristics: $f = 1\text{MHz}$; $t_r = t_f = 2\text{ns}$; $Z_0 = 50\Omega$)

Symbol	V_{CC}			
	$3.3\text{V} \pm 0.3\text{V}$	2.7V	$2.5\text{V} \pm 0.2\text{V}$	$1.8\text{V} \pm 0.15\text{V}$
V_{mi}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.15\text{V}$	$V_{OL} + 0.15\text{V}$
V_Y	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.15\text{V}$	$V_{OH} - 0.15\text{V}$
V_L	6V	6V	$V_{CC} \times 2$	$V_{CC} \times 2$

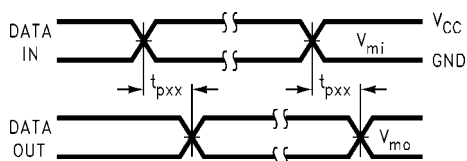


FIGURE 2. Waveform for Inverting and Non-inverting Functions

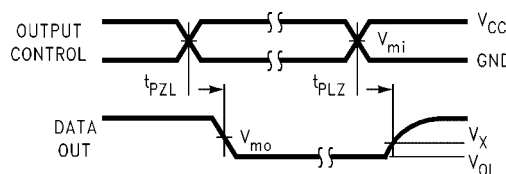


FIGURE 3. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

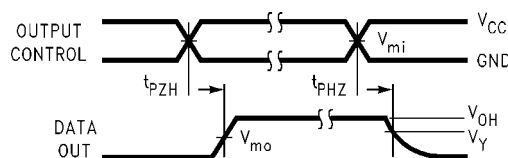


FIGURE 4. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

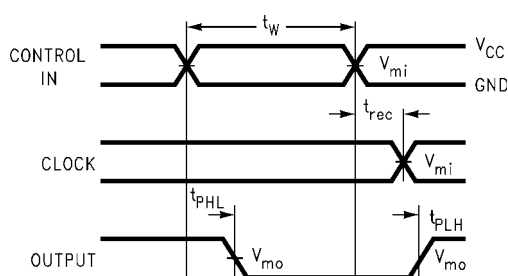


FIGURE 5. Propagation Delay, Pulse Width and t_{rec} Waveforms

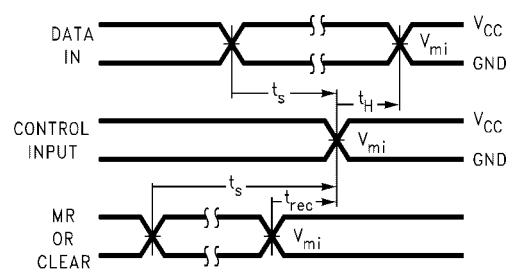
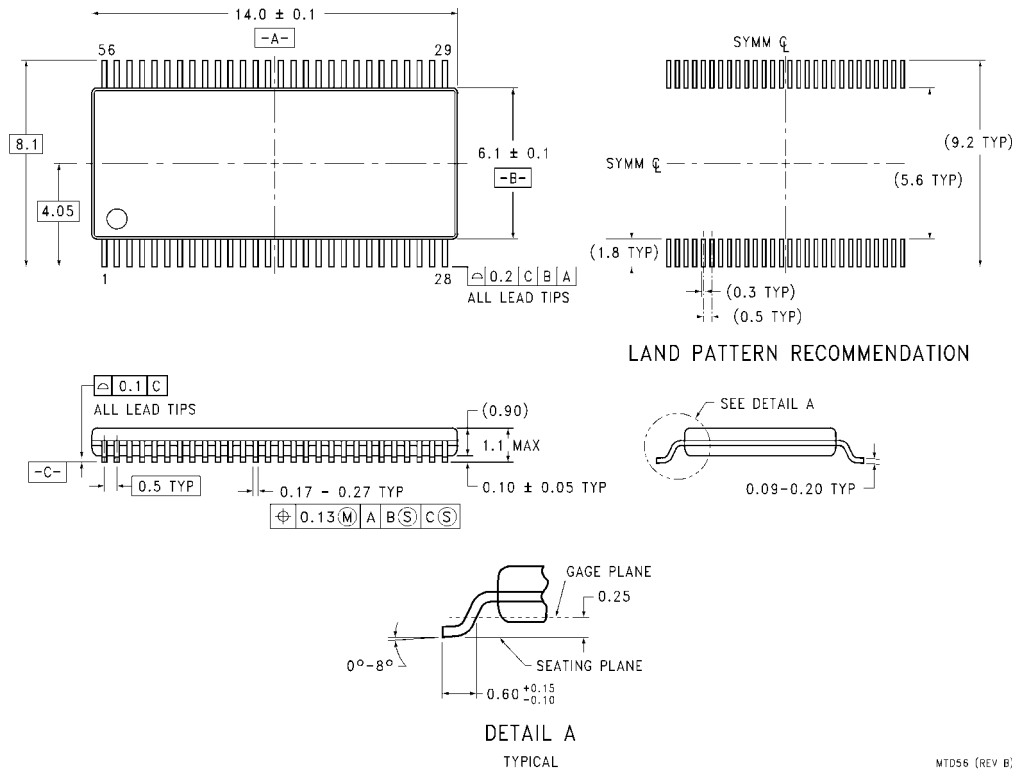


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Physical Dimensions

inches (millimeters) unless otherwise noted



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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