

## 74F539

### Dual 1-of-4 Decoder with 3-STATE Outputs

#### General Description

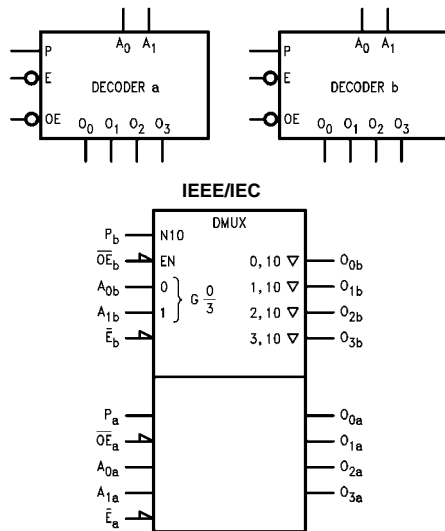
The 74F539 contains two independent decoders. Each accepts two Address ( $A_0$ ,  $A_1$ ) input signals and decodes them to select one of four mutually exclusive outputs. A polarity control input ( $P$ ) determines whether the outputs are active HIGH ( $P = L$ ) or active LOW ( $P = H$ ). An active LOW input Enable ( $E$ ) is available for data demultiplexing; data is routed to the selected output in non-inverted form in the active LOW mode or in inverted form in the active HIGH mode. A HIGH signal on the active LOW Output Enable ( $\overline{OE}$ ) input forces the 3-STATE outputs to the high impedance state.

#### Ordering Code:

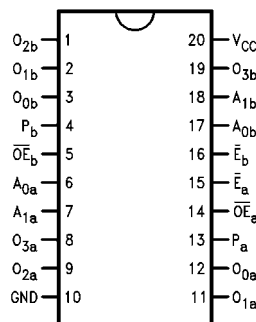
Order Number	Package Number	Package Description
74F539SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F539PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Logic Symbols



#### Connection Diagram



74F539 Dual 1-of-4 Decoder with 3-STATE Outputs

Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_{0a}-A_{1a}$	Side A Address Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$A_{0b}-A_{1b}$	Side B Address Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{E}_a, \overline{E}_b$	Enable Inputs (Active LOW)	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{OE}_a, \overline{OE}_b$	Output Enable Inputs (Active LOW)	1.0/1.0	20 $\mu$ A/-0.6 mA
$P_a, P_b$	Polarity Control Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$O_{0a}-O_{3a}$	Side A 3-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)
$O_{0b}-O_{3b}$	Side B 3-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

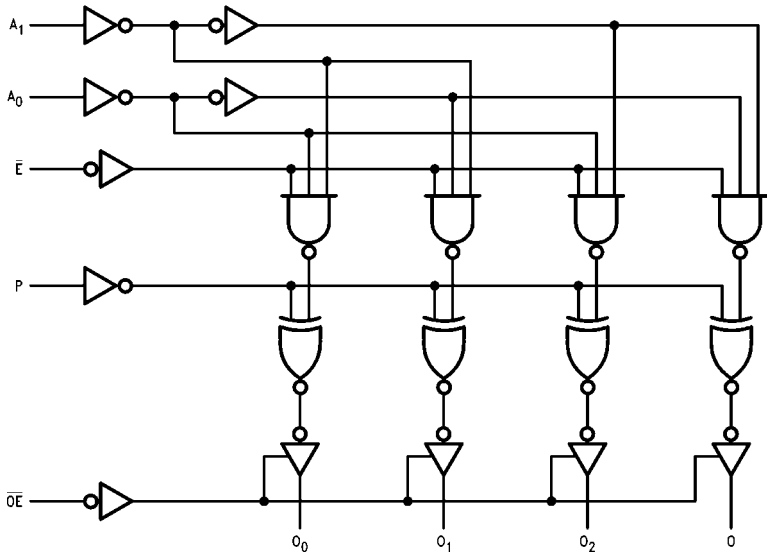
Truth Table

(each half)

Function	Inputs				Outputs			
	$\overline{OE}$	$\overline{E}$	$A_1$	$A_0$	$O_0$	$O_1$	$O_2$	$O_3$
High Impedance	H	X	X	X	Z	Z	Z	Z
Disable	L	H	X	X	$O_n = P$			
Active HIGH Output ( $P = L$ )	L	L	L	L	H	L	L	L
	L	L	L	H	L	H	L	L
	L	L	H	L	L	L	H	L
	L	L	H	H	L	L	L	H
Active LOW Output ( $P = H$ )	L	L	L	L	L	H	H	H
	L	L	L	H	H	L	H	H
	L	L	H	L	H	H	L	H
	L	L	H	H	H	H	H	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

Logic Diagram (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
3-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub> 10% V <sub>CC</sub> 5% V <sub>CC</sub> 5% V <sub>CC</sub>	2.5 2.4 2.7 2.7		V	Min	I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −3 mA
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			−0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	−60		−150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current		28	45	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		40	60	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		40	60	mA	Max	V <sub>O</sub> = HIGH Z

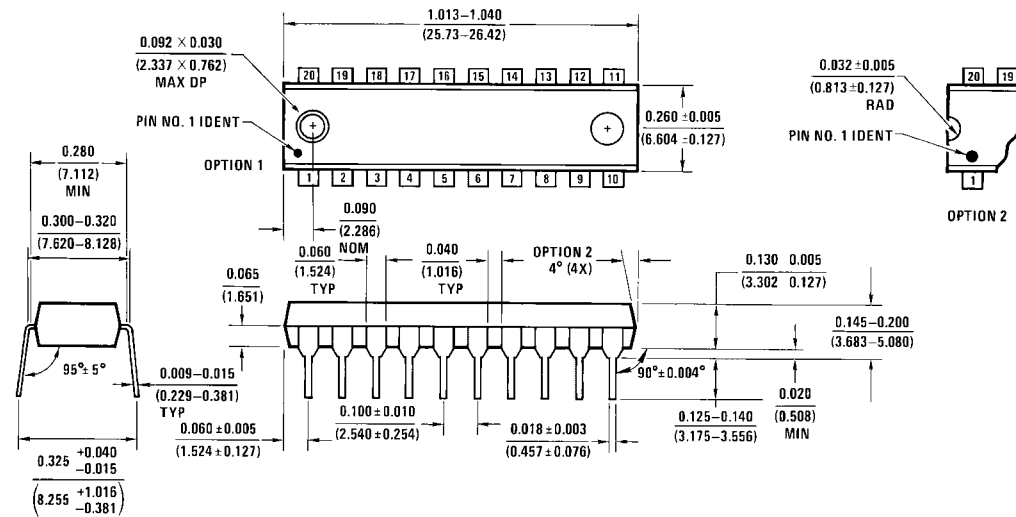
## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	4.0	14.5	18.5	3.5	19.5	ns
t <sub>PHL</sub>	A <sub>n</sub> to O <sub>n</sub>	4.0	9.5	12.0	4.0	13.0	
t <sub>PLH</sub>	Propagation Delay	5.0	12.0	16.0	5.5	17.0	ns
t <sub>PHL</sub>	$\bar{E}$ to O <sub>n</sub>	4.0	7.5	9.5	4.0	10.5	
t <sub>PLH</sub>	Propagation Delay	7.5	14.5	21.5	4.5	22.5	ns
t <sub>PHL</sub>	P to O <sub>n</sub>	5.0	11.0	16.5	4.5	17.5	
t <sub>pZH</sub>	Output Enable Time	4.5	8.0	10.5	4.0	11.5	ns
t <sub>pZL</sub>	$\bar{OE}$ to O <sub>n</sub>	5.5	10.0	13.0	5.0	14.0	
t <sub>pHZ</sub>	Output Disable Time	2.0	4.5	6.5	2.0	7.0	
t <sub>pLZ</sub>	$\bar{OE}$ to O <sub>n</sub>	3.0	6.5	8.5	3.0	9.5	

**Physical Dimensions** inches (millimeters) unless otherwise noted


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide  
Package Number M20B**

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N20A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)