

## 74F779

# 8-Bit Bidirectional Binary Counter with 3-STATE Outputs

### General Description

The 74F779 is a fully synchronous 8-stage up/down counter with multiplexed 3-STATE I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins ( $S_0$ ,  $S_1$ ). The device also features carry lookahead for easy cascading. All state changes are initiated by the rising edge of the clock.

### Features

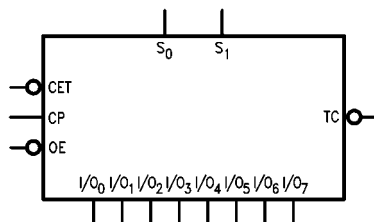
- Multiplexed 3-STATE I/O ports
- Built-in lookahead carry capability
- Count frequency 100 MHz typ
- Supply current 80 mA typ
- Available in SOIC (300 mil only)

### Ordering Code:

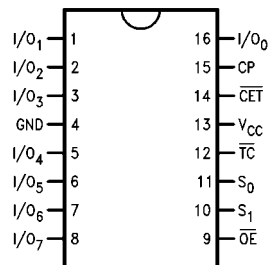
Order Number	Package Number	Package Description
74F779SC	M16B	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F779PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbol



### Connection Diagram



## Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$I/O_0-I/O_7$	Data Inputs	0.25/0.33	5 $\mu$ A/-0.2 mA
	Data Outputs	75/15 (12.5)	-3 mA/24 mA (20 mA)
$S_0, S_1$	Select Inputs	0.25/0.33	5 $\mu$ A/-0.2 mA
$\overline{OE}$	Output Enable Input (Active LOW)	0.25/0.33	5 $\mu$ A/-0.2 mA
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	0.25/0.33	5 $\mu$ A/-0.2 mA
CP	Clock Pulse Input (Active Rising Edge)	0.25/0.33	5 $\mu$ A/-0.2 mA
$\overline{TC}$	Terminal Count Output (Active LOW)	25/12.5	-1 mA/20 mA

## Function Table

$S_1$	$S_0$	$\overline{CET}$	$\overline{OE}$	CP	Function
X	X	X	H	X	$I/O_0$ to $I/O_7$ in High Z
X	X	X	L	X	Flip-Flop Outputs Appear on I/O Lines
L	L	X	H	$\nearrow$	Parallel Load All Flip-Flops
(Not LL)		H	X	$\nearrow$	Hold ( $\overline{TC}$ Held HIGH)
H	L	L	X	$\nearrow$	Count Up
L	H	L	X	$\nearrow$	Count Down

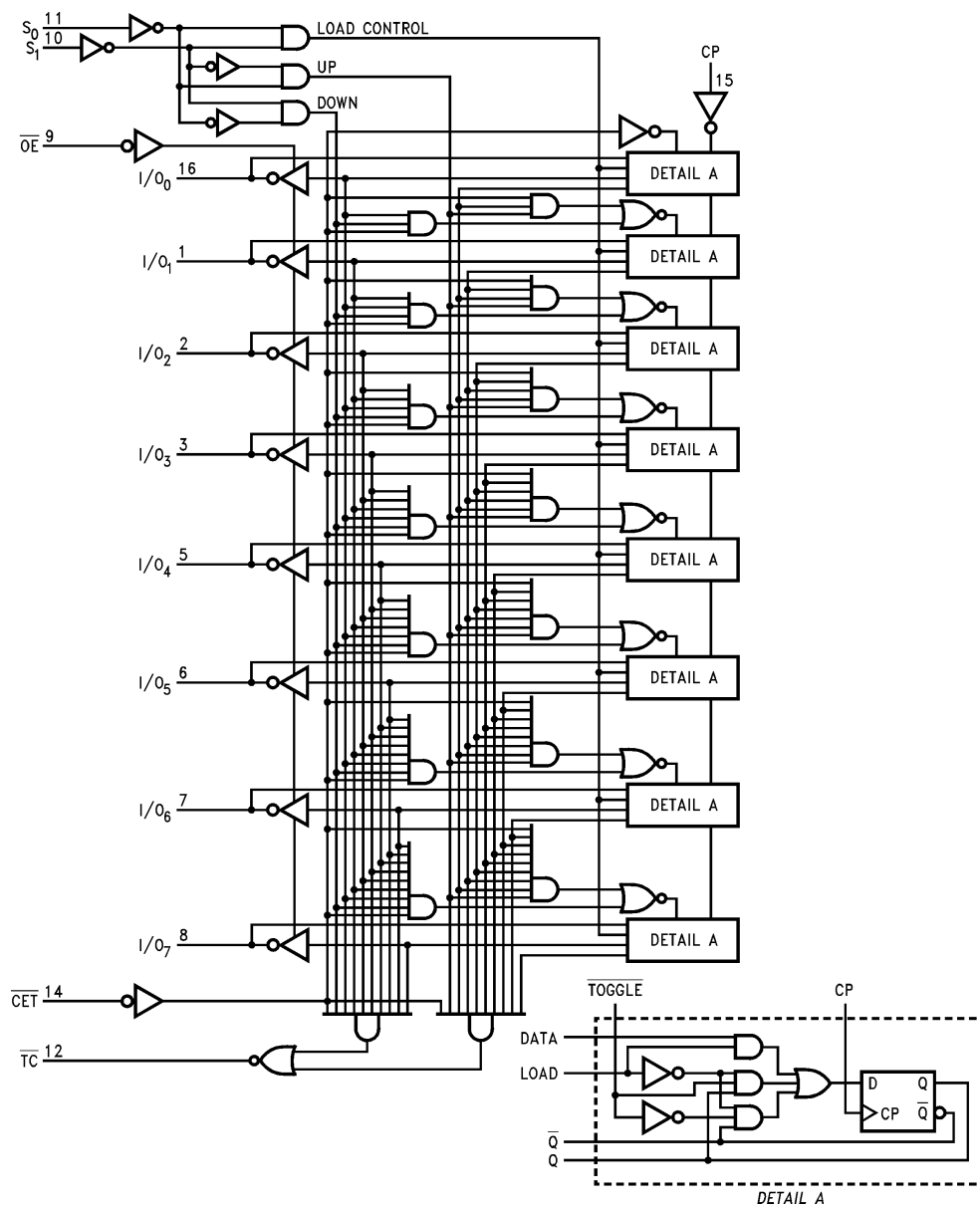
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

 $\nearrow$  = LOW-to-HIGH Clock Transition(Not LL) means  $S_0$  and  $S_1$  should never both be LOW level at the same time.

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current ((Note 2)	–30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	–0.5V to V <sub>CC</sub>
3-STATE Output	–0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			–1.2	V	Min	I <sub>IN</sub> = –18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub> 5% V <sub>CC</sub>	2.4 2.7		V	Min	I <sub>OH</sub> = –3 mA
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub> 5% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V (Non-I/O Pins)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V (Non-I/O Pins)
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)			0.5	mA	Max	V <sub>IN</sub> = 5.5V (I/O <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All other pins grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All other pins grounded
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0	V <sub>OUT</sub> = 5.25V
I <sub>IL</sub>	Input LOW Current			–0.2	mA	Max	V <sub>IN</sub> = 0.5V (Non I/O Pins)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (I/O <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			–200	μA	Max	V <sub>OUT</sub> = 0.5V (I/O <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	–60		–150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current			90	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			105	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current			110	mA	Max	V <sub>O</sub> = HIGH Z

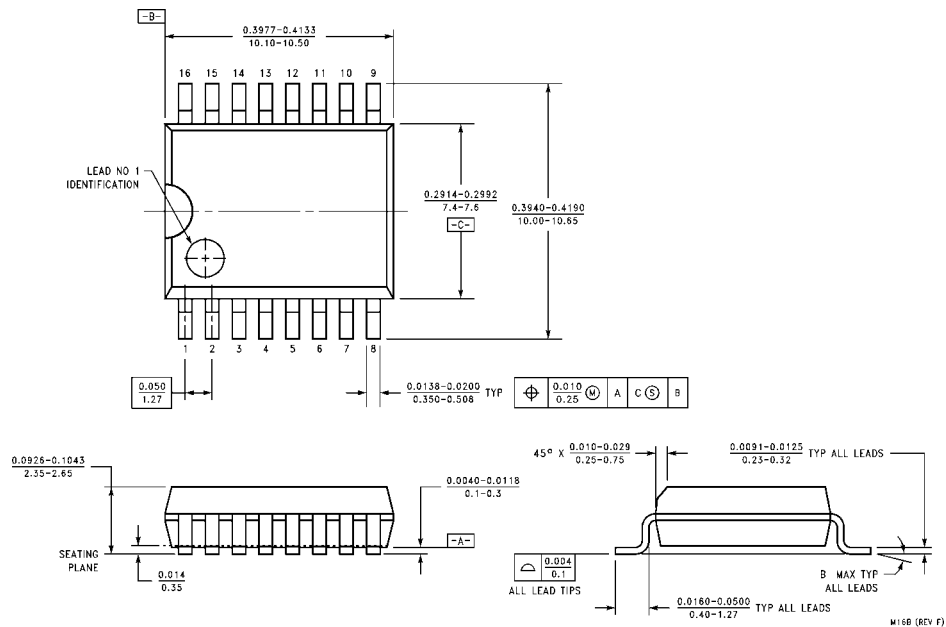
**AC Electrical Characteristics**

Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	
t <sub>MAX</sub>	Maximum Clock Frequency	100	105		90		
t <sub>PLH</sub>	Propagation Delay	3.0	5.0	8.0	3.0	8.5	ns
t <sub>PHL</sub>	CP to I/O <sub>n</sub>	5.0	7.5	11.0	5.0	11.0	
t <sub>PLH</sub>	Propagation Delay	5.0	7.5	9.0	5.0	10.0	ns
t <sub>PHL</sub>	CP to $\overline{\text{TC}}$	5.0	9.3	10.5	5.0	11.5	
t <sub>PLH</sub>	Propagation Delay	2.5	3.8	5.5	2.5	6.0	ns
t <sub>PHL</sub>	$\overline{\text{CET}}$ to $\overline{\text{TC}}$	4.5	6.1	8.0	4.5	8.5	
t <sub>PLH</sub>	Propagation Delay	3.5	6.5	12.0	3.5	13.0	ns
t <sub>PHL</sub>	SN to $\overline{\text{TC}}$	3.5	7.5	12.0	3.5	13.0	
t <sub>PZH</sub>	Output Enable Time	3.0	5.0	7.0	3.0	8.0	ns
t <sub>PZL</sub>	$\overline{\text{OE}}$ to I/O <sub>n</sub>	5.0	8.0	10.0	5.0	10.5	
t <sub>PHZ</sub>	Output Disable Time	1.0	4.0	6.5	1.0	7.0	ns
t <sub>PLZ</sub>	$\overline{\text{OE}}$ to I/O <sub>n</sub>	1.0	3.7	6.5	1.0	7.0	

**AC Operating Requirements**

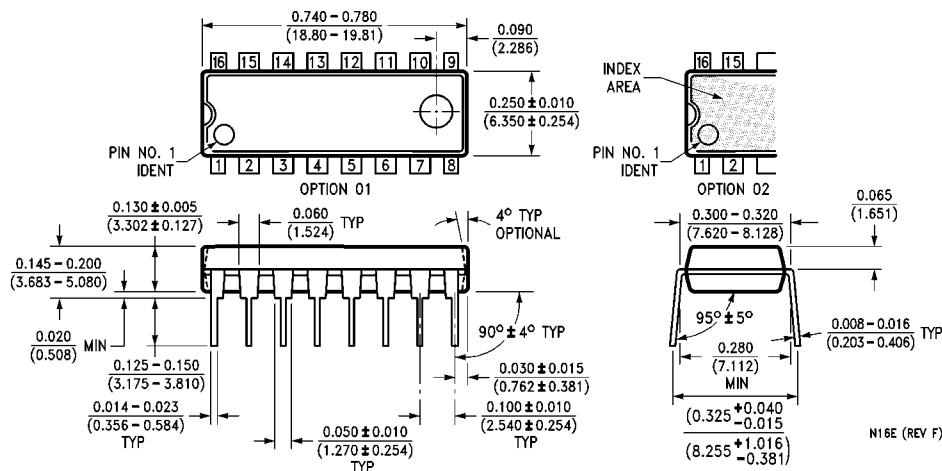
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V		Units
		Min	Max	Min	Max	
t <sub>S</sub> (H)	Setup Time	5.0		5.0		ns
t <sub>S</sub> (L)	I/O <sub>n</sub> to CP	5.0		5.0		
t <sub>H</sub> (H)	Hold Time	0.0		0.0		ns
t <sub>H</sub> (L)	I/O <sub>n</sub> to CP	0.0		0.0		
t <sub>S</sub> (H)	Setup Time	9.5		10.0		ns
t <sub>S</sub> (L)	S <sub>n</sub> to CP	9.5		10.0		
t <sub>H</sub> (H)	Hold Time	0.0		0.0		ns
t <sub>H</sub> (L)	S <sub>n</sub> to CP	0.0		0.0		
t <sub>S</sub> (H)	Setup Time	7.0		7.0		ns
t <sub>S</sub> (L)	$\overline{\text{CET}}$ to CP	7.0		7.0		
t <sub>H</sub> (H)	Hold Time	0.0		0.0		ns
t <sub>H</sub> (L)	$\overline{\text{CET}}$ to CP	0.0		0.0		
t <sub>W</sub> (H)	Clock Pulse Width	4.0		4.0		ns
t <sub>W</sub> (L)	HIGH or LOW	4.0		4.0		

# Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide  
Package Number M16B**

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N16E

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