



August 2001
Revised August 2001

74LCX32652

Low Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs (Preliminary)

General Description

The LCX32652 contains thirty-two non-inverting bidirectional bus transceivers with 3-STATE outputs providing multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to the HIGH logic level. Each byte has separate control inputs which can be shorted together for full 32-bit operation. Output Enable pins ($OEAB_n$, $OEBA_n$) are provided to control the transceiver function (see Functional Description).

The LCX32652 is designed for low-voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX32652 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 5.7 ns t_{PD} max ($V_{CC} = 3.3V$), 20 μA I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ± 24 mA output drive ($V_{CC} = 3.0V$)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V
- Packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

Note 1: To ensure the high-impedance state during power up or down, \overline{OE} should be tied to V_{CC} and OE tied to GND through a resistor; the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

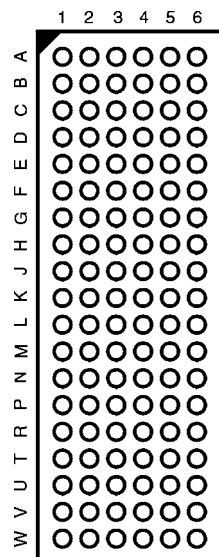
Order Number	Package Number	Package Description
74LCX32652GX (Note 2)	BGA114A (Preliminary)	114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]

Note 2: BGA package available in Tape and Reel only.

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Connection Diagram

Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Names	Description
1A ₀ - 1A ₁₅	Data Register A Inputs/3-STATE Outputs
2A ₀ - 2A ₁₅	
1B ₀ - 1B ₁₅	Data Register B Inputs/3-STATE Outputs
2B ₀ - 2B ₁₅	
CPAB _n , CPBA _n	Clock Pulse Inputs
SAB _n , SBA _n	Select Inputs
OEAB _n , OEBA _n	Output Enable Inputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	1A ₀	SAB ₁	CPAB ₁	CPBA ₁	SBA ₁	1B ₀
B	1A ₂	1A ₁	OEAB ₁	OEBA ₁	1B ₁	1B ₂
C	1A ₄	1A ₃	GND	GND	1B ₃	1B ₄
D	1A ₆	1A ₅	V _{CC}	V _{CC}	1B ₅	1B ₆
E	1A ₈	1A ₇	GND	GND	1B ₇	1B ₈
F	1A ₁₀	1A ₉	GND	GND	1B ₉	1B ₁₀
G	1A ₁₂	1A ₁₁	V _{CC}	V _{CC}	1B ₁₁	1B ₁₂
H	1A ₁₃	1A ₁₄	GND	GND	1B ₁₄	1B ₁₃
J	1A ₁₅	SAB ₂	CPAB ₂	CPBA ₂	SBA ₂	1B ₁₅
K	NC	CPAB ₃	OEAB ₂	OEBA ₂	CPBA ₃	NC
L	2A ₀	SAB ₃	OEAB ₃	OEBA ₃	SBA ₃	2B ₀
M	2A ₂	2A ₁	GND	GND	2B ₁	2B ₂
N	2A ₄	2A ₃	V _{CC}	V _{CC}	2B ₃	2B ₄
P	2A ₆	2A ₅	GND	GND	2B ₅	2B ₆
R	2A ₈	2A ₇	GND	GND	2B ₇	2B ₈
T	2A ₁₀	2A ₉	V _{CC}	V _{CC}	2B ₉	2B ₁₀
U	2A ₁₂	2A ₁₁	GND	GND	2B ₁₁	2B ₁₂
V	2A ₁₃	2A ₁₄	CPAB ₄	CPBA ₄	2B ₁₄	2B ₁₃
W	2A ₁₅	SAB ₄	OEAB ₄	OEBA ₄	SBA ₄	2B ₁₅

Truth Table

(Note 3)

Inputs						Inputs/Outputs (Note 4)		Operating Mode
OEAB ₁	OEBA ₁	CPAB ₁	CPBA ₁	SAB ₁	SBA ₁	1A ₀ thru 1A ₇	1B ₀ thru 1B ₇	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↘	↘	X	X			Store A and B Data
X	H	↘	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	↘	↘	X	X	Input	Output	Store A in Both Registers
L	X	H or L	↘	X	X	Not Specified	Input	Hold A, Store B
L	L	↘	↘	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

↘ = LOW-to-HIGH Clock Transition

Note 3: Data I/O paths (1A and 1B: 0 - 7) is shown. This also applies to data I/O (1A and 1B: 8 - 15) and #2 control pins, to data (2A and 2B: 0 - 7) and #3 control pins, to data (2A and 2B: 8 - 15) and #4 control pins.

Note 4: The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

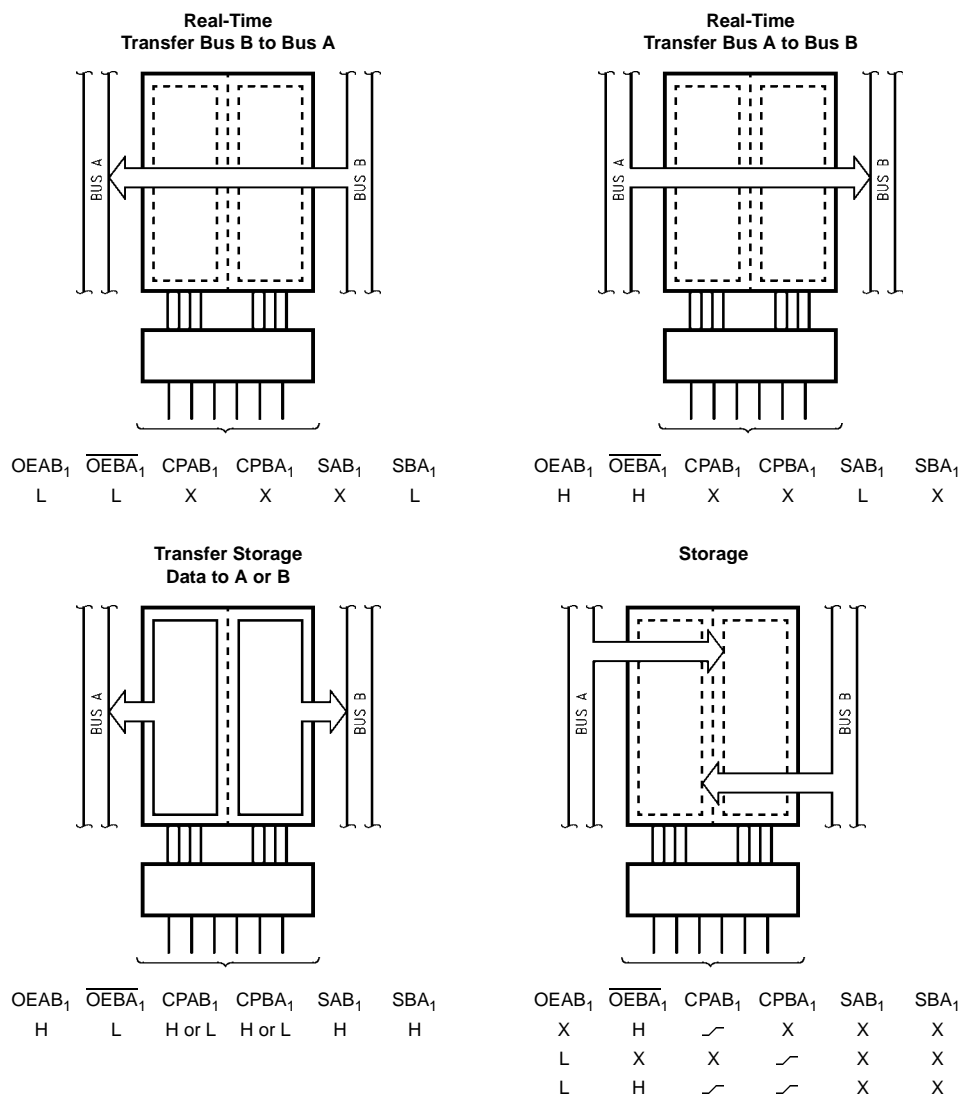
Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

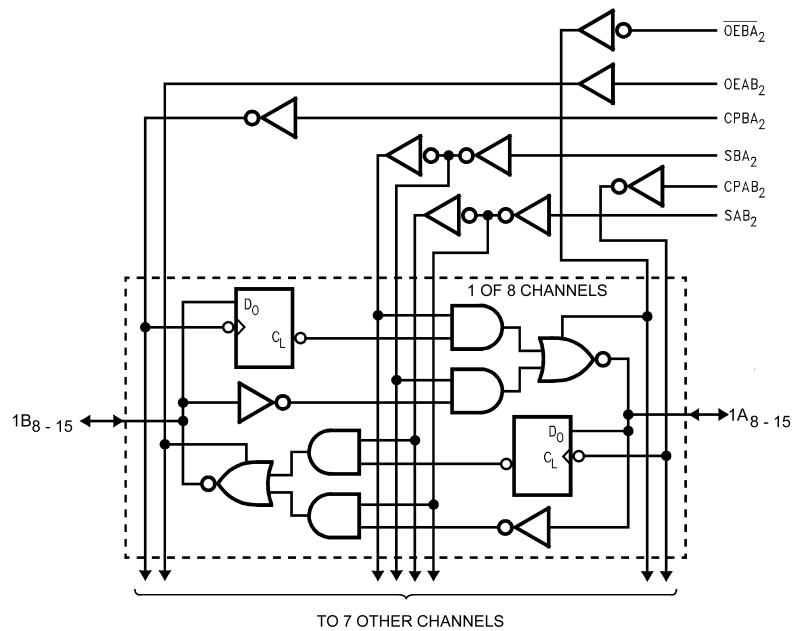
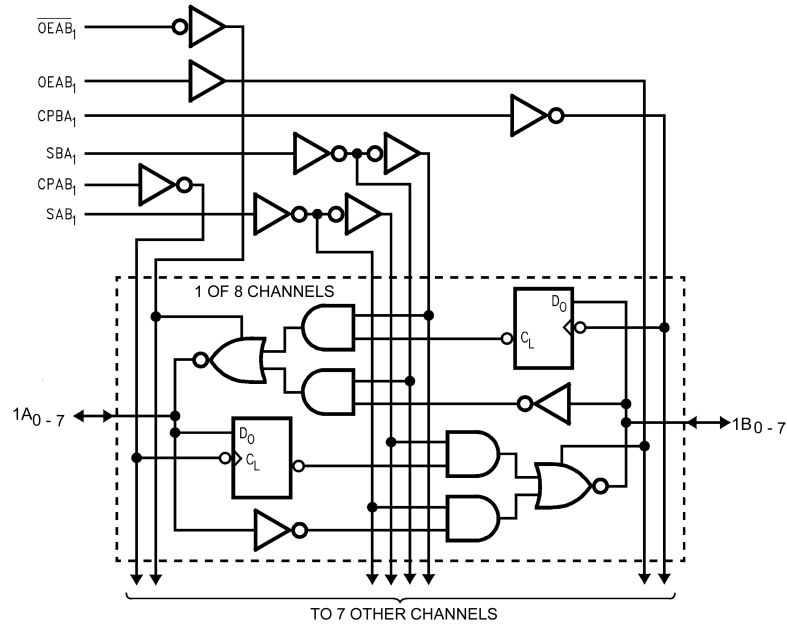
The select (SAB_n , SBA_n) controls can multiplex stored and real-time.

The examples below demonstrate the four fundamental bus-management functions that can be performed with the 74LCX32652 for data register I/O 1A and 1B: 0 - 7.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW-to-HIGH transitions at the appropriate Clock Inputs ($CPAB_n$, $CPBA_n$) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling $OEAB_n$ and $OEBA_n$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

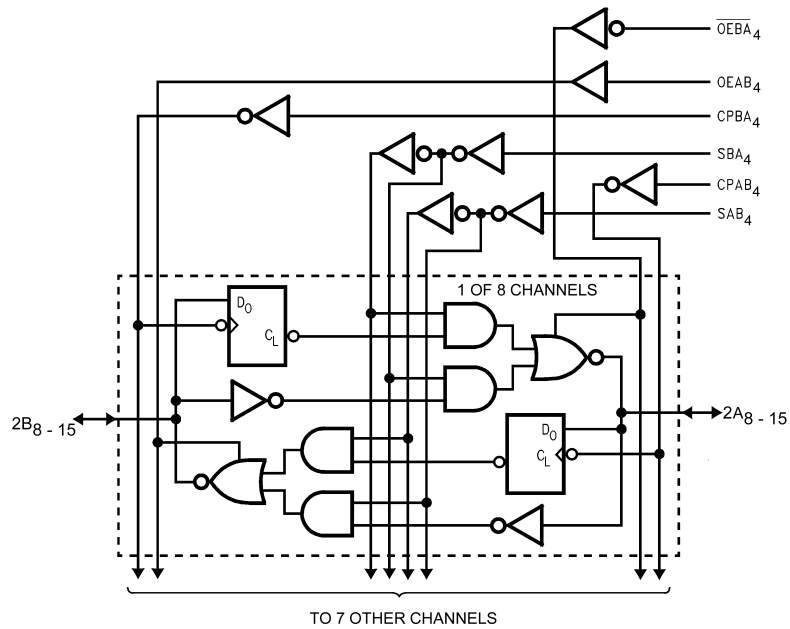
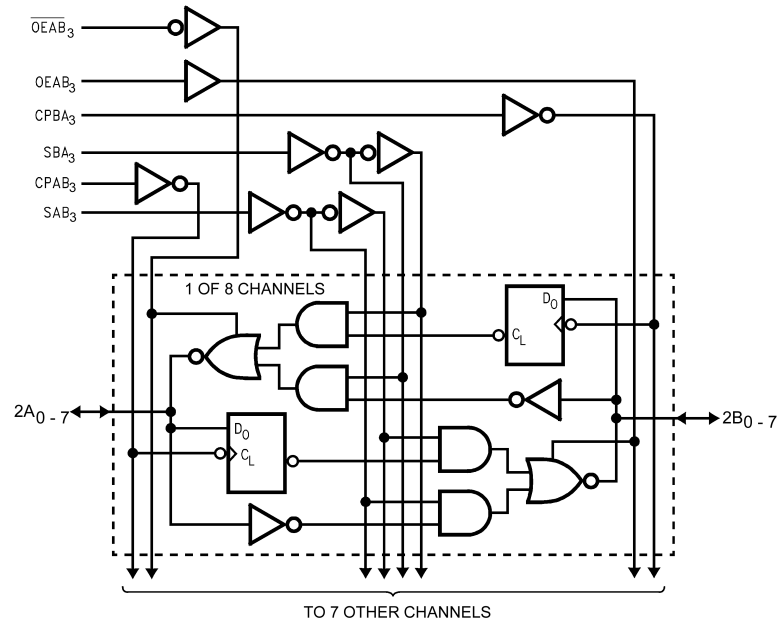


Logic Diagrams



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagrams (Continued)



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings ^(Note 5)				
Symbol	Parameter	Value	Conditions	Units
V _{CC}	Supply Voltage	−0.5 to +7.0		V
V _I	DC Input Voltage	−0.5 to +7.0		V
V _O	DC Output Voltage	−0.5 to +7.0 −0.5 to V _{CC} + 0.5	Output in 3-STATE Output in HIGH or LOW State (Note 6)	V
I _{IK}	DC Input Diode Current	−50	V _I < GND	mA
I _{OK}	DC Output Diode Current	−50 +50	V _O < GND V _O > V _{CC}	mA
I _O	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supply Current per Supply Pin	±100		mA
I _{GND}	DC Ground Current per Ground Pin	±100		mA
T _{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions ^(Note 7)

Symbol	Parameter	Min	Max	Units	
V _{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V _I	Input Voltage	0	5.5	V	
V _O	Output Voltage	HIGH or LOW State	0	V _{CC}	V
		3-STATE	0	5.5	
I _{OH} /I _{OL}	Output Current	V _{CC} = 3.0V – 3.6V		±24	mA
		V _{CC} = 2.7V – 3.0V		±12	
		V _{CC} = 2.3V – 2.7V		±8	
T _A	Free-Air Operating Temperature	−40	85	°C	
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V–2.0V, V _{CC} = 3.0V	0	10	ns/V	

Note 5: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

Note 6: I_O Absolute Maximum Rating must be observed.

Note 7: Unused (inputs or I/O’s) must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = −40°C to +85°C		Units
				Min	Max	
V _{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V _{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V _{OH}	HIGH Level Output Voltage	I _{OH} = −100 μA	2.3 – 3.6	V _{CC} − 0.2		V
		I _{OH} = −8 mA	2.3	1.8		
		I _{OH} = −12 mA	2.7	2.2		
		I _{OH} = −18 mA	3.0	2.4		
		I _{OH} = −24 mA	3.0	2.2		
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.3 – 3.6		0.2	V
		I _{OL} = 8 mA	2.3		0.6	
		I _{OL} = 12 mA	2.7		0.4	
		I _{OL} = 16 mA	3.0		0.4	
		I _{OL} = 24 mA	3.0		0.55	
I _I	Input Leakage Current	0 ≤ V _I ≤ 5.5V	2.3 – 3.6		±5.0	μA
I _{OZ}	3-STATE I/O Leakage	0 ≤ V _O ≤ 5.5V V _I = V _{IH} or V _{IL}	2.3 – 3.6		±5.0	μA
I _{OFF}	Power-Off Leakage Current	V _I or V _O = 5.5V	0		10	μA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units
				Min	Max	
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	2.3 – 3.6		20	μA
		3.6V ≤ V _I , V _O ≤ 5.5V (Note 8)	2.3 – 3.6		±20	
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} -0.6V	2.3 – 3.6		500	μA

Note 8: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

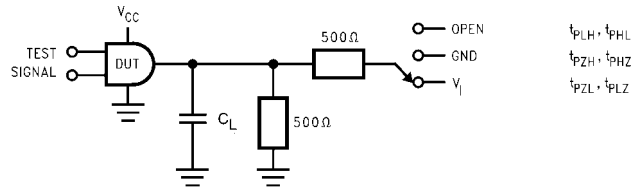
Symbol	Parameter	T _A = -40°C to +85°C, R _L = 500Ω						Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2V		
		C _L = 50 pF		C _L = 50 pF		C _L = 30 pF		
		Min	Max	Min	Max	Min	Max	
t _{MAX}	Maximum Clock Frequency	170						MHz
t _{PHL}	Propagation Delay	1.5	5.7	1.5	6.2	1.5	6.8	ns
t _{PLH}	Bus to Bus	1.5	5.7	1.5	6.2	1.5	6.8	
t _{PHL}	Propagation Delay	1.5	6.2	1.5	7.0	1.5	7.4	ns
t _{PLH}	Clock to Bus	1.5	6.2	1.5	7.0	1.5	7.4	
t _{PHL}	Propagation Delay	1.5	6.5	1.5	7.0	1.5	7.8	ns
t _{PLH}	Select to Bus	1.5	6.5	1.5	7.0	1.5	7.8	
t _{PZL}	Output Enable Time	1.5	7.0	1.5	8.0	1.5	9.1	ns
t _{PZH}		1.5	7.0	1.5	8.0	1.5	9.1	
t _{PLZ}	Output Disable Time	1.5	6.5	1.5	7.0	1.5	7.8	ns
t _{PHZ}		1.5	6.5	1.5	7.0	1.5	7.8	
t _S	Setup Time	2.5		2.5		3.0		ns
t _H	Hold Time	1.5		1.5		2.0		ns
t _W	Pulse Width	3.0		3.0		3.5		ns

Dynamic Switching Characteristics

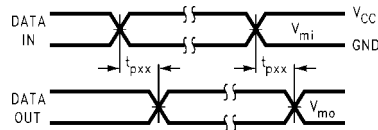
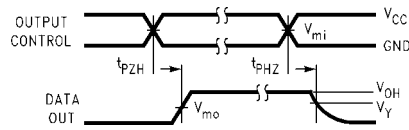
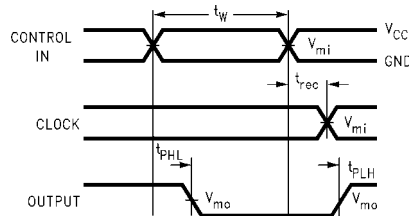
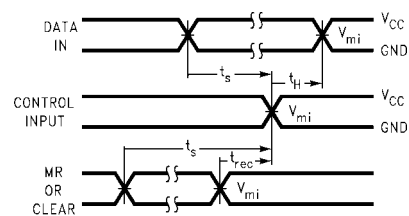
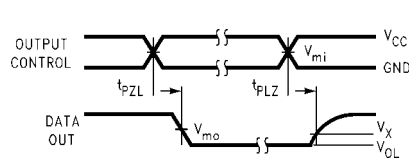
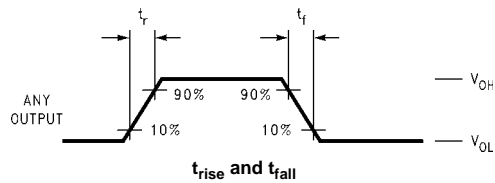
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C	Units
				Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V
		C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	2.5	0.6	
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	-0.8	V
		C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	2.5	-0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = Open, V _I = 0V or V _{CC}	7	pF
C _{I/O}	Input/Output Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC} , f = 10 MHz	20	pF

AC LOADING and WAVEFORMS Generic for LCX Family**FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)**

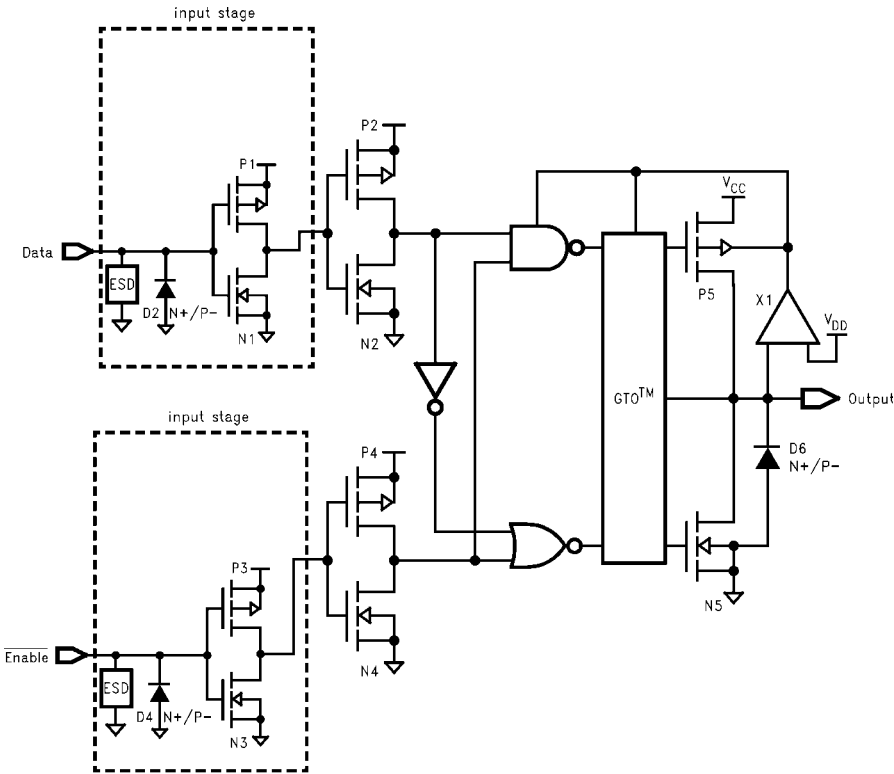
Test	Switch
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$, and 2.7V $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
t_{PZH} , t_{PHZ}	GND

**Waveform for Inverting and Non-Inverting Functions****3-STATE Output High Enable and Disable Times for Logic****Propagation Delay, Pulse Width and t_{rec} Waveforms****Setup Time, Hold Time and Recovery Time for Logic****3-STATE Output Low Enable and Disable Times for Logic****FIGURE 2. Waveforms**
(Input Characteristics; $f = 1 \text{ MHz}$, $t_r = t_f = 3 \text{ ns}$)

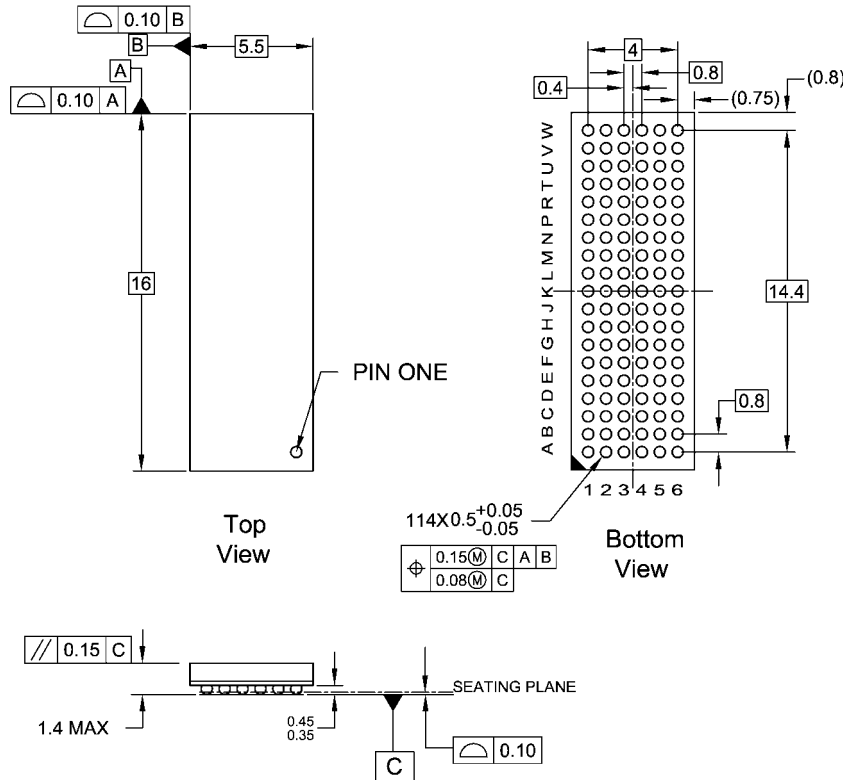
Symbol	V_{CC}		
	$3.3V \pm 0.3V$	2.7V	$2.5V \pm 0.2V$
V_{mi}	1.5V	1.5V	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

74LCX32652

Schematic Diagram Generic for LCX Family



Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA114ArevE

114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA114A
Preliminary

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