

## 74LCX86

### Low Voltage Quad 2-Input Exclusive-OR Gate with 5V Tolerant Inputs

#### General Description

The LCX86 contains four 2-input exclusive-OR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

The 74LCX86 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

#### Features

- 5V tolerant inputs
- 2.3V–3.6V  $V_{CC}$  specifications provided
- 6.5 ns  $t_{PD}$  max ( $V_{CC} = 3.3V$ ), 10  $\mu A$   $I_{CC}$  max
- Power down high impedance inputs and outputs
- $\pm 24$  mA output drive ( $V_{CC} = 3.0V$ )
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Machine model > 2000V
  - Human model > 200V

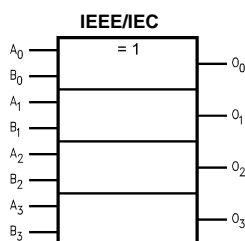
#### Ordering Code:

Order Number	Package Number	Package Description
74LCX86M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LCX86SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX86MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LCX86MTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

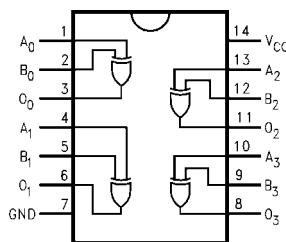
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.  
Pb-Free package per JEDEC J-STD-020B.

**Note 1:** "\_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

#### Logic Symbol



#### Connection Diagram



#### Pin Descriptions

Pin Names	Description
A <sub>0</sub> –A <sub>3</sub>	Inputs
B <sub>0</sub> –B <sub>3</sub>	Inputs
O <sub>0</sub> –O <sub>3</sub>	Outputs

**Absolute Maximum Ratings** (Note 2)

Symbol	Parameter	Value	Conditions	Units
V <sub>CC</sub>	Supply Voltage	−0.5 to +7.0		V
V <sub>I</sub>	DC Input Voltage	−0.5 to +7.0		V
V <sub>O</sub>	DC Output Voltage	−0.5 to V <sub>CC</sub> + 0.5	Output in HIGH or LOW State (Note 3)	V
I <sub>IK</sub>	DC Input Diode Current	−50	V <sub>I</sub> < GND	mA
I <sub>OK</sub>	DC Output Diode Current	−50 +50	V <sub>O</sub> < GND V <sub>O</sub> > V <sub>CC</sub>	mA
I <sub>O</sub>	DC Output Source/Sink Current	±50		mA
I <sub>CC</sub>	DC Supply Current per Supply Pin	±100		mA
I <sub>GND</sub>	DC Ground Current per Ground Pin	±100		mA
T <sub>STG</sub>	Storage Temperature	−65 to +150		°C

**Recommended Operating Conditions** (Note 4)

Symbol	Parameter	Min	Max	Units
V <sub>CC</sub>	Supply Voltage	Operating 2.0 Data Retention 1.5	3.6 3.6	V
V <sub>I</sub>	Input Voltage	0	5.5	V
V <sub>O</sub>	Output Voltage	HIGH or LOW State 0	V <sub>CC</sub>	V
I <sub>OH</sub> /I <sub>OL</sub>	Output Current	V <sub>CC</sub> = 3.0V – 3.6V V <sub>CC</sub> = 2.7V – 3.0V V <sub>CC</sub> = 2.3V – 2.7V	±24 ±12 ±8	mA
T <sub>A</sub>	Free-Air Operating Temperature	−40	85	°C
Δt/ΔV	Input Edge Rate, V <sub>IN</sub> = 0.8V–2.0V, V <sub>CC</sub> = 3.0V	0	10	ns/V

**Note 2:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 3:** I<sub>O</sub> Absolute Maximum Rating must be observed.

**Note 4:** Unused inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = −40°C to +85°C		Units
				Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage		2.3 – 2.7 2.7 – 3.6	1.7 2.0		V
V <sub>IL</sub>	LOW Level Input Voltage		2.3 – 2.7 2.7 – 3.6		0.7 0.8	V
V <sub>OH</sub>	HIGH Level Output Voltage	I <sub>OH</sub> = −100μA I <sub>OH</sub> = −8 mA I <sub>OH</sub> = −12 mA I <sub>OH</sub> = −18 mA I <sub>OH</sub> = −24 mA	2.3 – 3.6 2.3 2.7 3.0 3.0	V <sub>CC</sub> − 0.2 1.8 2.2 2.4 2.2		V
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100μA I <sub>OL</sub> = 8mA I <sub>OL</sub> = 12 mA I <sub>OL</sub> = 16 mA I <sub>OL</sub> = 24 mA	2.3 – 3.6 2.3 2.7 3.0 3.0		0.2 0.6 0.4 0.4 0.55	V
I <sub>I</sub>	Input Leakage Current	0 ≤ V <sub>I</sub> ≤ 5.5V	2.3 – 3.6		±5.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	V <sub>I</sub> or V <sub>O</sub> = 5.5V	0		10	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND 3.6V ≤ V <sub>I</sub> ≤ 5.5V	2.3 – 3.6 2.3 – 3.6		10 ±10	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> − 0.6V	2.3 – 3.6		500	μA

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500Ω						Units
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 2.5V ± 0.2V		
		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 30 pF		
		Min	Max	Min	Max	Min	Max	
t <sub>PHL</sub>	Propagation Delay	1.5	6.5	1.5	7.0	1.5	7.8	ns
t <sub>PLH</sub>		1.5	6.5	1.5	7.0	1.5	7.8	
t <sub>OSHL</sub>	Output to Output Skew (Note 5)		1.0					ns
t <sub>OSLH</sub>			1.0					

**Note 5:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ).

## Dynamic Switching Characteristics

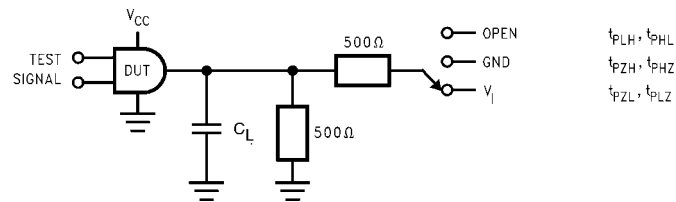
Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = 25^{\circ}\text{C}$	Units
				Typical	
$V_{OLP}$	Quiet Output Dynamic Peak $V_{OL}$	$C_L = 50\text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$ $C_L = 30\text{ pF}, V_{IH} = 2.5V, V_{IL} = 0V$	3.3 2.5	0.8 0.6	V
$V_{OLV}$	Quiet Output Dynamic Valley $V_{OL}$	$C_L = 50\text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$ $C_L = 30\text{ pF}, V_{IH} = 2.5V, V_{IL} = 0V$	3.3 2.5	-0.8 -0.6	V

## Capacitance

Symbol	Parameter	Conditions	Typical	Units
$C_{IN}$	Input Capacitance	$V_{CC} = \text{Open}, V_I = 0V \text{ or } V_{CC}$	7	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}$	8	pF
$C_{PD}$	Power Dissipation Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}, f = 10\text{ MHz}$	25	pF

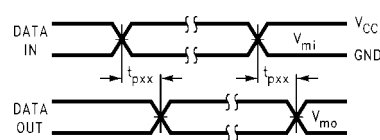
# AC Loading and Waveforms

Generic for LCX Family

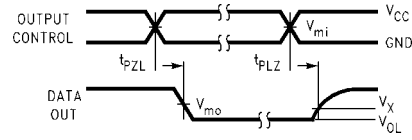
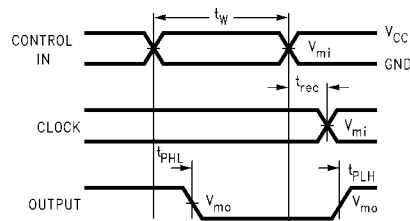


**FIGURE 1. AC Test Circuit**  
( $C_L$  includes probe and jig capacitance)

Test	Switch
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
$t_{PZH}, t_{PHZ}$	GND

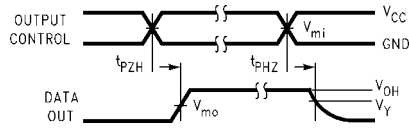


**Waveform for Inverting and Non-Inverting Functions**



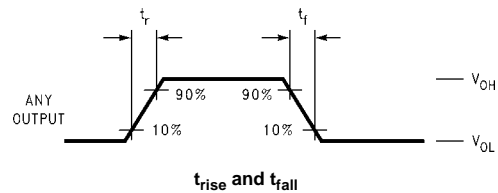
**3-STATE Output Low Enable and Disable Times for Logic**

**Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms**



**3-STATE Output High Enable and Disable Times for Logic**

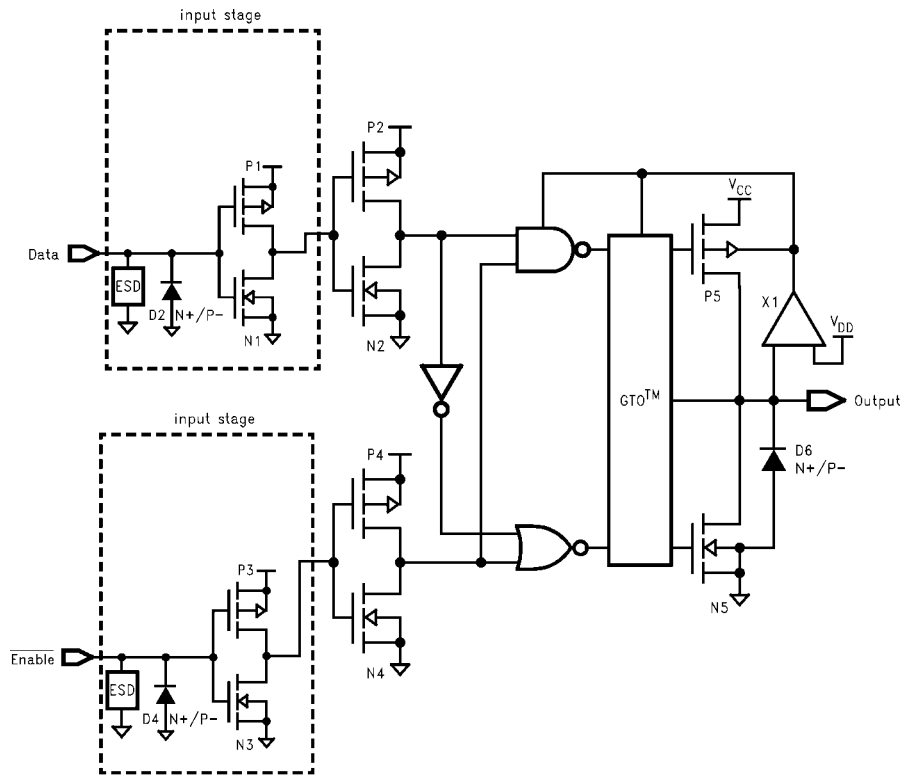
**Setup Time, Hold Time and Recovery Time for Logic**



**FIGURE 2. Waveforms**  
(Input Pulse Characteristics;  $f = 1\text{MHz}$ ,  $t_r = t_f = 3\text{ns}$ )

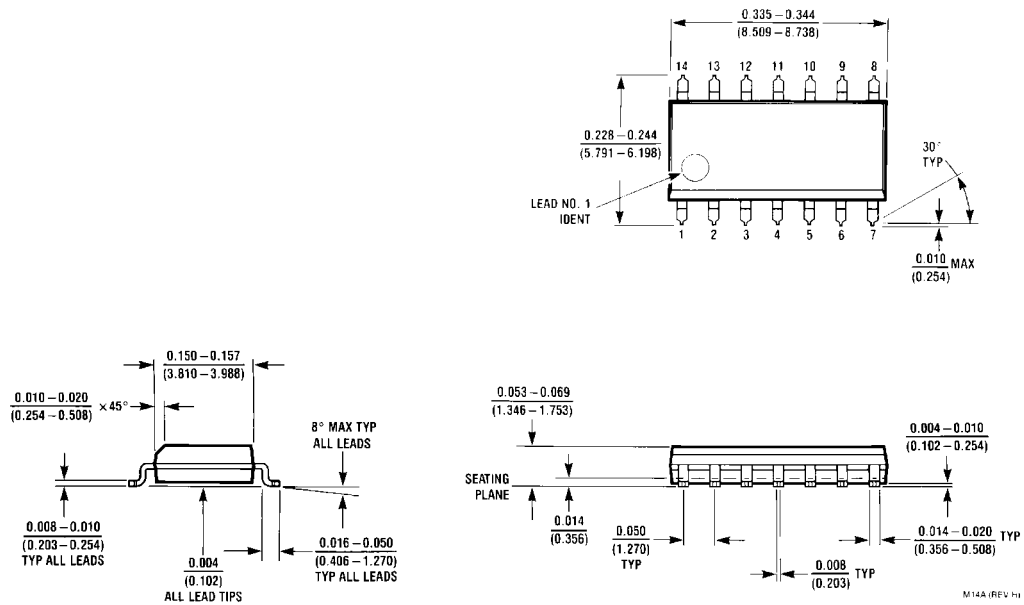
Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
$V_y$	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

# **Schematic Diagram** Generic for LCX Family



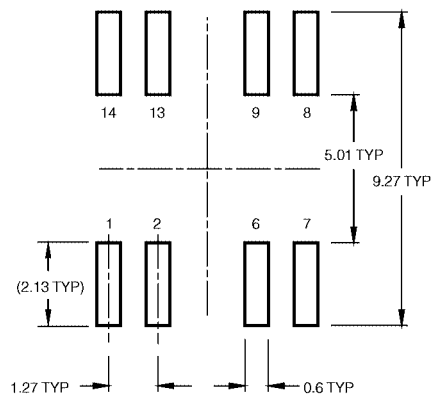
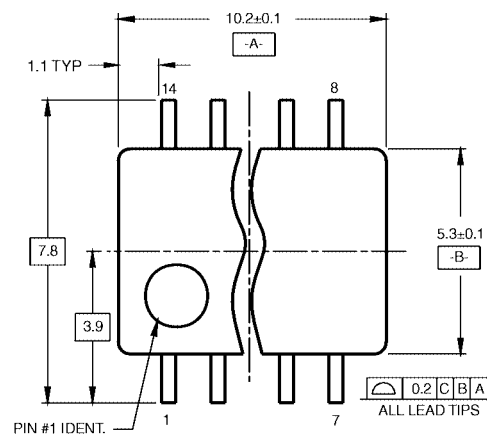
74LCX86

# Physical Dimensions inches (millimeters) unless otherwise noted

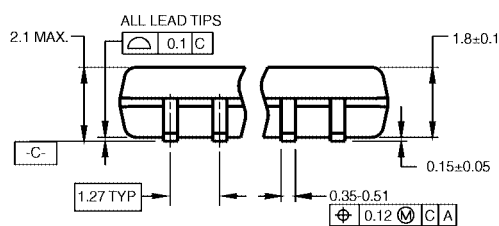


14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M14A

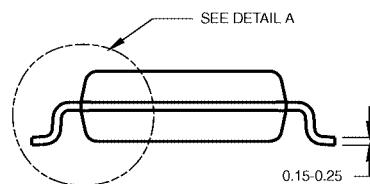
# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



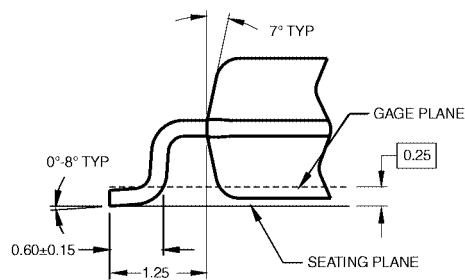
DIMENSIONS ARE IN MILLIMETERS



## NOTES:

- CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

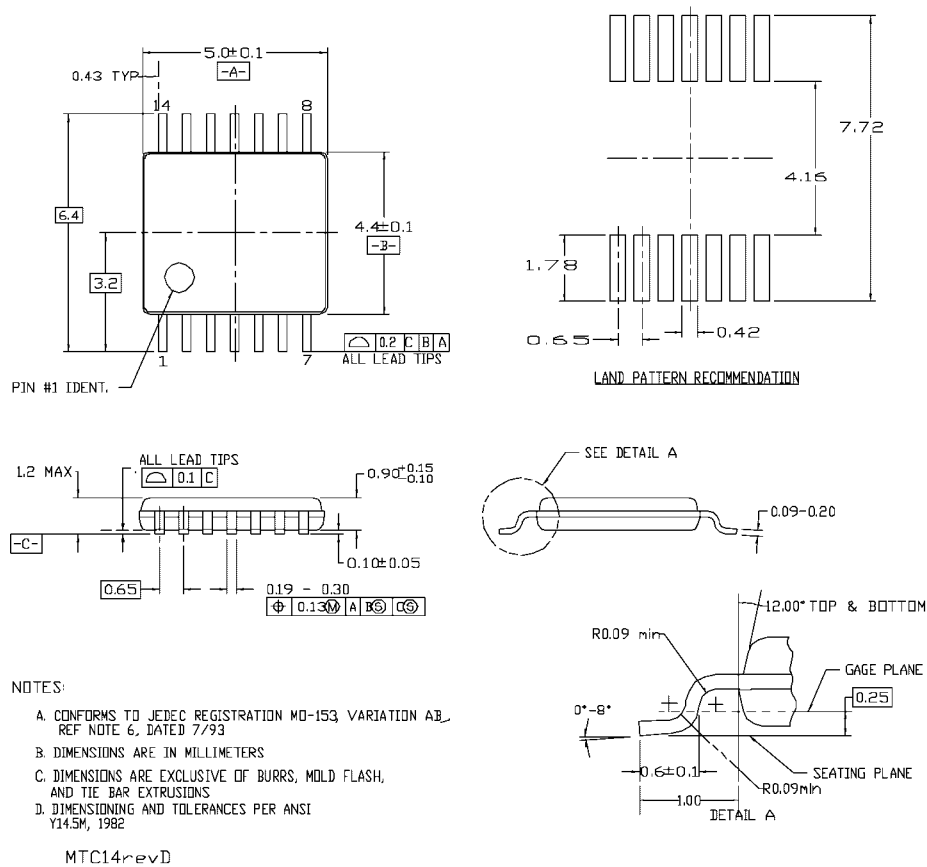
M14DRevB1



DETAIL A

**Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M14D**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC14

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)