

74LVT16543 • 74LVTH16543

Low Voltage 16-Bit Registered Transceiver with 3-STATE Outputs

General Description

The LVT16543 and LVTH16543 16-bit transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. Each byte has separate control inputs, which can be shorted together for full 16-bit operation.

The LVTH16543 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16543 and LVTH16543 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

Features

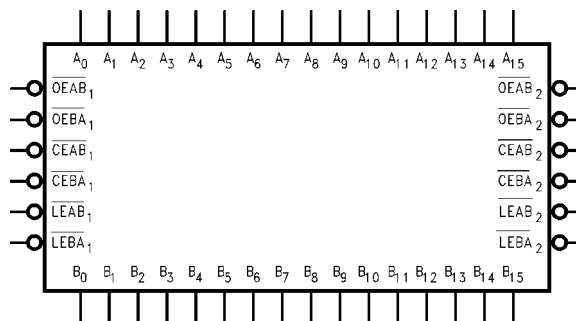
- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH16543)
- Also available without bushold feature (74LVT16543)
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Functionally compatible with the 74 series 16543
- Latch-up conforms to JEDEC JED78
- ESD performance:
 - Human-body model > 2000V
 - Machine model > 200V
 - Charged-device model > 1000V

Ordering Code:

Order Number	Package Number	Package Description
74LVT16543MEA (Preliminary)	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LVT16543MTD (Preliminary)	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
74LVTH16543MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LVTH16543MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

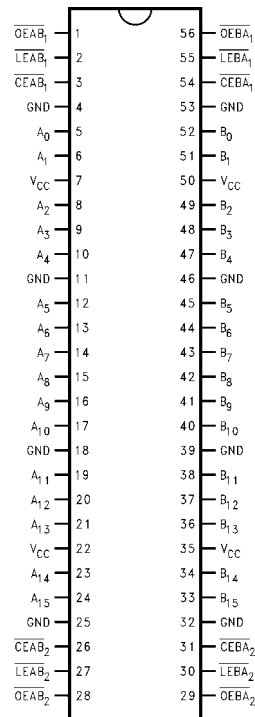
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



74LVT16543 • 74LVTH16543 Low Voltage 16-Bit Registered Transceiver with 3-STATE Outputs

Connection Diagram



Pin Descriptions

Pin Names	Description
\overline{OEAB}_n	A-to-B Output Enable Input (Active LOW)
\overline{OEBA}_n	B-to-A Output Enable Input (Active LOW)
\overline{CEAB}_n	A-to-B Enable Input (Active LOW)
\overline{CEBA}_n	B-to-A Enable Input (Active LOW)
\overline{LEAB}_n	A-to-B Latch Enable Input (Active LOW)
\overline{LEBA}_n	B-to-A Latch Enable Input (Active LOW)
A_0 – A_{15}	A-to-B Data Inputs or B-to-A 3-STATE Outputs
B_0 – B_{15}	B-to-A Data Inputs or A-to-B 3-STATE Outputs

Functional Description

The LVT16543 and LVTH16543 contain two sets of D-type latches, with separate input and output controls for each. For data flow from A to B, for example, the A to B Enable (\overline{CEAB}) input must be LOW in order to enter data from the A Port or take data from the B Port as indicated in the Data I/O Control Table. With \overline{CEAB} LOW, a low signal on (\overline{LEAB}) input makes the A to B latches transparent; a subsequent LOW-to-HIGH transition of the \overline{LEAB} line puts the

A latches in the storage mode and their outputs no longer change with the A inputs. With \overline{CEAB} and \overline{OEAB} both LOW, the B output buffers are active and reflect the data present on the output of the A latches. Control of data flow from B to A is similar, but using the \overline{CEBA} , \overline{LEBA} and \overline{OEBA} . Each byte has separate control inputs, allowing the device to be used as two 8-bit transceivers or as one 16-bit transceiver.

Data I/O Control Table

Inputs			Latch Status (Byte n)	Output Buffers (Byte n)
\overline{CEAB}_n	\overline{LEAB}_n	\overline{OEAB}_n		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

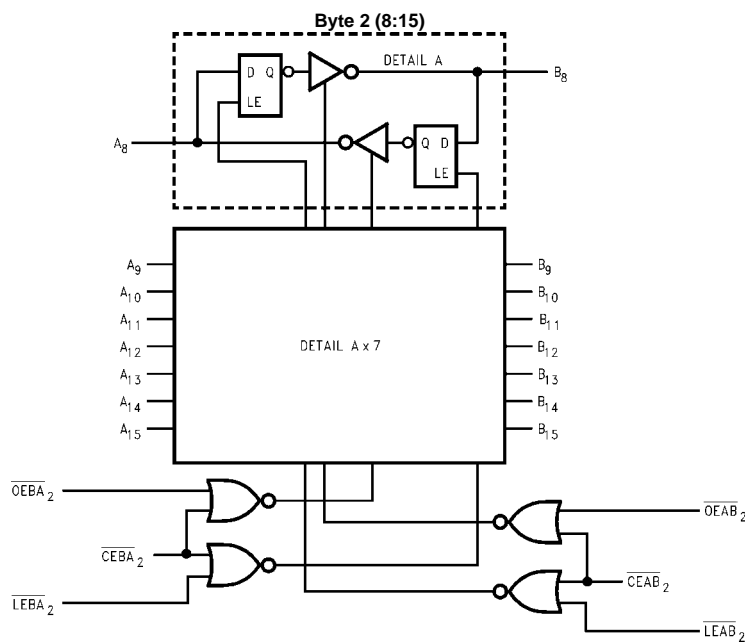
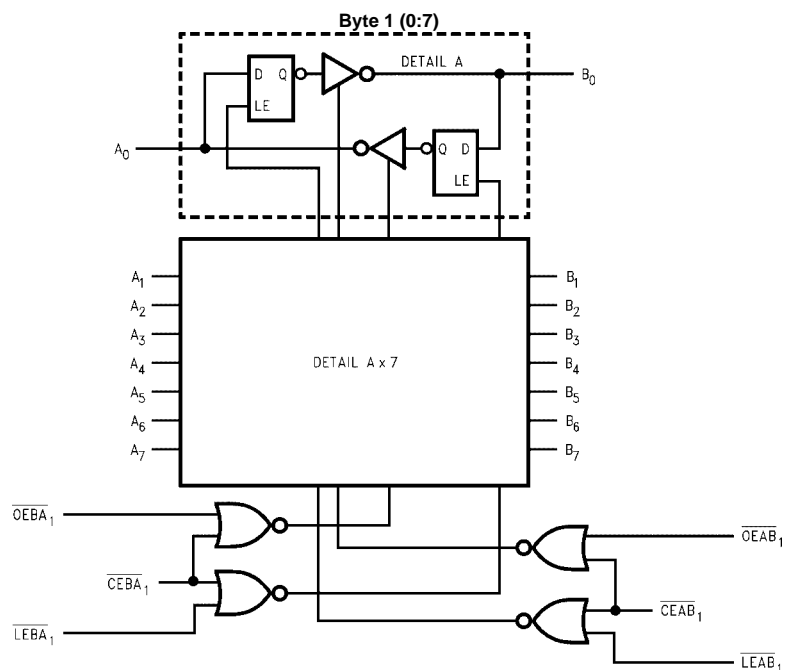
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

A-to-B data flow shown; B-to-A flow control is the same, except using \overline{CEBA}_n , \overline{LEBA}_n and \overline{OEBA}_n .

Logic Diagrams



Absolute Maximum Ratings(Note 1)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	–0.5 to +4.6		V
V_I	DC Input Voltage	–0.5 to +7.0		V
V_O	DC Output Voltage	–0.5 to +7.0	Output in 3-STATE	V
		–0.5 to +7.0	Output in HIGH or LOW State (Note 2)	V
I_{IK}	DC Input Diode Current	–50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	–50	$V_O < GND$	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	–65 to +150		°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH-Level Output Current		–32	mA
I_{OL}	LOW-Level Output Current		64	
T_A	Free-Air Operating Temperature	–40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V$ – $2.0V$, $V_{CC} = 3.0V$	0	10	ns/V

Note 1: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 2: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C		Units	Conditions
			Min	Max		
V _{IK}	Input Clamp Diode Voltage	2.7		-1.2	V	I _I = -18 mA
V _{IH}	Input HIGH Voltage	2.7-3.6	2.0		V	V _O ≤ 0.1V or V _O ≥ V _{CC} - 0.1V
V _{IL}	Input LOW Voltage	2.7-3.6		0.8		
V _{OH}	Output HIGH Voltage	2.7-3.6	V _{CC} - 0.2		V	I _{OH} = -100 μA
		2.7	2.4		V	I _{OH} = -8 mA
		3.0	2.0		V	I _{OH} = -32 mA
V _{OL}	Output LOW Voltage	2.7		0.2	V	I _{OL} = 100 μA
		2.7		0.5	V	I _{OL} = 24 mA
		3.0		0.4	V	I _{OL} = 16 mA
		3.0		0.5	V	I _{OL} = 32 mA
		3.0		0.55	V	I _{OL} = 64 mA
I _{I(HOLD)} (Note 3)	Bushold Input Minimum Drive	3.0	75		μA	V _I = 0.8V
			-75		μA	V _I = 2.0V
I _{I(OD)} (Note 3)	Bushold Input Over-Drive Current to Change State	3.0	500		μA	(Note 4)
			-500		μA	(Note 5)
I _I	Input Current	3.6		10	μA	V _I = 5.5V
	Control Pins	3.6		±1	μA	V _I = 0V or V _{CC}
	Data Pins	3.6		-5	μA	V _I = 0V
I _{OFF}	Power Off Leakage Current	0		±100	μA	V _I = V _{CC}
I _{PU/PD}	Power Up/Down 3-STATE Output Current	0-1.5V		±100	μA	0V ≤ V _I or V _O ≤ 5.5V
I _{OZL} (Note 3)	3-STATE Output Leakage Current	3.6		-5	μA	V _O = 0.0V
I _{OZL}	3-STATE Output Leakage Current	3.6		-5	μA	V _O = 0.5V
I _{OZH} (Note 3)	3-STATE Output Leakage Current	3.6		5	μA	V _O = 3.6V
I _{OZH}	3-STATE Output Leakage Current	3.6		5	μA	V _O = 3.0V
I _{OZH+}	3-STATE Output Leakage Current	3.6		10	μA	V _{CC} < V _O ≤ 5.5V
I _{CCH}	Power Supply Current	3.6		0.19	mA	Outputs HIGH
I _{CCL}	Power Supply Current	3.6		5	mA	Outputs LOW
I _{CCZ}	Power Supply Current	3.6		0.19	mA	Outputs Disabled
I _{CCZ+}	Power Supply Current	3.6		0.19	mA	V _{CC} ≤ V _O ≤ 5.5V, Outputs Disabled
ΔI _{CC}	Increase in Power Supply Current (Note 6)	3.6		0.2	mA	One Input at V _{CC} - 0.6V Other Inputs at V _{CC} or GND

Note 3: Applies to bushold versions only (74LVTH16543)

Note 4: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 5: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 6: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 7)

Symbol	Parameter	V _{CC} (V)	T _A = 25°C			Units	Conditions C _L = 50 pF, R _L = 500Ω
			Min	Typ	Max		
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3		0.8		V	(Note 8)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3		-0.8		V	(Note 8)

Note 7: Characterized in SSOP package. Guaranteed parameter, but not tested.

Note 8: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter		T _A = -40°C to +85°C C _L = 50 pF, R _L = 500 Ω				Units
			V _{CC} = 3.3 ± 0.3V		V _{CC} = 2.7V		
			Min	Max	Min	Max	
t _{PLH}	Propagation Delay		1.2	4.2	1.2	4.5	ns
t _{PHL}	Data to Outputs		1.2	4.4	1.2	4.9	
t _{PLH}	Propagation Delay		1.3	4.7	1.3	5.5	ns
t _{PHL}	\overline{LE} to A or B		1.3	5.1	1.3	5.8	
t _{PZH}	Output Enable Time		1.3	4.7	1.3	5.4	ns
t _{PZL}	\overline{OE} to A or B		1.3	5.1	1.3	6.1	
t _{PHZ}	Output Disable Time		2.0	5.5	2.0	5.7	ns
t _{PLZ}	\overline{OE} to A or B		2.0	4.9	2.0	4.9	
t _{PZH}	Output Enable Time		1.3	4.6	1.3	5.6	ns
t _{PZL}	\overline{CE} to A or B		1.3	5.0	1.3	6.1	
t _{PHZ}	Output Disable Time		2.0	5.5	2.0	5.8	ns
t _{PLZ}	\overline{CE} to A or B		2.0	4.9	2.0	4.9	
t _W	Pulse Duration \overline{LE} LOW		3.3		3.3		ns
t _S	Setup Time	A or B before \overline{LE} , Data HIGH	0.5		0.5		ns
		A or B before \overline{LE} , Data LOW	0.8		1.3		
		A or B before \overline{CE} , Data HIGH	0.5		0.0		
		A or B before \overline{CE} , Data LOW	0.6		1.1		
t _H	Hold Time	A or B after \overline{LE} , Data HIGH	1.5		0.7		ns
		A or B after \overline{LE} , Data LOW	1.2		1.3		
		A or B after \overline{CE} , Data HIGH	1.7		0.9		
		A or B after \overline{CE} , Data LOW	1.6		1.8		
t _{OSLH}	Output to Output Skew (Note 9)			1.0		1.0	ns
t _{OSHL}				1.0		1.0	

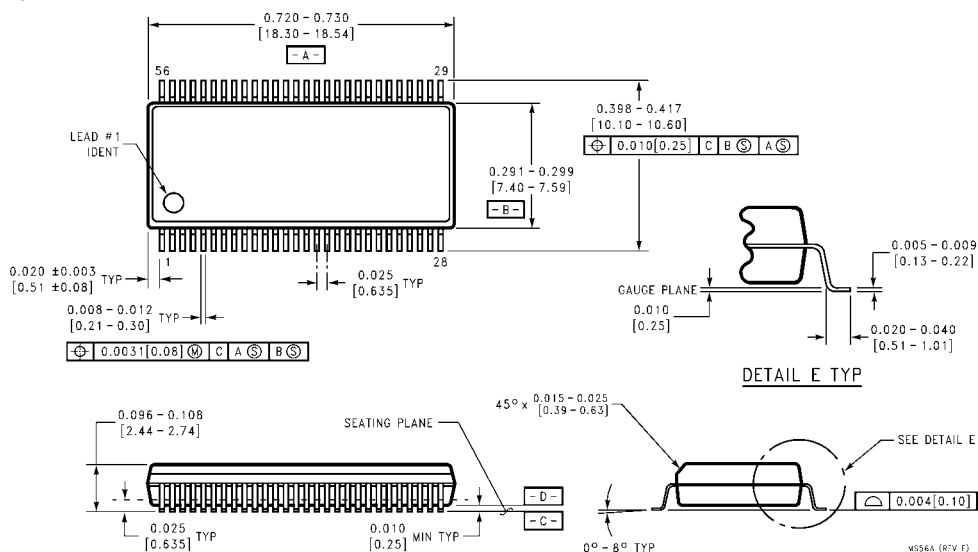
Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Capacitance (Note 10)

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = OPEN, V _I = 0V or V _{CC}	4	pF
C _{I/O}	Input/Output Capacitance	V _{CC} = 3.0V, V _O = 0V or V _{CC}	8	pF

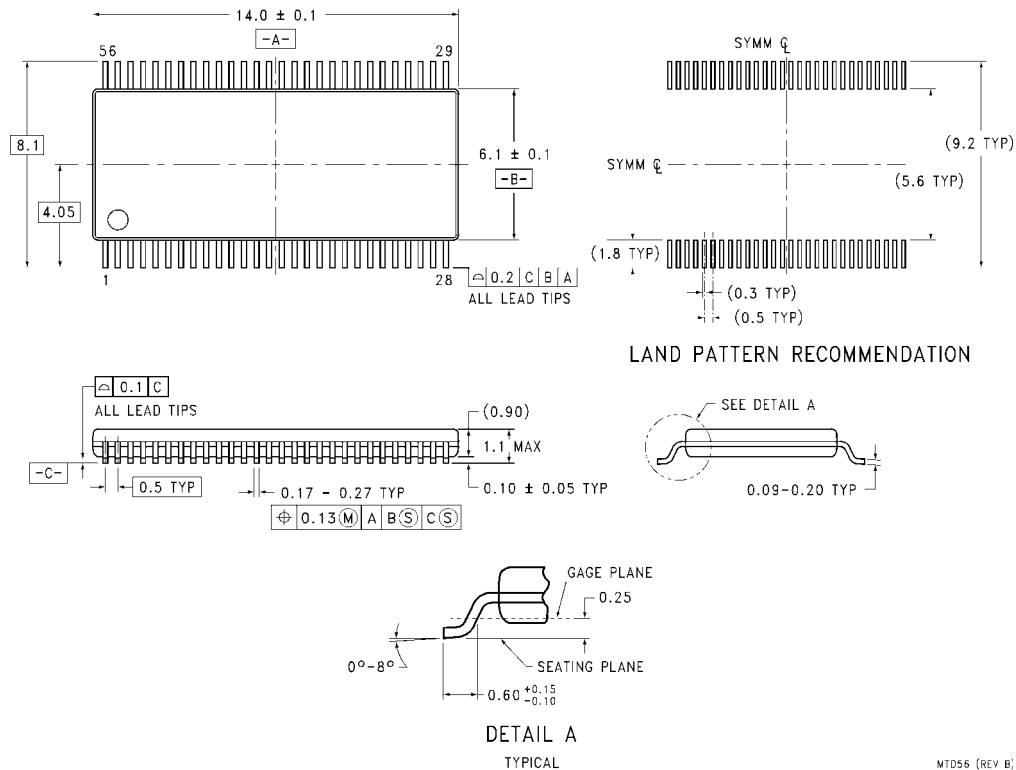
Note 10: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted



**56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS56A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com