

74VHCT14A Hex Schmitt Inverter

General Description

The VHCT14A is an advanced high speed CMOS Hex Schmitt Inverter fabricated with silicon gate CMOS technology. The VHCT14A contains six independent inverters which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

Protection circuits ensure that 0V to 7V can be applied to the input pins without regard to the supply voltage and to the output pins with $V_{CC} = 0V$. These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 3V to 5V systems and two supply systems such as battery backup.

Features

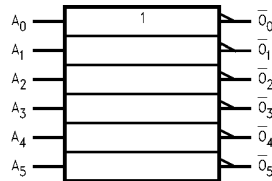
- High speed: $t_{PD} = 5.0$ ns (typ) at $T_A = 25^\circ C$
- High noise immunity: $V_{IH} = 2.0V$, $V_{IL} = 0.8V$
- Power down protection is provided on all inputs and outputs
- Low noise: $V_{OLP} = 1.0V$ (max)
- Low power dissipation:
 $I_{CC} = 2 \mu A$ (max) @ $T_A = 25^\circ C$
- Pin and function compatible with 74HCT14

Ordering Code:

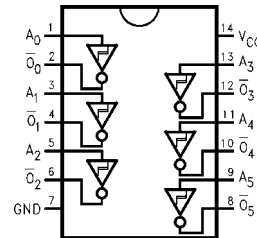
| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| 74VHCT14AM | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow |
| 74VHCT14ASJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74VHCT14AMTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74VHCT14AN | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

| Pin Names | Description |
|------------------|-------------|
| A_n | Inputs |
| \overline{O}_n | Outputs |

Truth Table

| A | \overline{O} |
|---|----------------|
| L | H |
| H | L |

Absolute Maximum Ratings (Note 1)

| | |
|---------------------------------------|--------------------------|
| Supply Voltage (V_{CC}) | –0.5V to +7.0V |
| DC Input Voltage (V_{IN}) | –0.5V to +7.0V |
| DC Output Voltage (V_{OUT}) | |
| (Note 2) | –0.5V to $V_{CC} + 0.5V$ |
| (Note 3) | –0.5V to 7.0V |
| Input Diode Current (I_{IK}) | –20 mA |
| Output Diode Current (I_{OK}) | |
| (Note 4) | ±20 mA |
| DC Output Current (I_{OUT}) | ±25 mA |
| DC V_{CC} /GND Current (I_{CC}) | ±50 mA |
| Storage Temperature (T_{STG}) | –65°C to +150°C |
| Lead Temperature (T_L) | |
| (Soldering, 10 seconds) | 260°C |

Recommended Operating Conditions (Note 5)

| | |
|-------------------------------------|----------------|
| Supply Voltage (V_{CC}) | 4.5V to +5.5V |
| Input Voltage (V_{IN}) | 0V to +5.5V |
| Output Voltage (V_{OUT}) | |
| (Note 2) | 0V to V_{CC} |
| (Note 3) | 0V to 5.5V |
| Operating Temperature (T_{OPR}) | –40°C to +85°C |

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: HIGH or LOW state. I_{OUT} absolute maximum rating must be observed.

Note 3: $V_{CC} = 0V$.

Note 4: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$ (Outputs Active)

Note 5: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

| Symbol | Parameter | V_{CC} (V) | $T_A = 25^\circ\text{C}$ | | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | Units | Conditions |
|-----------|--|-----------------|--------------------------|------|------|---|------|-------|---|
| | | | Min | Typ | Max | Min | Max | | |
| V_P | Positive Threshold Voltage | 4.5 | | | 1.9 | | 1.9 | V | |
| | | 5.5 | | | 2.1 | | 2.1 | | |
| V_N | Negative Threshold Voltage | 4.5 | 0.5 | | | 0.5 | | V | |
| | | 5.5 | 0.6 | | | 0.6 | | | |
| V_H | Hysteresis Voltage | 4.5 | 0.4 | | 1.4 | 0.4 | 1.4 | V | |
| | | 5.5 | 0.4 | | 1.5 | 0.4 | 1.5 | | |
| V_{OH} | HIGH Level Output Voltage | 4.5 | 4.40 | 4.50 | | 4.40 | | V | $V_{IN} = V_{IL}$ $I_{OH} = -50 \mu\text{A}$ |
| | | | 3.94 | | | 3.80 | | V | $I_{OH} = -8 \text{ mA}$ |
| V_{OL} | LOW Level Output Voltage | 4.5 | | 0.0 | 0.1 | | 0.1 | V | $V_{IN} = V_{IH}$ $I_{OL} = 50 \mu\text{A}$ |
| | | | | | 0.36 | | 0.44 | V | $I_{OL} = 8 \text{ mA}$ |
| I_{IN} | Input Leakage Current | 0 – 5.5 | | | ±0.1 | | ±1.0 | μA | $V_{IN} = 5.5V \text{ or } GND$ |
| I_{CC} | Quiescent Supply Current | 5.5 | | | 2.0 | | 20.0 | μA | $V_{IN} = V_{CC} \text{ or } GND$ |
| I_{CCT} | Maximum I_{CC} /Input | 5.5 | | | 1.35 | | 1.50 | mA | $V_{IN} = 3.4V$ Other Inputs = V_{CC} or GND |
| I_{OFF} | Output Leakage Current (Power Down State) | 0.0 | | | 0.5 | | 5.0 | μA | $V_{OUT} = 5.5V$ |

Noise Characteristics

| Symbol | Parameter | V_{CC} (V) | $T_A = 25^\circ\text{C}$ | | Units | Conditions |
|-----------------------|--|-----------------|--------------------------|--------|-------|-----------------------|
| | | | Typ | Limits | | |
| V_{OLP} (Note 6) | Quiet Output Maximum Dynamic V_{OL} | 5.0 | 0.8 | 1.0 | V | $C_L = 50 \text{ pF}$ |
| V_{OLV} (Note 6) | Quiet Output Minimum Dynamic V_{OL} | 5.0 | –0.8 | 1.0 | V | $C_L = 50 \text{ pF}$ |
| V_{IHD} (Note 6) | Minimum HIGH Level Dynamic Input Voltage | 5.0 | | 2.0 | V | $C_L = 50 \text{ pF}$ |
| V_{ILD} (Note 6) | Maximum LOW Level Dynamic Input Voltage | 5.0 | | 0.8 | V | $C_L = 50 \text{ pF}$ |

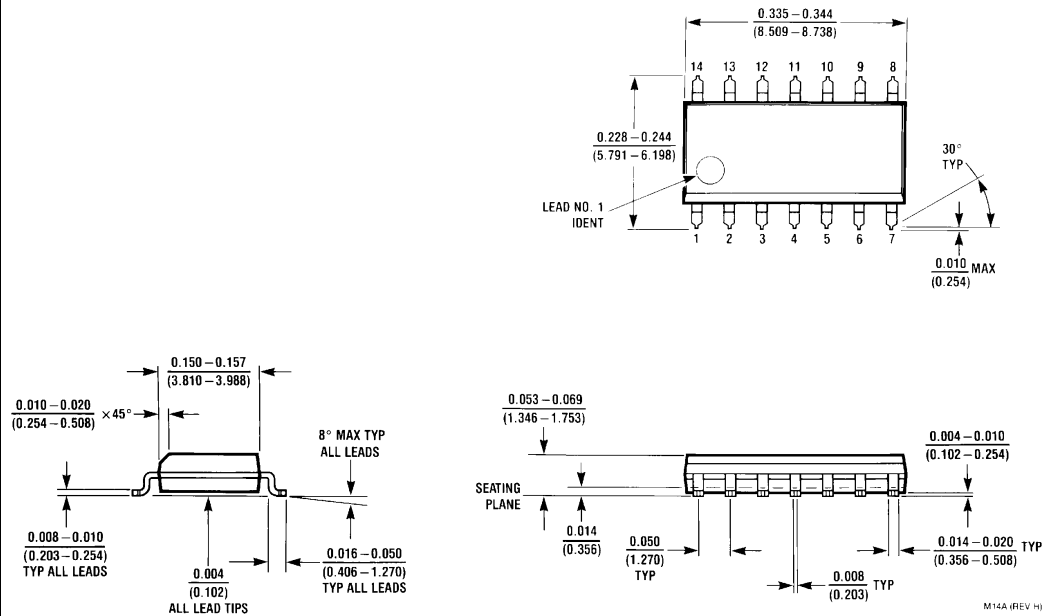
Note 6: Parameter guaranteed by design.

AC Electrical Characteristics

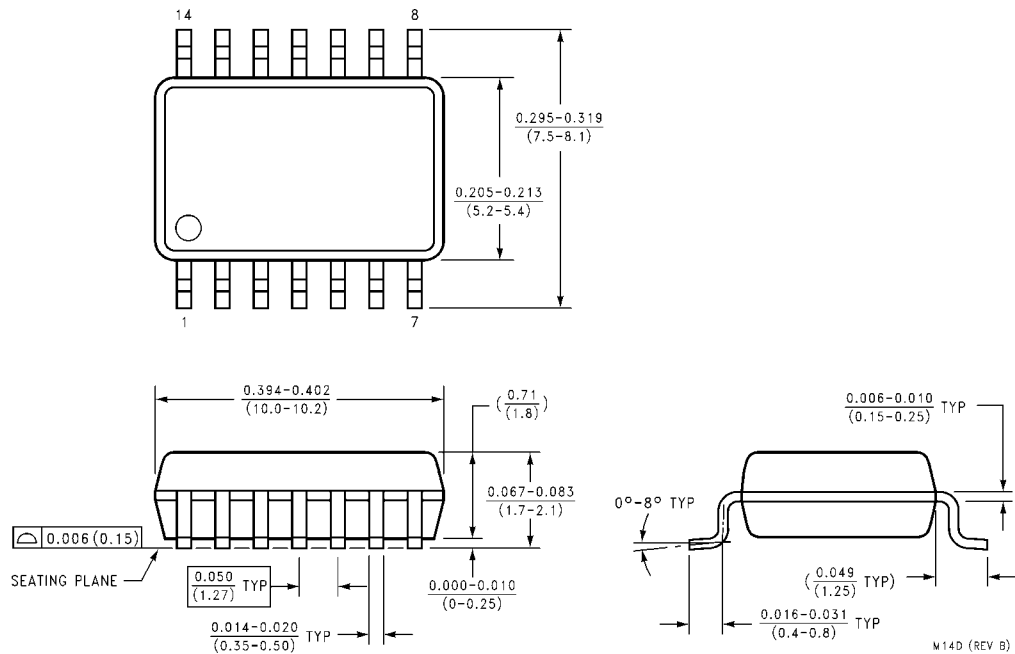
| Symbol | Parameter | V _{CC} (V) | T _A = 25°C | | | T _A = -40°C to +85°C | | Units | Conditions |
|------------------|-------------------------------|------------------------|-----------------------|-----|-----|---------------------------------|------|-------|------------------------|
| | | | Min | Typ | Max | Min | Max | | |
| t _{PHL} | Propagation Delay | 5.0 ± 0.5 | | 5.0 | 7.6 | 1.0 | 9.0 | ns | C _L = 15 pF |
| t _{PLH} | | | | 6.5 | 9.6 | 1.0 | 11.0 | ns | C _L = 50 pF |
| C _{IN} | Input Capacitance | | | 2 | 10 | | 10 | pF | V _{CC} = OPEN |
| C _{PD} | Power Dissipation Capacitance | | | 11 | | | | pF | (Note 7) |

Note 7: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}/6 (per gate).

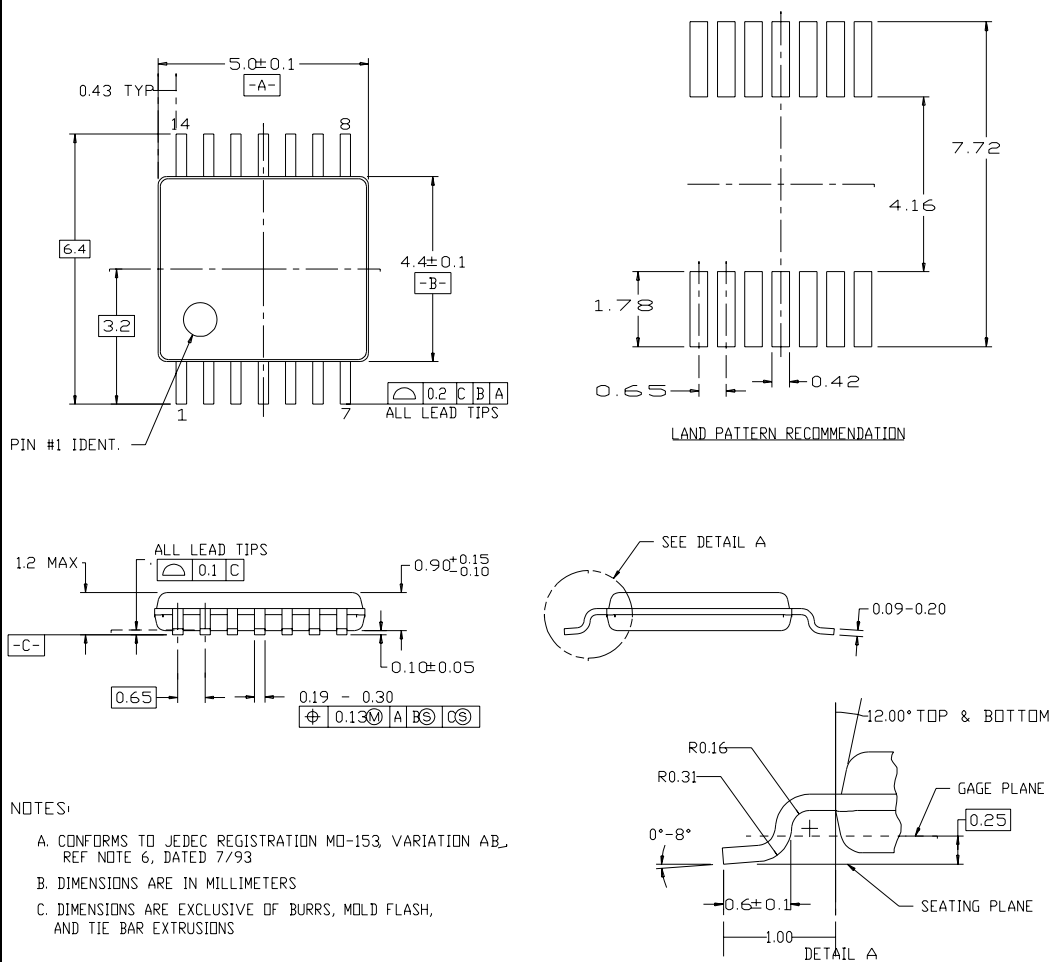
Physical Dimensions inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
Package Number M14A**

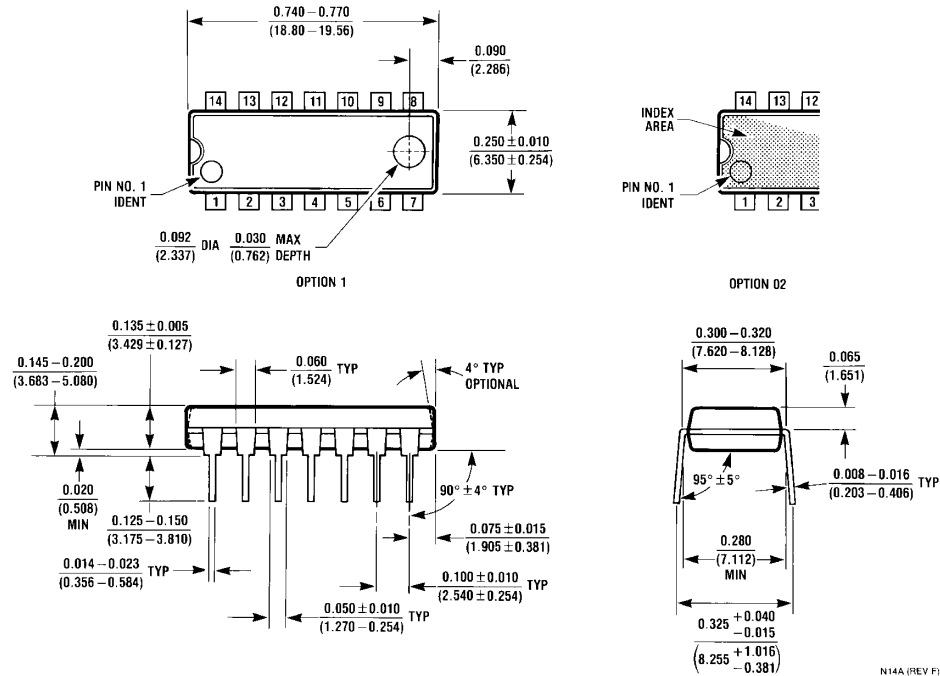


**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)


**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N14A (REV F)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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