

CD40106BC Hex Schmitt Trigger

General Description

The CD40106BC Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The positive and negative-going threshold voltages, V_{T+} and V_{T-} , show low variation with respect to temperature (typ 0.0005V/°C at $V_{DD} = 10V$), and hysteresis, $V_{T+} - V_{T-} \geq 0.2 V_{DD}$ is guaranteed.

All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS} .

Features

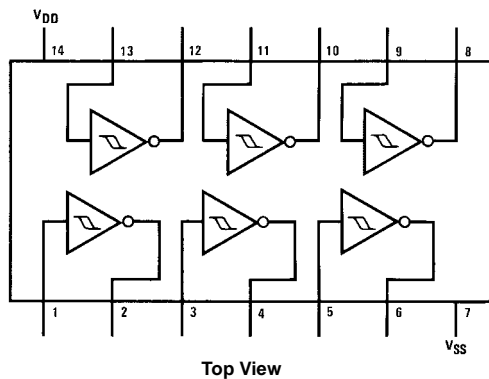
- Wide supply voltage range: 3V to 15V
- High noise immunity: $0.7 V_{DD}$ (typ.)
- Low power TTL compatibility:
Fan out of 2 driving 74L or 1 driving 74LS
- Hysteresis: $0.4 V_{DD}$ (typ.),
 $0.2 V_{DD}$ guaranteed
- Equivalent to MM74C14
- Equivalent to MC14584B

Ordering Code:

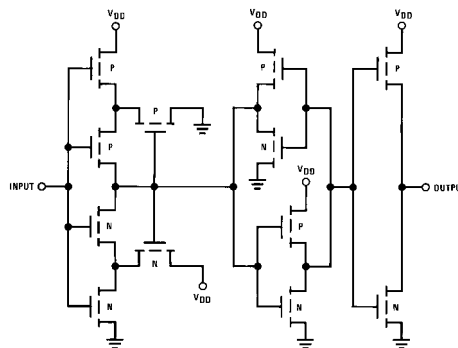
| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| CD40106BCM | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| CD40106BCN | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Schematic Diagram



Absolute Maximum Ratings(Note 1)

(Note 2)

| | |
|-------------------------------------|--------------------------------|
| DC Supply Voltage (V_{DD}) | -0.5 to +18 V_{DC} |
| Input Voltage (V_{IN}) | -0.5 to V_{DD} +0.5 V_{DC} |
| Storage Temperature Range (T_S) | -65°C to +150°C |
| Power Dissipation (P_D) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Lead Temperature (T_L) | |
| (Soldering, 10 seconds) | 260°C |

Recommended Operating Conditions (Note 2)

| | |
|---------------------------------------|------------------------|
| DC Supply Voltage (V_{DD}) | 3 to 15 V_{DC} |
| Input Voltage (V_{IN}) | 0 to V_{DD} V_{DC} |
| Operating Temperature Range (T_A) | -55°C to +125°C |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

DC Electrical Characteristics (Note 3)

| Symbol | Parameter | Conditions | -55°C | | +25°C | | | +125°C | | Units |
|----------|--|--|-----------------------|----------------------|-----------------------|-------------------------|----------------------|-----------------------|----------------------|---------|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| I_{DD} | Quiescent Device Current | $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$ | | 1.0 2.0 4.0 | | | 1.0 2.0 4.0 | | 30 60 120 | μA |
| V_{OL} | LOW Level Output Voltage | $ I_O < 1 \mu A$ $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$ | | 0.05 0.05 0.05 | | | 0.05 0.05 0.05 | | 0.05 0.05 0.05 | V |
| V_{OH} | HIGH Level Output Voltage | $ I_O < 1 \mu A$ $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$ | 4.95 9.95 14.95 | | 4.95 9.95 14.95 | 5 10 15 | | 4.95 0.95 14.95 | | V |
| V_{T-} | Negative-Going Threshold Voltage | $V_{DD} = 5V, V_O = 4.5V$ $V_{DD} = 10V, V_O = 9V$ $V_{DD} = 15V, V_O = 13.5V$ | 0.7 1.4 2.1 | 2.0 4.0 6.0 | 0.7 1.4 2.1 | 1.4 3.2 5.0 | 2.0 4.0 6.0 | 0.7 1.4 2.1 | 2.0 4.0 6.0 | V |
| V_{T+} | Positive-Going Threshold Voltage | $V_{DD} = 5V, V_O = 0.5V$ $V_{DD} = 10V, V_O = 1V$ $V_{DD} = 15V, V_O = 1.5V$ | 3.0 6.0 9.0 | 4.3 8.6 12.9 | 3.0 6.0 9.0 | 3.6 6.8 10.0 | 4.3 8.6 12.9 | 3.0 6.0 9.0 | 4.3 8.6 12.9 | V |
| V_H | Hysteresis ($V_{T+} - V_{T-}$) Voltage | $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$ | 1.0 2.0 3.0 | 3.6 7.2 10.8 | 1.0 2.0 3.0 | 2.2 3.6 5.0 | 3.6 7.2 10.8 | 1.0 2.0 3.0 | 3.6 7.2 10.8 | V |
| I_{OL} | LOW Level Output Current (Note 3) | $V_{DD} = 5V, V_O = 0.4V$ $V_{DD} = 10V, V_O = 0.5V$ $V_{DD} = 15V, V_O = 1.5V$ | 0.64 1.6 4.2 | | 0.51 1.3 3.4 | 0.88 2.25 8.8 | | 0.36 0.9 2.4 | | mA |
| I_{OH} | HIGH Level Output Current (Note 3) | $V_{DD} = 5V, V_O = 4.6V$ $V_{DD} = 10V, V_O = 9.5V$ $V_{DD} = 15V, V_O = 13.5V$ | -0.64 -1.6 -4.2 | | -0.51 -1.3 -3.4 | -0.88 -2.25 -8.8 | | -0.36 -0.9 -2.4 | | mA |
| I_{IN} | Input Current | $V_{DD} = 15V, V_{IN} = 0V$ $V_{DD} = 15V, V_{IN} = 15V$ | | -0.1 0.1 | | -10^{-5} 10^{-5} | -0.1 0.1 | | -1.0 1.0 | μA |

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 4)

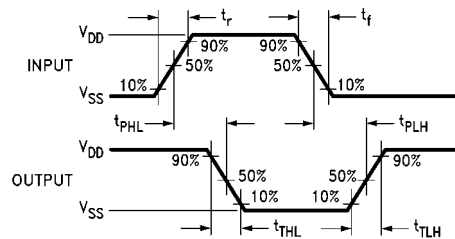
$T_A = 25^{\circ}\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$, t_r and $t_f = 20\text{ ns}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------------------|---|--|-----|-----------------|-------------------|-------|
| t_{PHL} or t_{PLH} | Propagation Delay Time from Input to Output | $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$ | | 220 80 70 | 400 200 160 | ns |
| t_{THL} or t_{TLH} | Transition Time | $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$ | | 100 50 40 | 200 100 80 | ns |
| C_{IN} | Average Input Capacitance | Any Input | | 5 | 7.5 | pF |
| C_{PD} | Power Dissipation Capacity | Any Gate (Note 5) | | 14 | | pF |

Note 4: AC Parameters are guaranteed by DC correlated testing.

Note 5: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 74C Family Characteristics Application Note, AN-90.

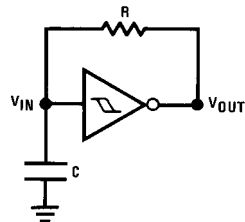
Switching Time Waveforms



$t_r = t_f = 20\text{ ns}$

Typical Applications

Low Power Oscillator



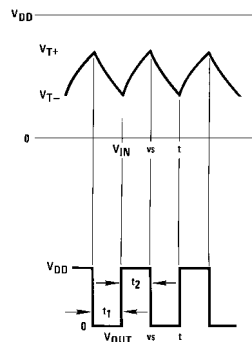
$$t_1 \approx RC \ln \frac{V_{T+}}{V_{T-}}$$

$$t_2 \approx RC \ln \frac{V_{DD} - V_{T-}}{V_{DD} - V_{T+}}$$

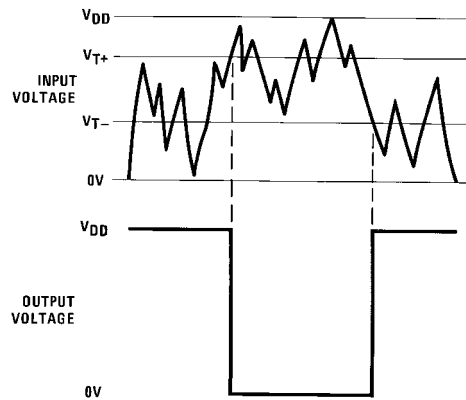
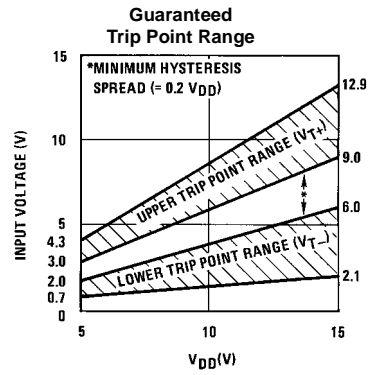
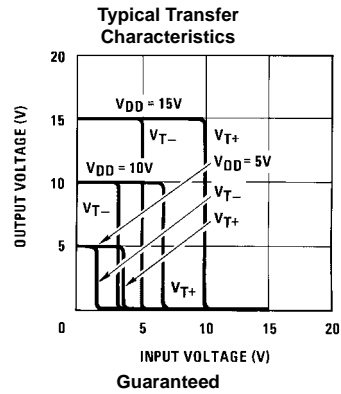
$$f \approx \frac{1}{RC \ln \frac{V_{T+} (V_{DD} - V_{T-})}{V_{T-} (V_{DD} - V_{T+})}}$$

Note: The equations assume

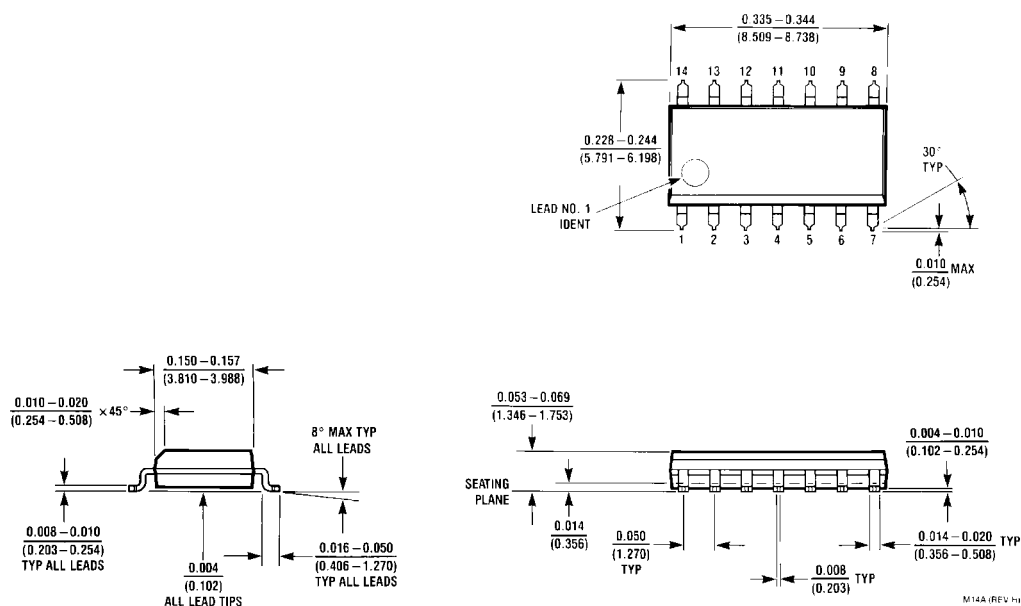
$$t_1 + t_2 \gg t_{PHL} + t_{PLH}$$



Typical Performance Characteristics

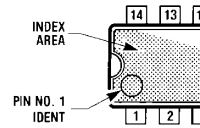
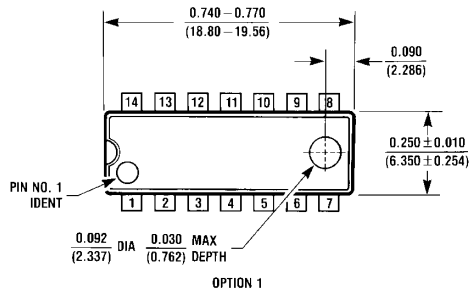


Physical Dimensions inches (millimeters) unless otherwise noted

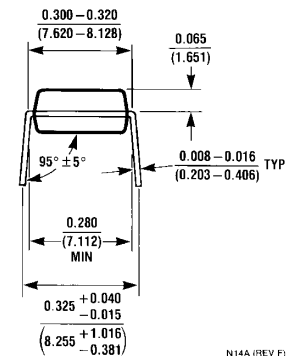
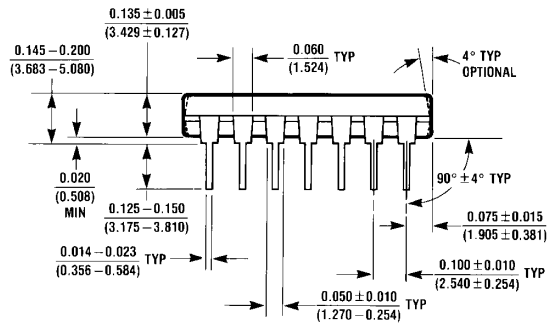


14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



OPTION 02



N14A (REV F)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com