

## GTLP2T152 2-Bit LVTTTL/GTLP Transceiver

### General Description

The GTLP2T152 is a 2-bit transceiver that provides LVTTTL-to-GTLP signal level translation. Data directional control is handled with a transmit/receive pin. High-speed backplane operation is a direct result of GTLP's reduced output swing (<1V), reduced input threshold levels and output edge rate control. The edge rate control minimizes bus-settling time. GTLP is a Fairchild Semiconductor derivative of the Gunning Transistor logic (GTL) JEDEC standard JESD8-3.

Fairchild's GTLP has internal edge-rate control and is process, voltage and temperature compensated. GTLP's I/O structure is similar to GTL and BTL but offers different output levels and receiver threshold. Typical GTLP output voltage levels are:  $V_{OL} = 0.5V$ ,  $V_{OH} = 1.5V$ , and  $V_{REF} = 1V$ .

### Features

- Bidirectional interface between GTLP and LVTTTL logic levels
- Designed with edge rate control circuitry to reduce output noise on the GTLP port
- $V_{REF}$  pin provides external supply reference voltage for receiver threshold adjustability
- Special PVT compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- TTL compatible driver and control inputs
- Designed using Fairchild advanced BiCMOS technology
- Bushold data inputs on A port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down and power off high impedance for live insertion
- Open drain on GTLP to support wired-or connection
- Flow through pinout optimizes PCB layout
- A Port source/sink -24mA/+24mA
- B Port sink +50mA

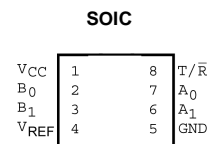
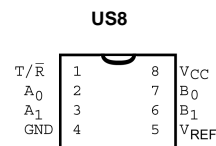
### Ordering Code:

Order Number	Package Number	Package Description
GTLP2T152M	M08A	8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow [TUBE]
GTLP2T152MX	M08A	8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow [TAPE and REEL]
GTLP2T152K8X	MAB08A (Preliminary)	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide [TAPE and REEL]

### Pin Descriptions

Pin Names	Description
$T/\bar{R}$	LVTTTL Direction Control (Receive Direction is Active LOW)
$V_{CC}$ , GND, $V_{REF}$	Device Supplies
$A_n$	A Port LVTTTL Input/Output
$B_n$	B Port GTLP Input/Output

### Connection Diagrams



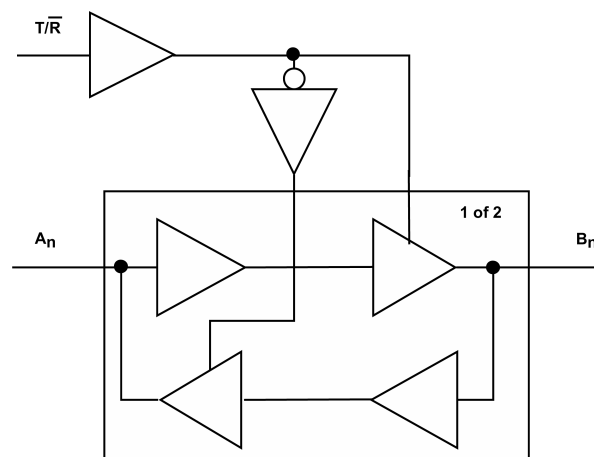
## Functional Description

The GTLP2T152 is a 2-bit transceiver that supports GTLP and LVTTTL signal levels. Data polarity is non-inverting and the the GTLP/LVTTTL outputs are controlled by the  $\overline{T/R}$  pin.

## Functional Table

Inputs	Outputs	Description
$\overline{T/R}$		
H	Bus $A_n$ Data to Bus $B_n$	$B_n$ Output Data Enabled
L	Bus $B_n$ Data to Bus $A_n$	$A_n$ Output Data Enabled

## Logic Diagram



# Absolute Maximum Ratings<sup>(Note 1)</sup>

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V
DC Input Voltage ( $V_I$ )	-0.5V to +4.6V
DC Output Voltage ( $V_O$ )	
Outputs 3-STATE	-0.5V to +4.6V
Outputs Active (Note 2)	-0.5V to +4.6V
DC Output Sink Current into	
A Port $I_{OL}$	48 mA
DC Output Source Current from	
A Port $I_{OH}$	-48 mA
DC Output Sink Current into	
B Port in the LOW State, $I_{OL}$	100 mA
DC Input Diode Current ( $I_{IK}$ )	
$V_I < 0V$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0V$	-50 mA
ESD Rating	>2000V
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C

# Recommended Operating Conditions

Supply Voltage $V_{CC}$	3.15V to 3.45V
Bus Termination Voltage ( $V_{TT}$ )	
GTLP	1.47V to 1.53V
$V_{REF}$	0.98V to 1.02V
Input Voltage ( $V_I$ )	
on A Port and Control Pins	0.0V to $V_{CC}$
HIGH Level Output Current ( $I_{OH}$ )	
A Port	-24 mA
LOW Level Output Current ( $I_{OL}$ )	
A Port	+24 mA
B Port	+50 mA
Operating Temperature ( $T_A$ )	-40°C to +85°C

**Note 1:** Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:**  $I_O$  Absolute Maximum Rating must be observed.

# DC Electrical Characteristics

Over Recommended Operating Free-Air Temperature Range,  $V_{REF} = 1.0V$  (unless otherwise noted).

Symbol		Test Conditions		Min	Typ (Note 3)	Max	Units
$V_{IH}$	B Port			$V_{REF} + 0.05$		$V_{TT}$	V
	Others			2.0			
$V_{IL}$	B Port			0.0		$V_{REF} - 0.05$	V
	Others					0.8	
$V_{REF}$	B Port			0.7V	1.0	1.3V	V
$V_{TT}$	B Port			$V_{REF} + 50\text{ mV}$	1.5	$V_{CC}$	V
$V_{IK}$		$V_{CC} = 3.15V$	$I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$	A Port	$V_{CC} = \text{Min to Max (Note 4)}$	$I_{OH} = -100\text{ }\mu A$	$V_{CC} - 0.2$			V
		$V_{CC} = 3.15V$	$I_{OH} = -8\text{ mA}$	2.4			
			$I_{OH} = -24\text{ mA}$	2.2			
$V_{OL}$	A Port	$V_{CC} = \text{Min to Max (Note 4)}$	$I_{OL} = 100\text{ }\mu A$			0.2	V
		$V_{CC} = 3.15V$	$I_{OL} = 8\text{ mA}$			0.4	
		$V_{CC} = 3.15V$	$I_{OL} = 24\text{ mA}$			0.5	
	B Port	$V_{CC} = 3.15V$	$I_{OL} = 40\text{ mA}$			0.4	V
			$I_{OL} = 50\text{ mA}$			0.55	
$I_I$	Control Pins	$V_{CC} = 3.45V$	$V_I = 3.45V$ $V_I = 0V$			5 -5	$\mu A$
	A Port	$V_{CC} = 3.45V$	$V_I = 3.45V$ $V_I = 0V$			10 -10	
	B Port	$V_{CC} = 3.45V$	$V_I = 3.45V$ $V_I = 0$			5 -5	
$I_{OFF}$	A Port, Control Pins	$V_{CC} = 0$	$V_I$ or $V_O = 0$ to 3.45V			30	$\mu A$
	B Port	$V_{CC} = 0$	$V_I$ or $V_O = 0$ to 3.45V			30	
$I_I(\text{HOLD})$	A Port	$V_{CC} = 3.15V$	$V_I = 0.8V$ $V_I = 2.0V$	75		-75	$\mu A$
$I_{OZH}$	A Port	$V_{CC} = 3.45V$	$V_O = 3.45V$			10	$\mu A$
	B Port		$V_O = 3.45V$			5	

## DC Electrical Characteristics (Continued)

Symbol	Test Conditions	Min	Typ (Note 3)	Max	Units
$I_{OZL}$	A Port	$V_{CC} = 3.45V$	$V_O = 0V$	-10	$\mu A$
	B Port				
$I_{PU/PD}$	All Ports	$V_{CC} = 0$ to $1.5V$	$V_I = 0$ to $3.45V$	30	$\mu A$
$I_{CC}$	A Port or B Port	$V_{CC} = 3.45V$ $I_O = 0$ $V_I = V_{CC}/V_{TT}$ or GND	Outputs HIGH	11	mA
			Outputs LOW	11	
			Outputs Disabled	11	
$\Delta I_{CC}$ (Note 5)	A Port and Control Pins	$V_{CC} = 3.45V$ , A or Control Inputs at $V_{CC}$ or GND	One Input at $V_{CC}$ -0.6V	2	mA
$C_i$	Control Pins		$V_I = V_{CC}$ or 0	3	pF
$C_{I/O}$	A Port		$V_I = V_{CC}$ or 0	5	pF
	B Port		$V_I = V_{TT}$ or 0	5.5	pF

**Note 3:** All typical values are at  $V_{CC} = 3.3V$  and  $T_A = 25^\circ C$ .

**Note 4:** For conditions shown as Min, use the appropriate value specified under recommended operating conditions.

**Note 5:** This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

**Note:** GTLP  $V_{REF}$  and  $V_{TT}$  are specified to 2% tolerance since signal integrity and noise margin can be significantly degraded if these supplies are noisy. In addition,  $V_{TT}$  and  $R_{TERM}$  can be adjusted beyond the recommended operating to accommodate backplane impedances other than  $50\Omega$ , but must remain within the boundaries of the DC Absolute Maximum Ratings. Similarly,  $V_{REF}$  can be adjusted to optimize noise margin.

## AC Electrical Characteristics

Over recommended range of supply voltage and operating free-air temperature,  $V_{REF} = 1.0V$  (unless otherwise noted).

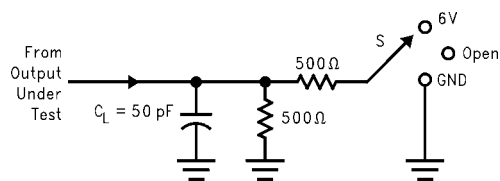
$C_L = 30$  pF for B Port and  $C_L = 50$  pF for A Port.

Symbol	From (Input)	To (Output)	Min	Typ (Note 6)	Max	Unit
t <sub>PLH</sub>	A	B	1.2	2.9	7.3	ns
t <sub>PHL</sub>			0.8	2.0	4.5	
t <sub>PLH</sub>	B	A	1.4	2.5	4.4	ns
t <sub>PHL</sub>			1.6	2.7	5.0	
t <sub>RISE</sub>	Transition Time, B Outputs (20% to 80%)			1.5		ns
t <sub>FALL</sub>	Transition Time, B Outputs (80% to 20%)			1.8		ns
t <sub>RISE</sub>	Transition Time, A Outputs (10% to 90%)			2.5		ns
t <sub>FALL</sub>	Transition Time, A Outputs (90% to 10%)			2.2		ns

**Note 6:** All typical values are at  $V_{CC} = 3.3V$ , and  $T_A = 25^\circ C$ .

# Test Circuits and Timing Waveforms

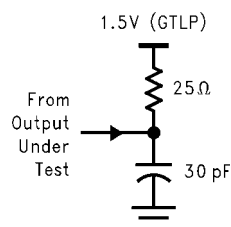
Test Circuit for A Outputs



Test	S
$t_{PLH}/t_{PHL}$	OPEN
$t_{PLZ}/t_{PZL}$	6V
$t_{PHZ}/t_{PZH}$	GND

Note:  $C_L$  includes probes and Jig capacitance.

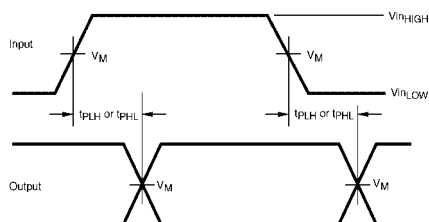
Test Circuit for B Outputs



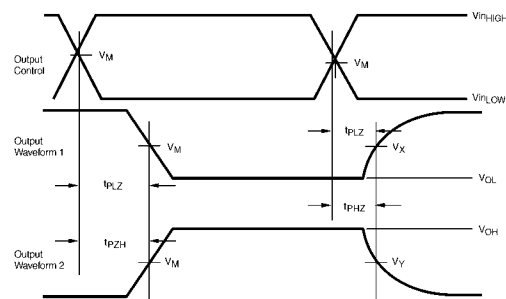
Note:  $C_L$  includes probes and Jig capacitance.

Note: For B Port,  $C_L = 30\text{ pF}$  is used for worst case.

Voltage Waveforms Propagation Delay



Voltage Waveform Enable and Disable Times



	A or LVTTTL Pins	B or GTLP Pins
$V_{IN\_HIGH}$	$V_{CC}$	1.5
$V_{IN\_LOW}$	0.0	0.0
$V_M$	$V_{CC}/2$	1.0
$V_X$	$V_{OL} + 0.3V$	N/A
$V_Y$	$V_{OH} - 0.3V$	N/A

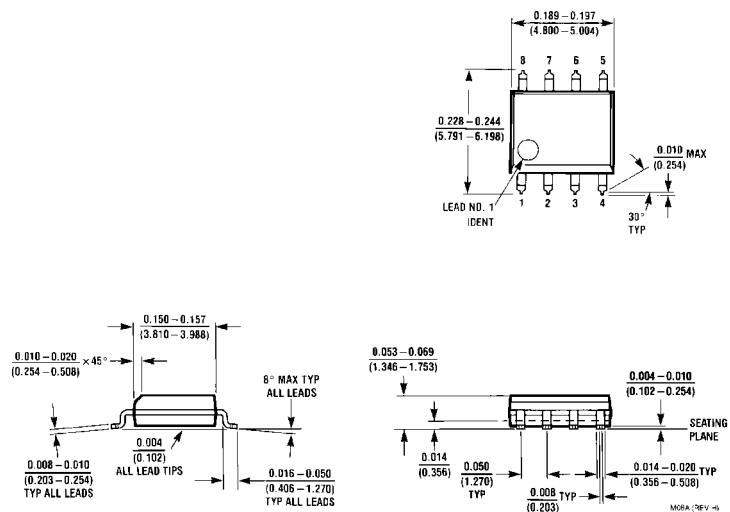
Note: Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

Note: All input pulses have the following characteristics:

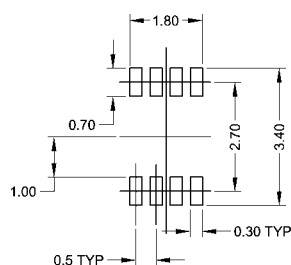
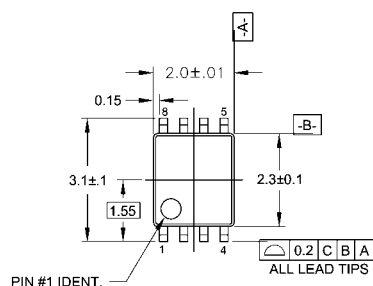
Frequency = 10MHz,  $t_{RISE} = t_{FALL} = 2\text{ ns}$  (10% to 90%),  $Z_O = 50\Omega$ . The outputs are measured one at a time with one transition per measurement.

# Physical Dimensions inches (millimeters) unless otherwise noted

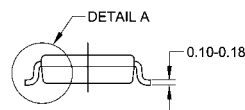
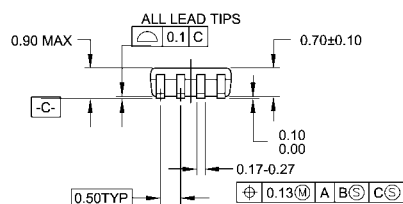


8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M08A

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

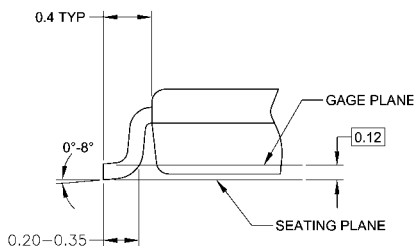


## LAND PATTERN RECOMMENDATION



## NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-187
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.



## DETAIL A

MAB08AREVC

8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide  
Package Number MAB08A  
Preliminary

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