

## FEATURES

- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 10  $\mu$ A (Max.) @  $V_{DS} = 200V$
- Lower  $R_{DS(ON)}$  : 1.185  $\Omega$  (Typ.)

$$BV_{DSS} = 200 V$$

$$R_{DS(on)} = 1.5 \Omega$$

$$I_D = 0.77 A$$

## SOT-223



1. Gate 2. Drain 3. Source

## Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
$V_{DSS}$	Drain-to-Source Voltage	200	V
$I_D$	Continuous Drain Current ( $T_A=25^\circ C$ )	0.77	A
	Continuous Drain Current ( $T_A=70^\circ C$ )	0.62	
$I_{DM}$	Drain Current-Pulsed ①	6.1	A
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulsed Avalanche Energy ②	27	mJ
$I_{AR}$	Avalanche Current ①	0.77	A
$E_{AR}$	Repetitive Avalanche Energy ①	0.18	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
$P_D$	Total Power Dissipation ( $T_A=25^\circ C$ ) *	1.8	W
	Linear Derating Factor *	0.014	W/ $^\circ C$
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
$T_L$	Maximum Lead Temp. for Soldering Purposes, 1/8 " from case for 5-seconds	300	

## Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient *	--	69.4	$^\circ C/W$

\* When mounted on the minimum pad size recommended (PCB Mount).

**Electrical Characteristics** ( $T_C=25^{\circ}\text{C}$  unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$BV_{DSS}$	Drain-Source Breakdown Voltage	200	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.19	--	$V/^{\circ}\text{C}$	$I_D=250\mu A$ <b>See Fig 7</b>
$V_{GS(th)}$	Gate Threshold Voltage	1.0	--	2.0	V	$V_{DS}=5V, I_D=250\mu A$
$I_{GSS}$	Gate-Source Leakage , Forward	--	--	100	nA	$V_{GS}=20V$
	Gate-Source Leakage , Reverse	--	--	-100		$V_{GS}=-20V$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	10	$\mu A$	$V_{DS}=200V$
		--	--	100		$V_{DS}=160V, T_C=125^{\circ}\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	1.5	$\Omega$	$V_{GS}=5V, I_D=0.39A$ ④
$g_{fs}$	Forward Transconductance	--	1.8	--	$\text{S}$	$V_{DS}=40V, I_D=0.39A$ ④
$C_{iss}$	Input Capacitance	--	185	240	pF	$V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$ <b>See Fig 5</b>
$C_{oss}$	Output Capacitance	--	35	45		
$C_{rss}$	Reverse Transfer Capacitance	--	14	20		
$t_{d(on)}$	Turn-On Delay Time	--	9	30	ns	$V_{DD}=100V, I_D=3.3A,$ $R_G=22\Omega$ <b>See Fig 13</b> ④ ⑤
$t_r$	Rise Time	--	9	30		
$t_{d(off)}$	Turn-Off Delay Time	--	20	50		
$t_f$	Fall Time	--	6	20		
$Q_g$	Total Gate Charge	--	6.1	9	nC	$V_{DS}=160V, V_{GS}=5V,$ $I_D=3.3A$ <b>See Fig 6 &amp; Fig 12</b> ④ ⑤
$Q_{gs}$	Gate-Source Charge	--	1.4	--		
$Q_{gd}$	Gate-Drain( " Miller " ) Charge	--	2.8	--		

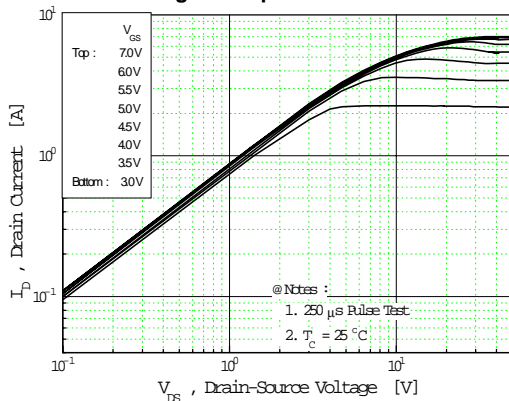
**Source-Drain Diode Ratings and Characteristics**

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$I_S$	Continuous Source Current	--	--	0.77	A	Integral reverse pn-diode in the MOSFET
$I_{SM}$	Pulsed-Source Current ①	--	--	6.1		
$V_{SD}$	Diode Forward Voltage ④	--	--	1.5	V	$T_J=25^{\circ}\text{C}, I_S=0.77A, V_{GS}=0V$
$t_{rr}$	Reverse Recovery Time	--	123	--	ns	$T_J=25^{\circ}\text{C}, I_F=3.3A$
$Q_{rr}$	Reverse Recovery Charge	--	0.38	--	$\mu C$	$di_F/dt=100A/\mu s$ ④

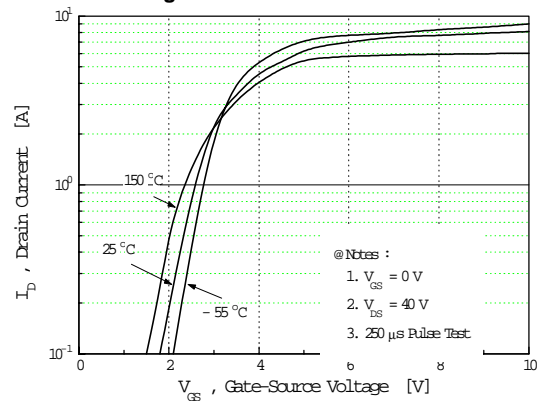
**Notes ;**

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ②  $L=70\text{mH}, I_{AS}=0.77A, V_{DD}=50V, R_G=27\Omega$ , Starting  $T_J=25^{\circ}\text{C}$
- ③  $I_{SD}\leq 3.3A, di/dt\leq 140A/\mu s, V_{DD}\leq BV_{DSS}$ , Starting  $T_J=25^{\circ}\text{C}$
- ④ Pulse Test : Pulse Width =  $250\mu s$ , Duty Cycle  $\leq 2\%$
- ⑤ Essentially Independent of Operating Temperature

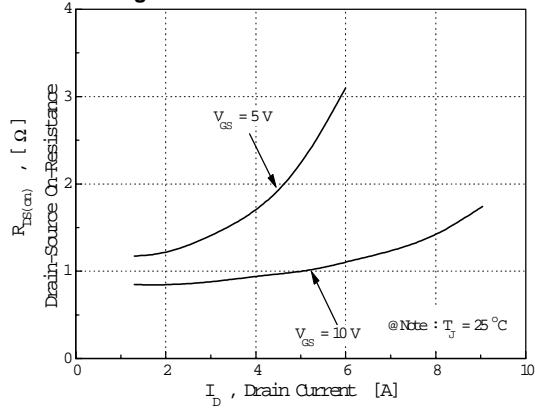
**Fig 1. Output Characteristics**



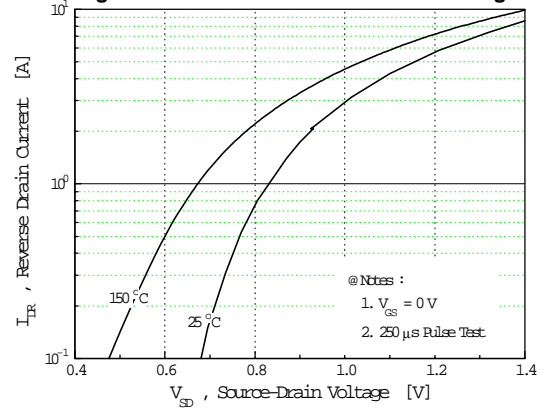
**Fig 2. Transfer Characteristics**



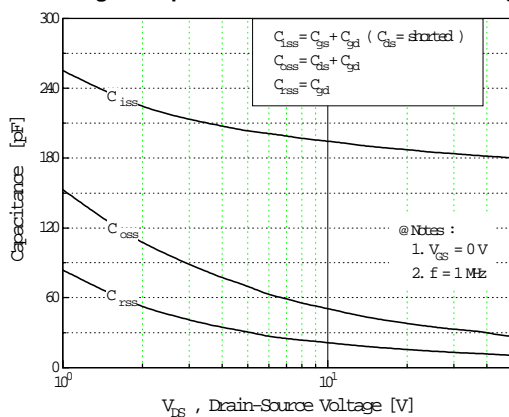
**Fig 3. On-Resistance vs. Drain Current**



**Fig 4. Source-Drain Diode Forward Voltage**



**Fig 5. Capacitance vs. Drain-Source Voltage**



**Fig 6. Gate Charge vs. Gate-Source Voltage**

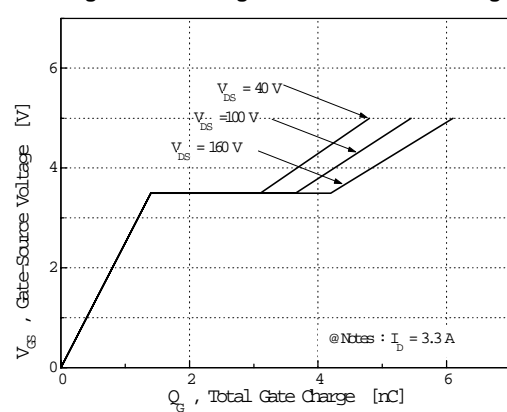


Fig 7. Breakdown Voltage vs. Temperature

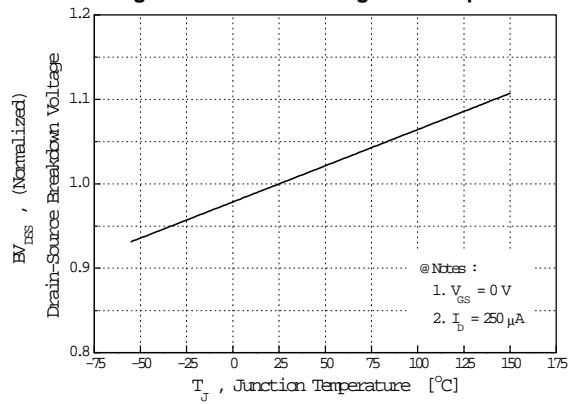


Fig 8. On-Resistance vs. Temperature

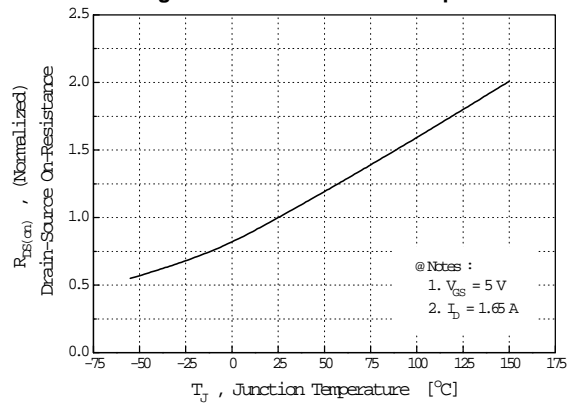


Fig 9. Max. Safe Operating Area

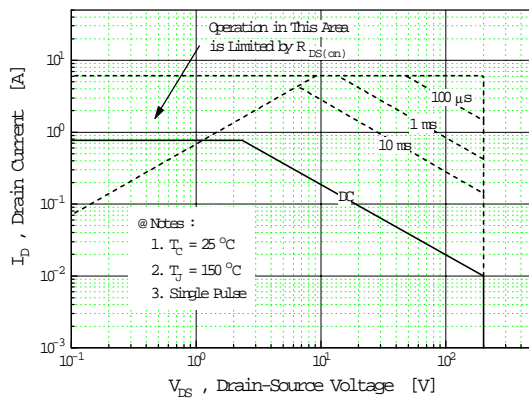


Fig 10. Max. Drain Current vs. Ambient Temperature

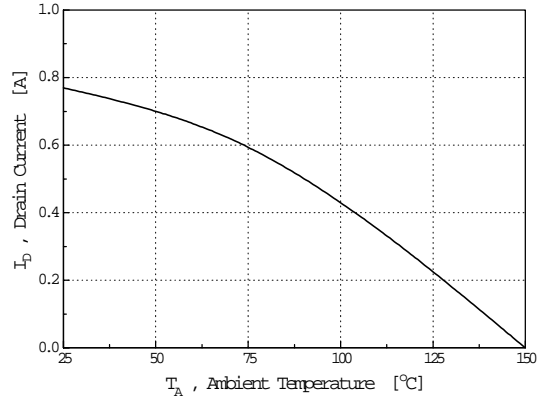
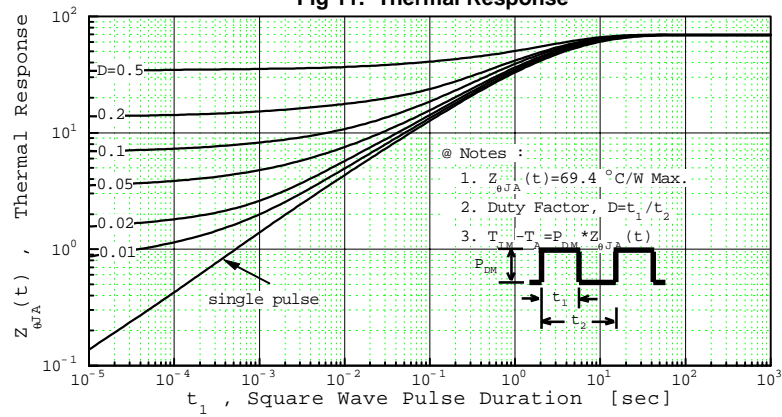
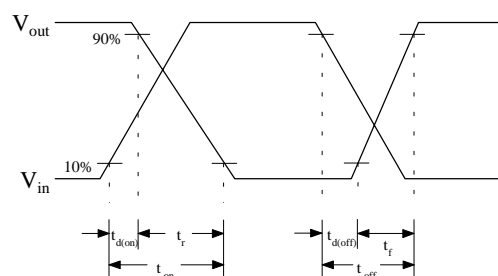
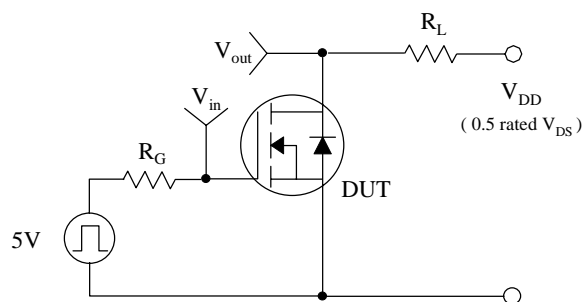


Fig 11. Thermal Response



The diagram illustrates a current source circuit for a DUT. A 12V source is connected to a 200nF capacitor and a 50KΩ resistor. The resistor is connected to a MOSFET (labeled "Current Regulator") which is also connected to a 300nF capacitor. The MOSFET's gate is connected to a 3mA current source. The MOSFET's drain is connected to the DUT (labeled "DUT") which is also connected to a 300nF capacitor. The DUT's gate is connected to a 3mA current source. The DUT's drain is connected to a resistor  $R_1$ , which is connected to a current sampling resistor ( $I_G$ ). The DUT's source is connected to a resistor  $R_2$ , which is connected to a current sampling resistor ( $I_D$ ). The DUT's gate is also connected to a 3mA current source.



Vary  $t_p$  to obtain required peak  $I_D$

$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 - \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

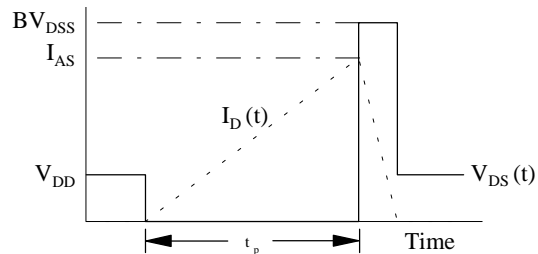
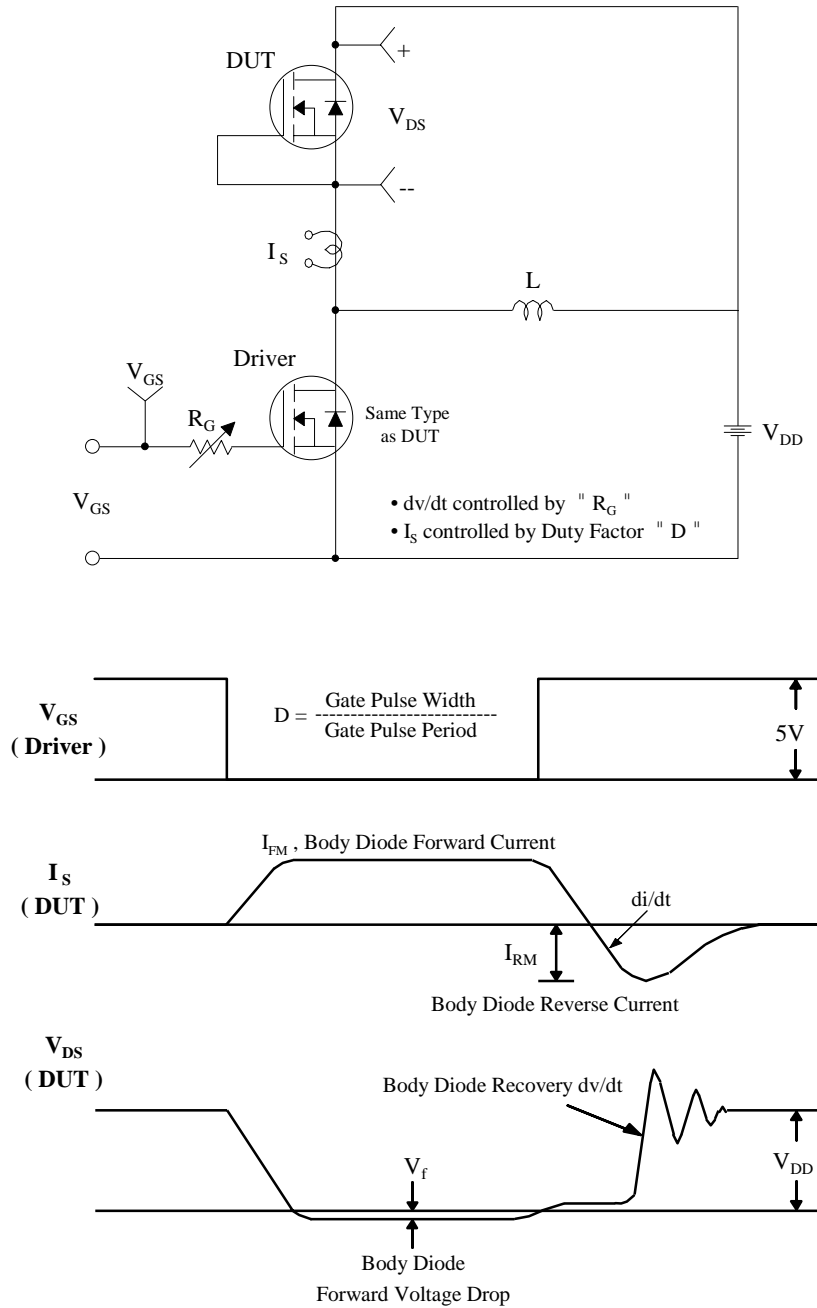


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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