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1.1	2002/02/19	2002/3/4	P.14	Change the Gamma correction graph.

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EK7402

DATA SHEET

384-Channel 6-bit Source Driver for color TFT LCDs



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384-Channel 6-bit Source Driver for color TFT LCDs

DESCRIPTION

The EK7402A, EK7402B are 6-bit source driver ICs dedicated for XGA and SXGA TFT-LCD panels. The digital input is a 6-bit word by 6 dots digital display data, where each word can generate 64-grayscale levels. By using R/G/B filters 3 dots can be combined to generate a 260'000 colors pixel. Each output can drive alternately 64 positive-polarity or 64 negative-polarity grayscale levels with respect to the opposite polarity of adjacent odd and even output pins. These 64 positive and negative grayscale levels are generated with 2x5 external reference voltages (V0-V4, V5-V9) feeding a built-in RDAC that implements a gamma correction for the panel. With positive and negative output voltage, these circuits feature a dot-dot inversion, n-lines-dot inversion and frame-dot inversion schemes.

FEATURES

- CMOS input level (2.3V to 3.6V)
- High-speed data transfer: $F_{MAX} = 65$ MHz (internal data transfer speed when operating at $V_{DD1} = 3.0V$)
- 36 data bits (6-bit grayscales code x 3 RGB dot x 2 pixels)
- Logic power supply voltage (V_{DD1}): 2.3V to 3.6V
- Driver power supply voltage (V_{DD2}): 7V to 12V
- Output dynamic range: $V_{SS2} + 0.1V$ to $V_{DD2} - 0.1V$
- 384 outputs
- 64 positive and negative output voltage levels by means of 2x5 external reference voltages and a built in D/A converter (R-DAC)
- Applies for dot-dot inversion, n-line-dot inversion and frame-dot inversion
- Output voltage polarity inversion function (POL)
- Bi-directional shift (R/L)
- Chip-enable signal generation circuit
- Display data inversion function (POL1, POL2)
- Low power control function (LPC)
- Difference point between EK7402A and EK7402B: Gamma correction (Refer to point 11)

1. INTERNAL BLOCK DIAGRAM

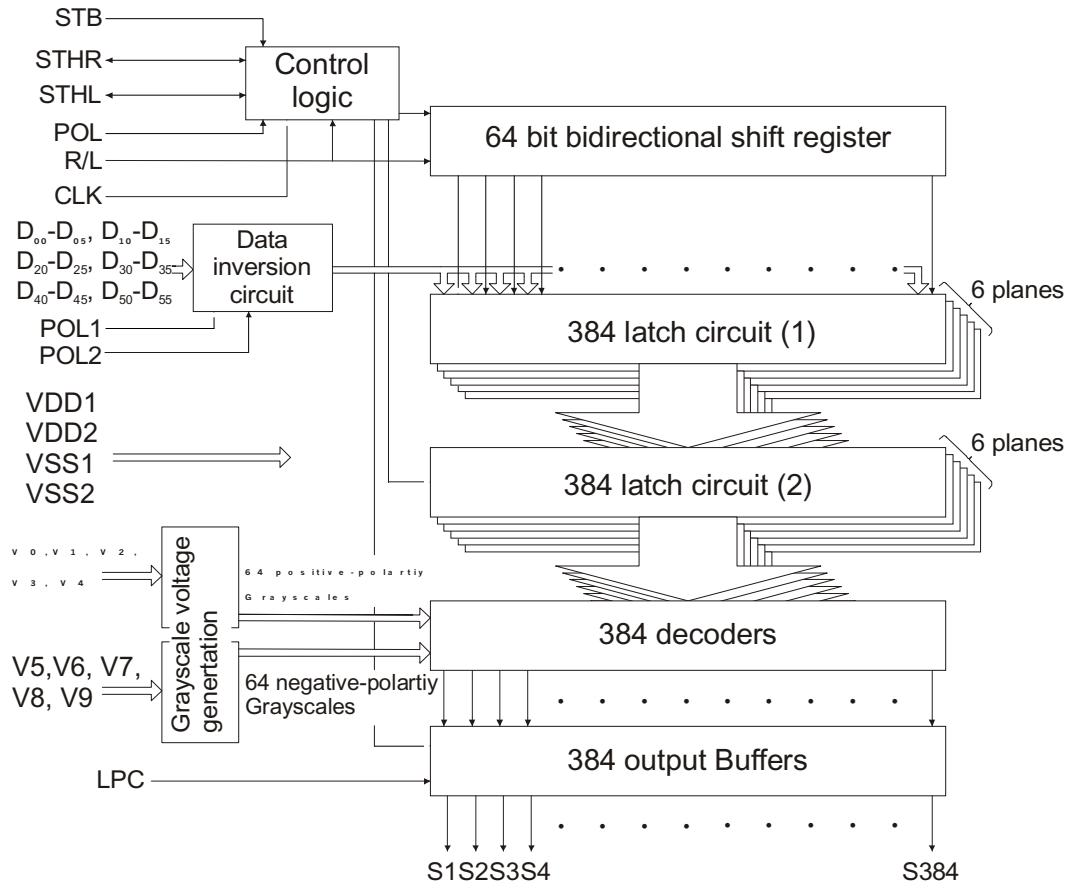


Figure 1: Block diagram

1. **Control logic unit**
Generates the chip-enable signal STHR and STHL and the internal control signals.
2. **Data inversion unit**
Uses the POL1-POL2 signals to invert or not the 6 x 6-bit input data.
3. **64 bits bi-directional shift register**
Generates the enable signals for sequential latching of 64 groups of 36-bit input data.
4. **Latch circuit (1)**
384x6-bit latch circuits that latch sequentially 6 outputs x 6-bit (2 pixels) from the data bus.
5. **Latch circuit (2)**
Stores on the rising edge of STB signal the 384x6-bit line data from the first latch stage to the output buffers.
6. **Decoders**
Select one of the 64-grayscale levels as a function of the 6-bit code word.
7. **Grayscale voltage generation unit**
Performs a voltage division of the 10 external input reference voltages, and generates 64 positive-polarity and 64 negative-polarity grayscale levels.
8. **Buffers**
Drive the selected grayscale voltage level to the panel.

2. PIN CONFIGURATION (TCP I PACKAGE)

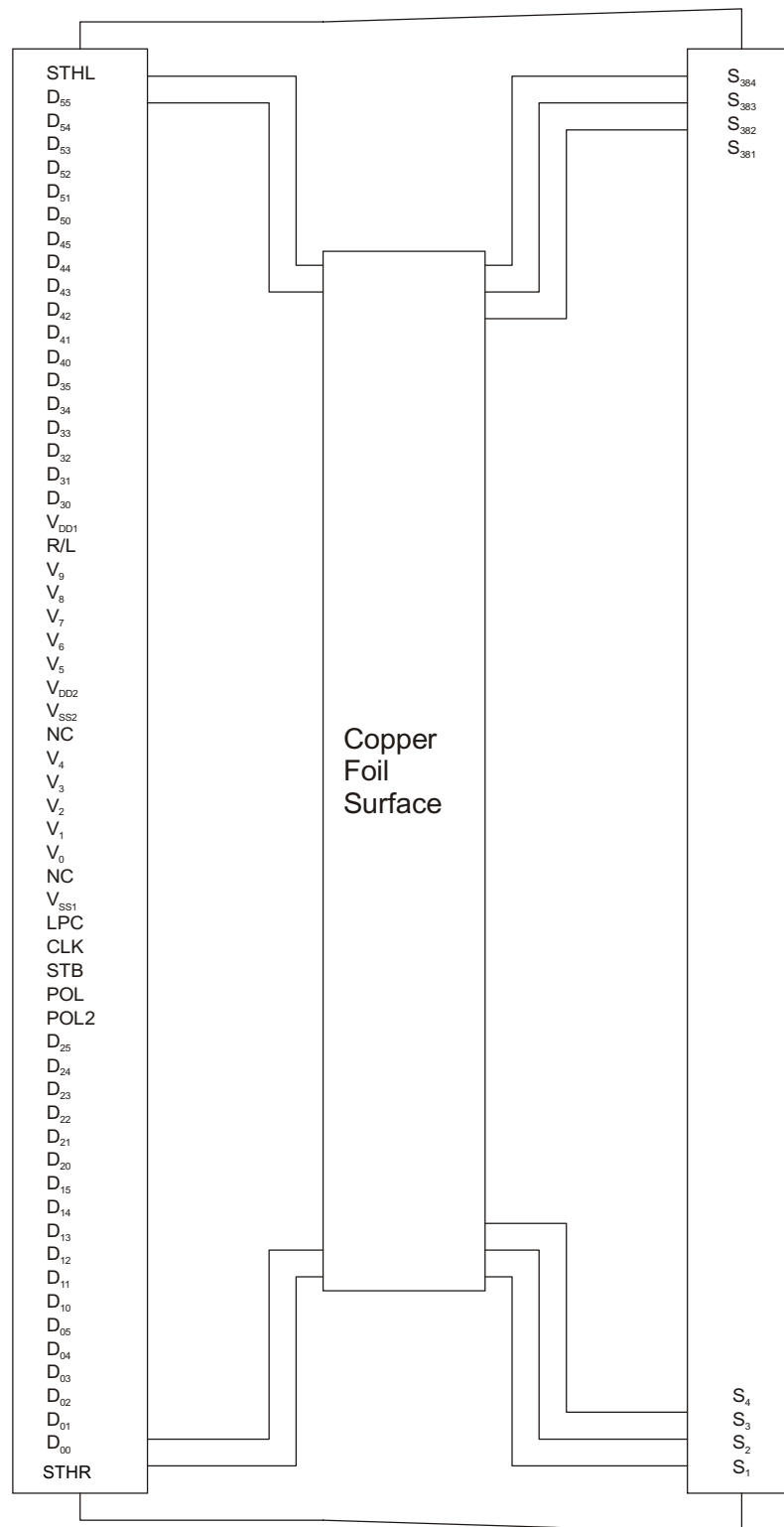


Figure 2: Pin Arrangement

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3. PIN CONFIGURATION (TCP II PACKAGE)

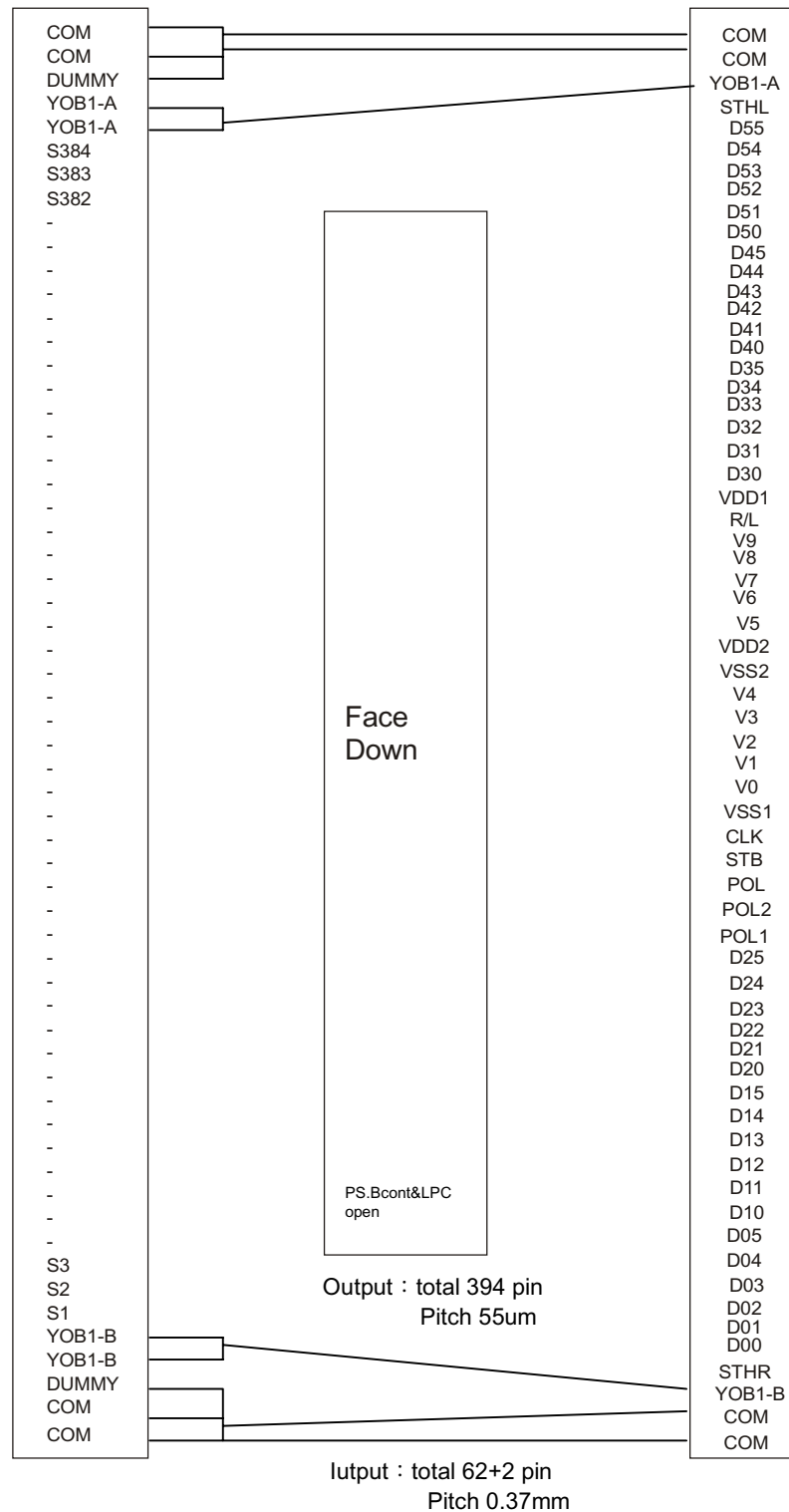


Figure 3: Pin Arrangement

4. PIN FUNCTIONS

Signal Name	Pin Type	Function
S_1 to S_{384}	Output	Signal lines for output of liquid-crystal application voltages
D_{00} to D_{05} D_{10} to D_{15} D_{20} to D_{25} D_{30} to D_{35} D_{40} to D_{45} D_{50} to D_{55}	Input	6-bit Input (grayscale data) x 6-dot display data (2pixels) <i>D_{X0}: is the LSB, D_{X5}: is the MSB</i>
R/L	Input	Controls the display data shift direction <i>$R/L = H$: $STHR$ input, $S_1 \rightarrow S_{384}$, $STHL$ output $R/L = L$: $STHL$ input, $S_{384} \rightarrow S_1$, $STHR$ output</i>
STHR	Bidir	Right shift start pulse <i>$R/L = H$: Becomes the start pulse input pin $R/L = L$: Becomes the start pulse output pin</i>
STHL	Bidir	Left shift start pulse <i>$R/L = H$: Becomes the start pulse output pin $R/L = L$: Becomes the start pulse input pin</i>
CLK	Input	Shift register clock input <i>Refers to the shift register's shift clock input. The display data are incorporated into the first stage latch at the rising edge of this clock. At the rising edge of the 64th clock after the input start pulse, the output start pulse goes high, and becomes the input start pulse of the next driver stage. After the input start pulse, display data storing is halted automatically when 66 clock pulses are input.</i>
STB	Input	Load line <i>The data of one line is transfered from the latch 1 to the latch 2 stage at the rising edge of this clock, and the liquid-crystal application voltage is output at its falling edge. Outputs are in high impedance when STB is active. One pulse must be input in each horizontal period.</i>
POL	Input	Polarity <i>$POL = L$: The S_{2n-1} outputs drive positive-polarity grayscales levels The S_{2n} outputs drive negative-polarity grayscale levels. $POL = H$: The S_{2n-1} outputs drive negative-polarity grayscales levels The S_{2n} outputs drive positive-polarity grayscale levels. S_{2n-1} indicates odd outputs and S_{2n} indicates even outputs.</i>
POL1, POL2	Input	Data inversion control of display input data <i>$POL1$ controls D_{0j} to D_{2j}, $POL2$ controls D_{3j} to D_{5j} $POLx = H$: Display data is inverted $POLx = L$: Display data is not inverted Default $POL1$ is shorted to $POL2$ on the TCP to control D_{0j} to D_{5j} simultaneously.</i>

LPC	Input (pull-up)	Low power control input <i>The nominal bias current of the output buffers can be reduced by a scale factor of two third when activating the LPC function. This pin is pulled up to the V_{DD1} power supply inside the IC.</i> <i>LPC = H or Open: Normal power mode</i> <i>LPC = L: Low power mode</i>
V_0 to V_9	Power	γ -Correction reference voltage pins <i>Input the reference voltage levels for the γ - correction. The following relationships must be maintained: $V_{DD2} - 0.1V > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.1V$</i>
V_{DD1}	Power	Logic power supply
V_{DD2}	Power	Driver power supply
V_{SS1}	Power	Logic ground
V_{SS2}	Power	Driver ground

5. SYSTEM OVERVIEW

TFT LCD panels are composed of source drivers and gate drivers. The gate driver selects one of the lines of the panel and the source driver writes the grayscale levels on each dot. A controller converts the input RGB video signals to 36-bit data display signals (2 pixels). It controls the gate and source driver ICs. A power supply unit is used to generate the 10 gamma corrected reference voltage (see point 11).

For a XGA panels (1024x 768) 8 Source drivers of 384 outputs and 3 gate drivers of 256 outputs are used. For SXGA (1280x1024) 10 Source driver and 4 gate driver are used.

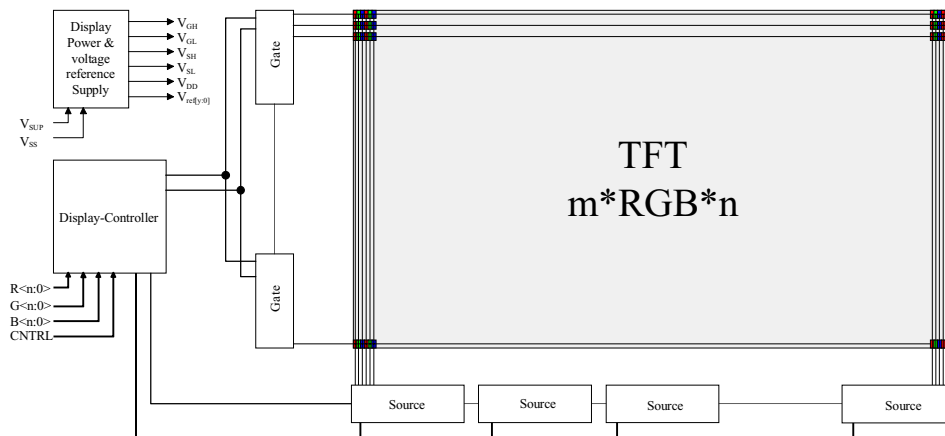


Figure 4: System block diagram

Timing diagram for the 16-bit parallel data bus (D0-D15) and control signals (CLK, STHR, STB, STHL, Latch 2, S1 to S384) during a read operation. The diagram shows the sequence of events for reading data from Line n-1 and Line n. The data bus D0-D15 is shown with data words D1-D18, D367-D402, and D3055-D3067. The control signals STB, STHL, and Latch 2 are shown as pulses. The S1 to S384 signal is shown as a high impedance state during the read operation.

Line

CLK

STHR

D0j

D1j

D2j

D3j

D4j

D5j

STB

STHL 1st Chip

STHL Last Chip

Latch 2

S1 to S384

High Z

Line n-1

Line n

R/L = VDD1 shift from left to right

The start condition is initiated by applying a start pulse to the enable input pin (STHR when $R/L=V_{DD1}$) at the beginning of each line of the first chip. During the next 64 CLK rising edges, the source driver chip stores 64 times 36 display data bits (6 grayscale code bits x 3 RGB dot x 2 pixels). While the 63rd data is being stored, it activates the enable output signal (STHL when $R/L=V_{DD1}$) to enable the following chip.

As soon as the loading of the input data for a complete line is achieved, all enable output signals are activated. Then the controller activates the STB signal to force the 384 output buffers in a high impedance state. At the next CLK rising edge, the output enable of all ICs are deactivated and the data is stored from the first stage latch to the second stage, thus, selecting one of the 64-grayscale levels. Finally, at the falling edge of STB, the 384 output buffers drive the selected grayscale levels to the panel.

7. RELATIONSHIP BETWEEN INPUT AND OUTPUT PIN

Data format: 6 bits x 2 RGB_S (6 dots)

Input width: 36 bits (2-pixel data)

R,/L = H (Right shift)

Output	S ₁	S ₂	S ₃	S ₄	...	S ₃₈₃	S ₃₈₄
Data	D ₀₀ to D ₀₅	D ₁₀ to D ₁₅	D ₂₀ to D ₂₅	D ₃₀ to D ₃₅	...	D ₄₀ to D ₄₅	D ₅₀ to D ₅₅

R,/L = L (Left shift)

Output	S ₁	S ₂	S ₃	S ₄	...	S ₃₈₃	S ₃₈₄
Data	D ₀₀ to D ₀₅	D ₁₀ to D ₁₅	D ₂₀ to D ₂₅	D ₃₀ to D ₃₅	...	D ₄₀ to D ₄₅	D ₅₀ to D ₅₅

8. RELATIONSHIP BETWEEN STB, POL AND OUTPUT WAVEFORM

Figure 6 explains the relation between the POL signal and the output voltage. As shown, the POL signal is sampled at the first CLK rising edge after the activation of STB. The resulting internal signal selects directly which output (Odd or Even) is positive or negative. As long as STB is active, the 384 output buffers are forced in a high impedance state.

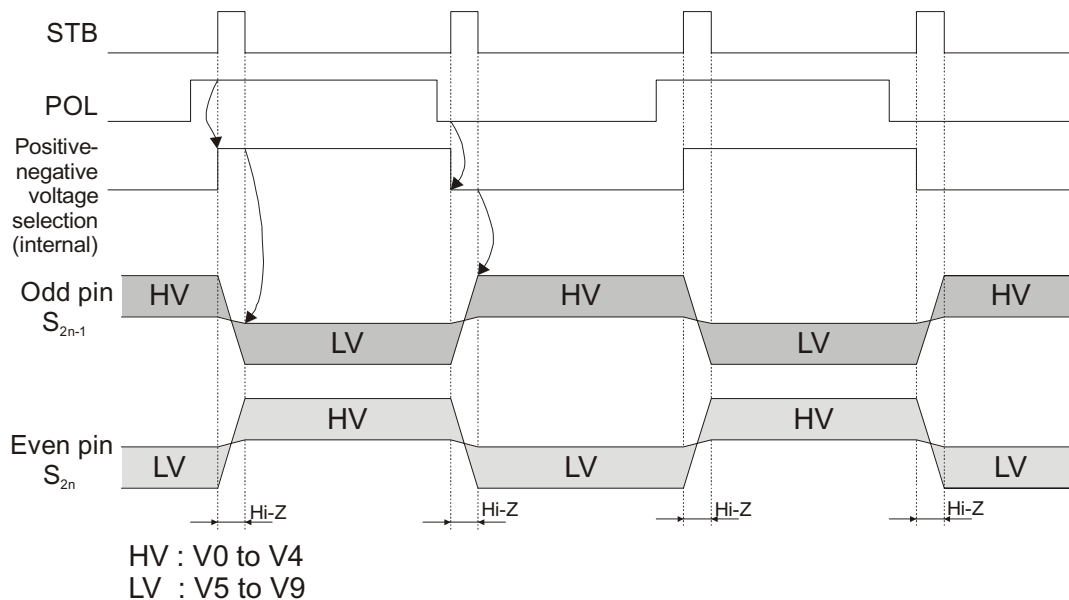


Figure 6: STB and POL timing diagram

9. CURRENT CONSUMPTION REDUCTION FUNCTION

It is strongly recommend not using LPC function for quality panels, as these functions affect directly the performance of the output buffers. However, for low-power modes, the LPC pin reduces the bias current of the output.

Low power control function (LPC)

The nominal bias current of the output buffers can be reduced by a scaling factor of one third, when activating the LPC function.

LPC = H or Open: Normal power mode

LPC = L: Low power mode

10. DRIVING SCHEMES

The EK7402 source driver features an alternate positive and negative driving scheme for the odd and even output pins. The polarity selection is achieved by the POL signal. Controlling the POL signal will enable 3 different driving schemes.

Frame-dot inversion

When POL signal is toggled every frame, the polarity inversion is applied on each dot for the same line and on each frame for the same column.

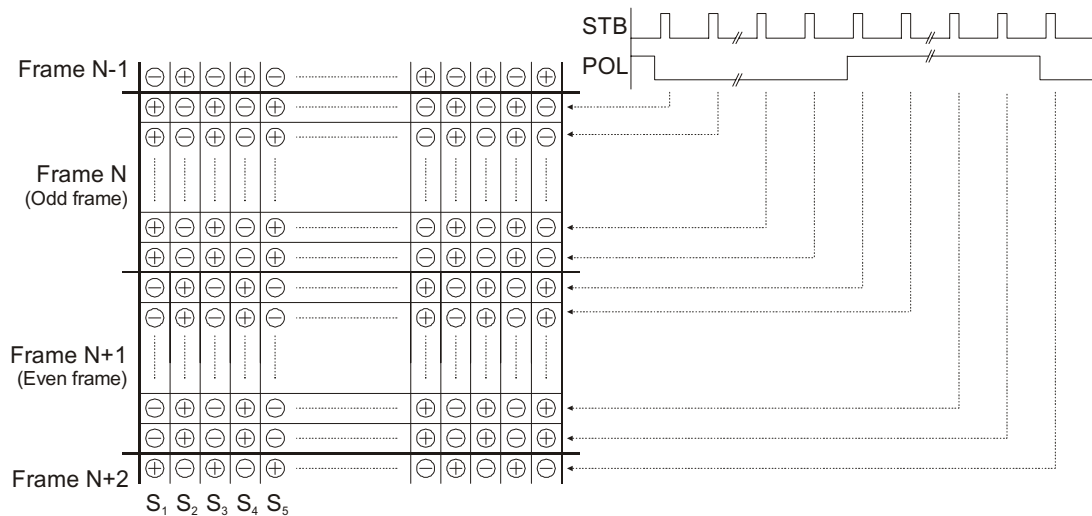


Figure 7: Frame-Dot inversion driving scheme

N-Line-Dot inversion

When POL signal is toggled every n-line, the polarity inversion is applied on each dot for the same line and on each n-line for the same column.

2-line inversion is shown in Figure 8 to illustrate such driving scheme.

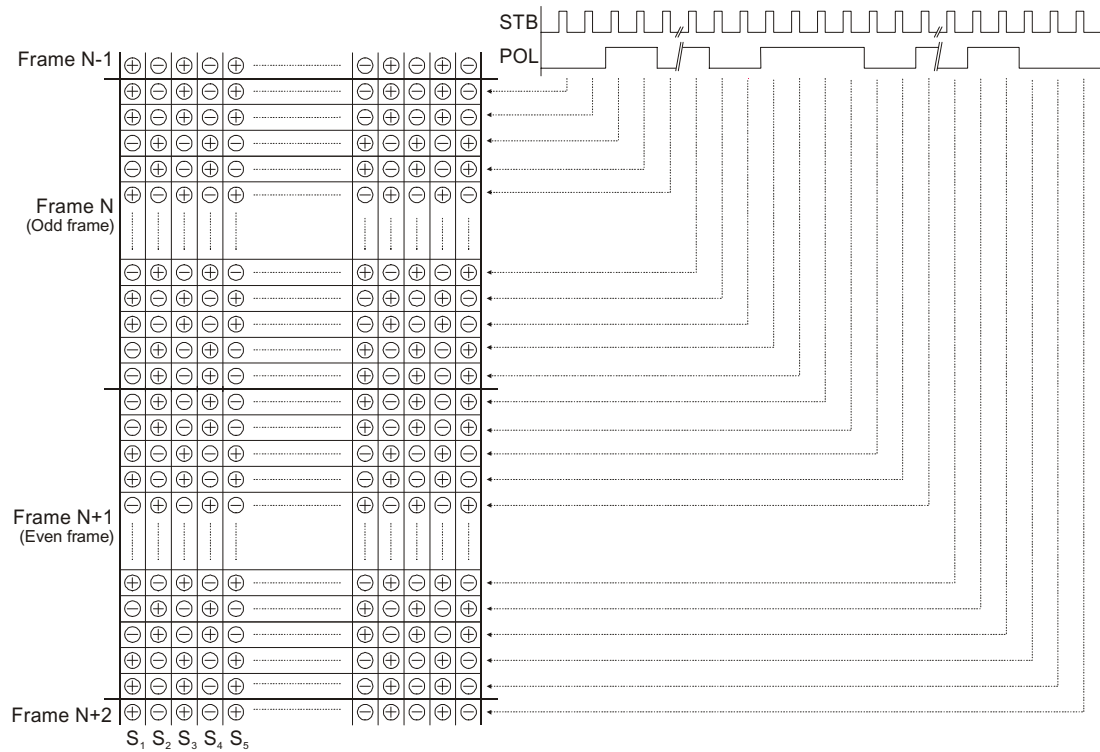


Figure 8: n-Line-Dot driving scheme

Dot-Dot inversion

When POL signal is toggled every line, the polarity inversion is applied on each dot for the same line and on each line for the same column.

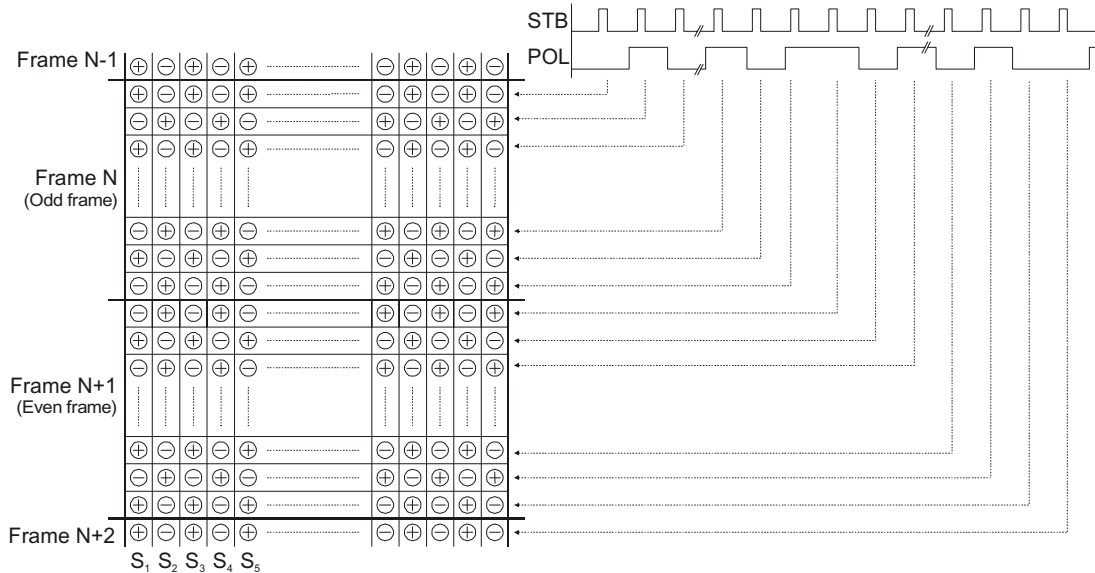


Figure 9 : Dot-Dot driving scheme

For higher quality panels, dot-dot inversion driving scheme can be used. It reduces the cross talk and the sensitivity to flickering. Moreover, odd and even frames should be alternated to avoid the polarization of the liquid.

11. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The EK7402 features two different versions (A and B) as a function of the required gamma correction. A built in 6-bits D/A converter implements the gamma correction, where two different 64 levels resistor ladders, one for the negative and one for the positive grayscale levels, are used. Five reference voltages (V_0, V_1, V_2, V_3, V_4 and V_5, V_6, V_7, V_8, V_9) connect every 16 values. When no fine precision is required on the grayscale levels, V_0, V_4, V_5 and V_9 can be connected only. With the 6 intermediate reference voltages (V_1 to V_3, V_6 to V_8), the gamma correction can be finely adjusted.

Figure 10 and Figure 11 represent the relationship between the gamma correction reference voltages, the power supplies V_{DD2} and V_{SS2} and the LCD common voltage. The following voltage relationship $V_{DD2} - 0.1V > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.1V$ must be respected.

Table 1 and Table 2 show the relationship between the input data display values and the output voltage with respect to the reference voltages.

Table 3 shows the ladder resistor values.

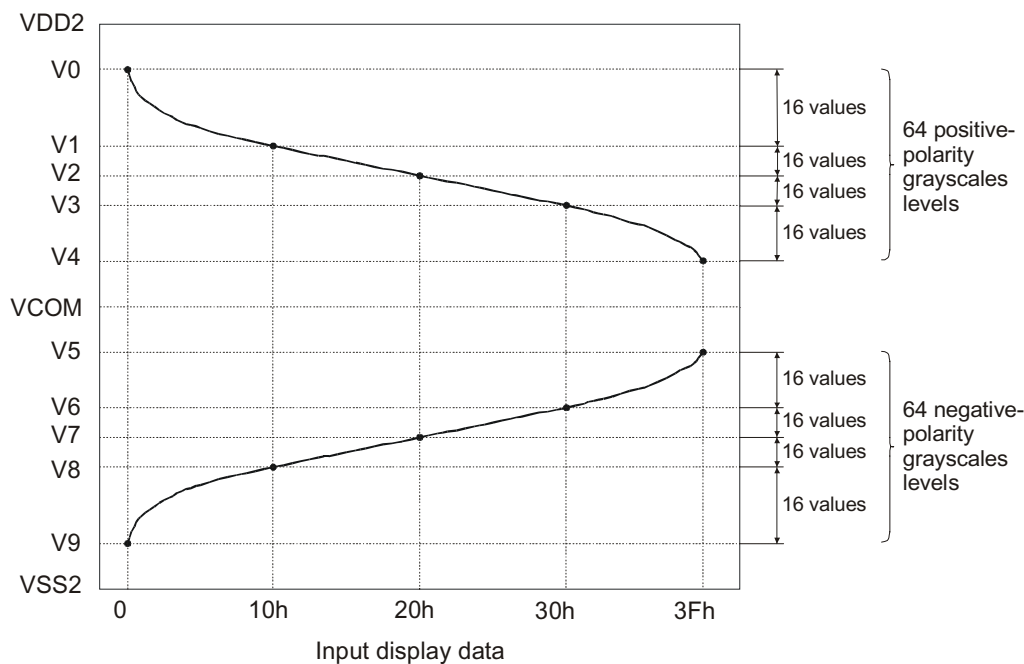


Figure 10: Gamma correction EK7402A version

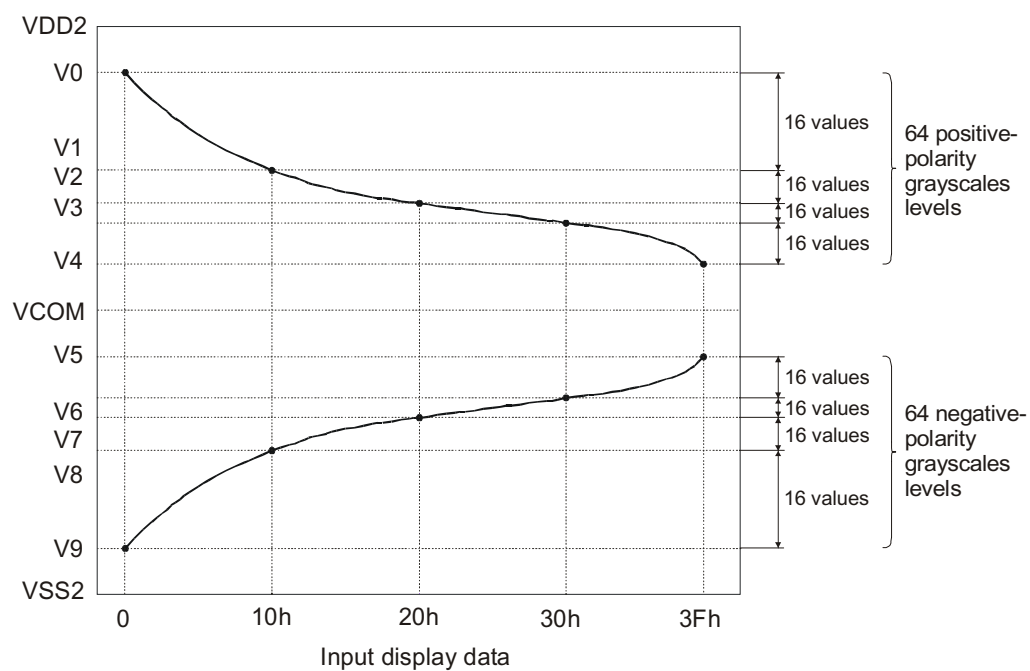


Figure 11: Gamma correction EK7402B version

Table 1: Relationship between Input Data and Output Voltage (1/2)

Data	D _{X5}	D _{X4}	D _{X3}	D _{X2}	D _{X1}	D _{X0}		Output Voltage		
									EK7402A	EK7402B
00H	0	0	0	0	0	0	V ₀ ⁻	V ₀		
01H	0	0	0	0	0	1	V ₁ ⁻	V ₁ +(V ₀ -V ₁) x	7250/8050	4585/6351
02H	0	0	0	0	1	0	V ₂ ⁻	V ₁ +(V ₀ -V ₁) x	6500/8050	3849/6351
03H	0	0	0	0	1	1	V ₃ ⁻	V ₁ +(V ₀ -V ₁) x	5800/8050	3283/6351
04H	0	0	0	1	0	0	V ₄ ⁻	V ₁ +(V ₀ -V ₁) x	5150/8050	2774/6351
05H	0	0	0	1	0	1	V ₅ ⁻	V ₁ +(V ₀ -V ₁) x	4550/8050	2378/6351
06H	0	0	0	1	1	0	V ₆ ⁻	V ₁ +(V ₀ -V ₁) x	4000/8050	2038/6351
07H	0	0	0	1	1	1	V ₇ ⁻	V ₁ +(V ₀ -V ₁) x	3450/8050	1755/6351
08H	0	0	1	0	0	0	V ₈ ⁻	V ₁ +(V ₀ -V ₁) x	2950/8050	1472/6351
09H	0	0	1	0	0	1	V ₉ ⁻	V ₁ +(V ₀ -V ₁) x	2450/8050	1246/6351
0AH	0	0	1	0	1	0	V ₁₀ ⁻	V ₁ +(V ₀ -V ₁) x	2050/8050	1020/6351
0BH	0	0	1	0	1	1	V ₁₁ ⁻	V ₁ +(V ₀ -V ₁) x	1650/8050	850/6351
0CH	0	0	1	1	0	0	V ₁₂ ⁻	V ₁ +(V ₀ -V ₁) x	1300/8050	680/6351
0DH	0	0	1	1	0	1	V ₁₃ ⁻	V ₁ +(V ₀ -V ₁) x	950/8050	510/6351
0EH	0	0	1	1	1	0	V ₁₄ ⁻	V ₁ +(V ₀ -V ₁) x	600/8050	340/6351
0FH	0	0	1	1	1	1	V ₁₅ ⁻	V ₁ +(V ₀ -V ₁) x	300/8050	170/6351
10H	0	1	0	0	0	0	V ₁₆ ⁻	V ₁		
11H	0	1	0	0	0	1	V ₁₇ ⁻	V ₂ +(V ₁ -V ₂) x	2450/2750	2280/2432
12H	0	1	0	0	1	0	V ₁₈ ⁻	V ₂ +(V ₁ -V ₂) x	2200/2750	2128/2432
13H	0	1	0	0	1	1	V ₁₉ ⁻	V ₂ +(V ₁ -V ₂) x	1950/2750	1976/2432
14H	0	1	0	1	0	0	V ₂₀ ⁻	V ₂ +(V ₁ -V ₂) x	1700/2750	1824/2432
15H	0	1	0	1	0	1	V ₂₁ ⁻	V ₂ +(V ₁ -V ₂) x	1500/2750	1672/2432
16H	0	1	0	1	1	0	V ₂₂ ⁻	V ₂ +(V ₁ -V ₂) x	1300/2750	1520/2432
17H	0	1	0	1	1	1	V ₂₃ ⁻	V ₂ +(V ₁ -V ₂) x	1100/2750	1368/2432
18H	0	1	1	0	0	0	V ₂₄ ⁻	V ₂ +(V ₁ -V ₂) x	950/2750	1216/2432
19H	0	1	1	0	0	1	V ₂₅ ⁻	V ₂ +(V ₁ -V ₂) x	800/2750	1064/2432
1AH	0	1	1	0	1	0	V ₂₆ ⁻	V ₂ +(V ₁ -V ₂) x	650/2750	912/2432
1BH	0	1	1	0	1	1	V ₂₇ ⁻	V ₂ +(V ₁ -V ₂) x	500/2750	760/2432
1CH	0	1	1	1	0	0	V ₂₈ ⁻	V ₂ +(V ₁ -V ₂) x	400/2750	608/2432
1DH	0	1	1	1	0	1	V ₂₉ ⁻	V ₂ +(V ₁ -V ₂) x	300/2750	456/2432
1EH	0	1	1	1	1	0	V ₃₀ ⁻	V ₂ +(V ₁ -V ₂) x	200/2750	304/2432
1FH	0	1	1	1	1	1	V ₃₁ ⁻	V ₂ +(V ₁ -V ₂) x	100/2750	152/2432
20H	1	0	0	0	0	0	V ₃₂ ⁻	V ₂		
21H	1	0	0	0	0	1	V ₃₃ ⁻	V ₃ +(V ₂ -V ₃) x	1500/1600	2340/2496
22H	1	0	0	0	1	0	V ₃₄ ⁻	V ₃ +(V ₂ -V ₃) x	1400/1600	2184/2496
23H	1	0	0	0	1	1	V ₃₅ ⁻	V ₃ +(V ₂ -V ₃) x	1300/1600	2028/2496
24H	1	0	0	1	0	0	V ₃₆ ⁻	V ₃ +(V ₂ -V ₃) x	1200/1600	1872/2496
25H	1	0	0	1	0	1	V ₃₇ ⁻	V ₃ +(V ₂ -V ₃) x	1100/1600	1716/2496
26H	1	0	0	1	1	0	V ₃₈ ⁻	V ₃ +(V ₂ -V ₃) x	1000/1600	1560/2496
27H	1	0	0	1	1	1	V ₃₉ ⁻	V ₃ +(V ₂ -V ₃) x	900/1600	1404/2496
28H	1	0	1	0	0	0	V ₄₀ ⁻	V ₃ +(V ₂ -V ₃) x	800/1600	1248/2496
29H	1	0	1	0	0	1	V ₄₁ ⁻	V ₃ +(V ₂ -V ₃) x	700/1600	1092/2496
2AH	1	0	1	0	1	0	V ₄₂ ⁻	V ₃ +(V ₂ -V ₃) x	600/1600	936/2496
2BH	1	0	1	0	1	1	V ₄₃ ⁻	V ₃ +(V ₂ -V ₃) x	500/1600	780/2496
2CH	1	0	1	1	0	0	V ₄₄ ⁻	V ₃ +(V ₂ -V ₃) x	400/1600	624/2496
2DH	1	0	1	1	0	1	V ₄₅ ⁻	V ₃ +(V ₂ -V ₃) x	300/1600	468/2496
2EH	1	0	1	1	1	0	V ₄₆ ⁻	V ₃ +(V ₂ -V ₃) x	200/1600	312/2496
2FH	1	0	1	1	1	1	V ₄₇ ⁻	V ₃ +(V ₂ -V ₃) x	100/1600	156/2496
30H	1	1	0	0	0	0	V ₄₈ ⁻	V ₃		
31H	1	1	0	0	0	1	V ₄₉ ⁻	V ₄ +(V ₃ -V ₄) x	3350/3450	4397/4572
32H	1	1	0	0	1	0	V ₅₀ ⁻	V ₄ +(V ₃ -V ₄) x	3250/3450	4222/4572
33H	1	1	0	0	1	1	V ₅₁ ⁻	V ₄ +(V ₃ -V ₄) x	3150/3450	4047/4572
34H	1	1	0	1	0	0	V ₅₂ ⁻	V ₄ +(V ₃ -V ₄) x	3050/3450	3872/4572
35H	1	1	0	1	0	1	V ₅₃ ⁻	V ₄ +(V ₃ -V ₄) x	2950/3450	3697/4572
36H	1	1	0	1	1	0	V ₅₄ ⁻	V ₄ +(V ₃ -V ₄) x	2800/3450	3465/4572
37H	1	1	0	1	1	1	V ₅₅ ⁻	V ₄ +(V ₃ -V ₄) x	2650/3450	3233/4572
38H	1	1	1	0	0	0	V ₅₆ ⁻	V ₄ +(V ₃ -V ₄) x	2500/3450	3001/4572
39H	1	1	1	0	0	1	V ₅₇ ⁻	V ₄ +(V ₃ -V ₄) x	2300/3450	2769/4572
3AH	1	1	1	0	1	0	V ₅₈ ⁻	V ₄ +(V ₃ -V ₄) x	2100/3450	2480/4572
3BH	1	1	1	0	1	1	V ₅₉ ⁻	V ₄ +(V ₃ -V ₄) x	1850/3450	2135/4572
3CH	1	1	1	1	0	0	V ₆₀ ⁻	V ₄ +(V ₃ -V ₄) x	1600/3450	1733/4572
3DH	1	1	1	1	0	1	V ₆₁ ⁻	V ₄ +(V ₃ -V ₄) x	1300/3450	1331/4572
3EH	1	1	1	1	1	0	V ₆₂ ⁻	V ₄ +(V ₃ -V ₄) x	800/3450	872/4572
3FH	1	1	1	1	1	1	V ₆₃ ⁻	V ₄		

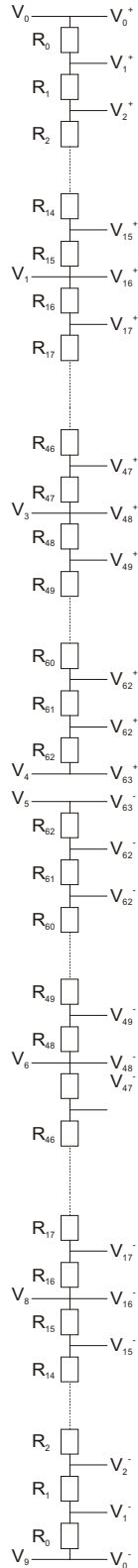
$$V_{DD2} - 0.1V > V_0 > V_1 > V_2 > V_3 > V_4 > V_5, \text{POL2} = L$$

Table 2: Relationship between Input Data and Output Voltage (2/2)

Data	D _{X5}	D _{X4}	D _{X3}	D _{X2}	D _{X1}	D _{X0}		Output Voltage		
									7402A	7402B
00H	0	0	0	0	0	0	V ₀ ⁺	V ₉		
01H	0	0	0	0	0	1	V ₁ ⁺	V ₉ +(V ₈ -V ₉) x	800/8050	1766/6351
02H	0	0	0	0	1	0	V ₂ ⁺	V ₉ +(V ₈ -V ₉) x	1550/8050	2502/6351
03H	0	0	0	0	1	1	V ₃ ⁺	V ₉ +(V ₈ -V ₉) x	2250/8050	3068/6351
04H	0	0	0	1	0	0	V ₄ ⁺	V ₉ +(V ₈ -V ₉) x	2900/8050	3577/6351
05H	0	0	0	1	0	1	V ₅ ⁺	V ₉ +(V ₈ -V ₉) x	3500/8050	3973/6351
06H	0	0	0	1	1	0	V ₆ ⁺	V ₉ +(V ₈ -V ₉) x	4050/8050	4313/6351
07H	0	0	0	1	1	1	V ₇ ⁺	V ₉ +(V ₈ -V ₉) x	4600/8050	4596/6351
08H	0	0	1	0	0	0	V ₈ ⁺	V ₉ +(V ₈ -V ₉) x	5100/8050	4879/6351
09H	0	0	1	0	0	1	V ₉ ⁺	V ₉ +(V ₈ -V ₉) x	5600/8050	5105/6351
0AH	0	0	1	0	1	0	V ₁₀ ⁺	V ₉ +(V ₈ -V ₉) x	6000/8050	5331/6351
0BH	0	0	1	0	1	1	V ₁₁ ⁺	V ₉ +(V ₈ -V ₉) x	6400/8050	5501/6351
0CH	0	0	1	1	0	0	V ₁₂ ⁺	V ₉ +(V ₈ -V ₉) x	6750/8050	5671/6351
0DH	0	0	1	1	0	1	V ₁₃ ⁺	V ₉ +(V ₈ -V ₉) x	7100/8050	5841/6351
0EH	0	0	1	1	1	0	V ₁₄ ⁺	V ₉ +(V ₈ -V ₉) x	7450/8050	6011/6351
0FH	0	0	1	1	1	1	V ₁₅ ⁺	V ₉ +(V ₈ -V ₉) x	7750/8050	6181/6351
10H	0	1	0	0	0	0	V ₁₆ ⁺	V ₈		
11H	0	1	0	0	0	1	V ₁₇ ⁺	V ₈ +(V ₇ -V ₈) x	300/2750	152/2432
12H	0	1	0	0	1	0	V ₁₈ ⁺	V ₈ +(V ₇ -V ₈) x	550/2750	304/2432
13H	0	1	0	0	1	1	V ₁₉ ⁺	V ₈ +(V ₇ -V ₈) x	800/2750	456/2432
14H	0	1	0	1	0	0	V ₂₀ ⁺	V ₈ +(V ₇ -V ₈) x	1050/2750	608/2432
15H	0	1	0	1	0	1	V ₂₁ ⁺	V ₈ +(V ₇ -V ₈) x	1250/2750	760/2432
16H	0	1	0	1	1	0	V ₂₂ ⁺	V ₈ +(V ₇ -V ₈) x	1450/2750	912/2432
17H	0	1	0	1	1	1	V ₂₃ ⁺	V ₈ +(V ₇ -V ₈) x	1650/2750	1064/2432
18H	0	1	1	0	0	0	V ₂₄ ⁺	V ₈ +(V ₇ -V ₈) x	1800/2750	1216/2432
19H	0	1	1	0	0	1	V ₂₅ ⁺	V ₈ +(V ₇ -V ₈) x	1950/2750	1368/2432
1AH	0	1	1	0	1	0	V ₂₆ ⁺	V ₈ +(V ₇ -V ₈) x	2100/2750	1520/2432
1BH	0	1	1	0	1	1	V ₂₇ ⁺	V ₈ +(V ₇ -V ₈) x	2250/2750	1672/2432
1CH	0	1	1	1	0	0	V ₂₈ ⁺	V ₈ +(V ₇ -V ₈) x	2350/2750	1824/2432
1DH	0	1	1	1	0	1	V ₂₉ ⁺	V ₈ +(V ₇ -V ₈) x	2450/2750	1976/2432
1EH	0	1	1	1	1	0	V ₃₀ ⁺	V ₈ +(V ₇ -V ₈) x	2550/2750	2128/2432
1FH	0	1	1	1	1	1	V ₃₁ ⁺	V ₈ +(V ₇ -V ₈) x	2650/2750	2280/2432
20H	1	0	0	0	0	0	V ₃₂ ⁺	V ₇		
21H	1	0	0	0	0	1	V ₃₃ ⁺	V ₇ +(V ₆ -V ₇) x	100/1600	156/2496
22H	1	0	0	0	1	0	V ₃₄ ⁺	V ₇ +(V ₆ -V ₇) x	200/1600	312/2496
23H	1	0	0	0	1	1	V ₃₅ ⁺	V ₇ +(V ₆ -V ₇) x	300/1600	468/2496
24H	1	0	0	1	0	0	V ₃₆ ⁺	V ₇ +(V ₆ -V ₇) x	400/1600	624/2496
25H	1	0	0	1	0	1	V ₃₇ ⁺	V ₇ +(V ₆ -V ₇) x	500/1600	780/2496
26H	1	0	0	1	1	0	V ₃₈ ⁺	V ₇ +(V ₆ -V ₇) x	600/1600	936/2496
27H	1	0	0	1	1	1	V ₃₉ ⁺	V ₇ +(V ₆ -V ₇) x	700/1600	1092/2496
28H	1	0	1	0	0	0	V ₄₀ ⁺	V ₇ +(V ₆ -V ₇) x	800/1600	1248/2496
29H	1	0	1	0	0	1	V ₄₁ ⁺	V ₇ +(V ₆ -V ₇) x	900/1600	1404/2496
2AH	1	0	1	0	1	0	V ₄₂ ⁺	V ₇ +(V ₆ -V ₇) x	1000/1600	1560/2496
2BH	1	0	1	0	1	1	V ₄₃ ⁺	V ₇ +(V ₆ -V ₇) x	1100/1600	1716/2496
2CH	1	0	1	1	0	0	V ₄₄ ⁺	V ₇ +(V ₆ -V ₇) x	1200/1600	1872/2496
2DH	1	0	1	1	0	1	V ₄₅ ⁺	V ₇ +(V ₆ -V ₇) x	1300/1600	2028/2496
2EH	1	0	1	1	1	0	V ₄₆ ⁺	V ₇ +(V ₆ -V ₇) x	1400/1600	2184/2496
2FH	1	0	1	1	1	1	V ₄₇ ⁺	V ₇ +(V ₆ -V ₇) x	1500/1600	2340/2496
30H	1	1	0	0	0	0	V ₄₈ ⁺	V ₆		
31H	1	1	0	0	0	1	V ₄₉ ⁺	V ₆ +(V ₅ -V ₆) x	100/3450	175/4572
32H	1	1	0	0	1	0	V ₅₀ ⁺	V ₆ +(V ₅ -V ₆) x	200/3450	350/4572
33H	1	1	0	0	1	1	V ₅₁ ⁺	V ₆ +(V ₅ -V ₆) x	300/3450	525/4572
34H	1	1	0	1	0	0	V ₅₂ ⁺	V ₆ +(V ₅ -V ₆) x	400/3450	700/4572
35H	1	1	0	1	0	1	V ₅₃ ⁺	V ₆ +(V ₅ -V ₆) x	500/3450	875/4572
36H	1	1	0	1	1	0	V ₅₄ ⁺	V ₆ +(V ₅ -V ₆) x	650/3450	1107/4572
37H	1	1	0	1	1	1	V ₅₅ ⁺	V ₆ +(V ₅ -V ₆) x	800/3450	1339/4572
38H	1	1	1	0	0	0	V ₅₆ ⁺	V ₆ +(V ₅ -V ₆) x	950/3450	1571/4572
39H	1	1	1	0	0	1	V ₅₇ ⁺	V ₆ +(V ₅ -V ₆) x	1150/3450	1803/4572
3AH	1	1	1	0	1	0	V ₅₈ ⁺	V ₆ +(V ₅ -V ₆) x	1350/3450	2092/4572
3BH	1	1	1	0	1	1	V ₅₉ ⁺	V ₆ +(V ₅ -V ₆) x	1600/3450	2437/4572
3CH	1	1	1	1	0	0	V ₆₀ ⁺	V ₆ +(V ₅ -V ₆) x	1850/3450	2839/4572
3DH	1	1	1	1	0	1	V ₆₁ ⁺	V ₆ +(V ₅ -V ₆) x	2150/3450	3241/4572
3EH	1	1	1	1	1	0	V ₆₂ ⁺	V ₆ +(V ₅ -V ₆) x	2650/3450	3700/4572
3FH	1	1	1	1	1	1	V ₆₃ ⁺	V ₅		

$$V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.1V, \text{ POL2=L}$$

Table 3: Resistance Ladder Values (Reference Values)



R	(\$\Omega\$)	
	7402A	7402B
R ₀	800	1766
R ₁	750	736
R ₂	700	566
R ₃	650	509
R ₄	600	396
R ₅	550	340
R ₆	550	283
R ₇	500	283
R ₈	500	226
R ₉	400	226
R ₁₀	400	170
R ₁₁	350	170
R ₁₂	350	170
R ₁₃	350	170
R ₁₄	300	170
R ₁₅	300	170
R ₁₆	300	152
R ₁₇	250	152
R ₁₈	250	152
R ₁₉	250	152
R ₂₀	200	152
R ₂₁	200	152
R ₂₂	200	152
R ₂₃	150	152
R ₂₄	150	152
R ₂₅	150	152
R ₂₆	150	152
R ₂₇	100	152
R ₂₈	100	152
R ₂₉	100	152
R ₃₀	100	152
R ₃₁	100	152
R ₃₂	100	156
R ₃₃	100	156
R ₃₄	100	156
R ₃₅	100	156
R ₃₆	100	156
R ₃₇	100	156
R ₃₈	100	156
R ₃₉	100	156
R ₄₀	100	156
R ₄₁	100	156
R ₄₂	100	156
R ₄₃	100	156
R ₄₄	100	156
R ₄₅	100	156
R ₄₆	100	156
R ₄₇	100	156
R ₄₈	100	175
R ₄₉	100	175
R ₅₀	100	175
R ₅₁	100	175
R ₅₂	100	175
R ₅₃	150	232
R ₅₄	150	232
R ₅₅	150	232
R ₅₆	200	232
R ₅₇	200	289
R ₅₈	250	345
R ₅₉	250	402
R ₆₀	300	402
R ₆₁	500	459
R ₆₂	800	872
R _{total}	15850	15851

Caution: there is no connection between V4 and V5 terminal in the chip

12. ELECTRICAL SPECIFICATIONS

Absolute Maximum Rating ($T_A = +25^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = 0\text{V}$)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	-0.5 to +4.0V	V
Driver Part Supply Voltage	V_{DD2}	-0.5 to +13.0V	V
Logic Part Input Voltage	V_{I1}	-0.5 to $V_{DD1} + 0.5$	V
Driver Part Supply Voltage	V_{I2}	-0.5 to $V_{DD2} + 0.5$	V
Logic Part Output Voltage	V_{O1}	-0.5 to $V_{DD1} + 0.5$	V
Driver Part Output Voltage	V_{O2}	-0.5 to $V_{DD2} + 0.5$	V
Operating Ambient Temperature	T_A	-30 to +75	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-55 to +125	$^{\circ}\text{C}$

Caution: If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum rating, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum rating.

Recommended Operating Range ($T_A = -30$ to $+75^{\circ}\text{C}$, $V_{SS1}=V_{SS2}=0\text{ V}$)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Logic Part Supply Voltage	V_{DD1}		2.3		3.6	V
Driver Part Supply Voltage	V_{DD2}		7.0	8.5	12.0	V
High-level Input Voltage	V_{IH}		$0.7 \cdot V_{DD1}$		V_{DD1}	V
Low-level Input Voltage	V_{IL}		0		$0.3 \cdot V_{DD1}$	V
γ -Corrected Voltage	V_0 to V_9		$V_{SS2} + 0.1$		$V_{DD2} - 0.1$	V
Driver Part Output Voltage	V_0		$V_{SS2} + 0.1$		$V_{DD2} - 0.1$	V
Maximum Clock Frequency	F_{MAX}	$V_{DD1}=2.3\text{V to }3.6\text{V}$			50	MHz
		$V_{DD1}=3.0\text{ to }3.6\text{V}$			65	MHz

Electrical Characteristics ($T_A = -30$ to $+75^\circ\text{C}$, $V_{DD1} = 2.3\text{V}$ to 3.6V , $V_{DD2} = 7\text{V}$ to 12V , $V_{SS1} = V_{SS2} = 0\text{V}$, Unless otherwise specified, the input level is defined to be LPC= H or Open)

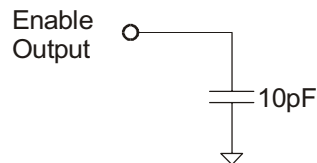
Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input Leakage Current	I _{IL}					±1.0	μA
High-level Output Voltage	V _{OH}	STHR(STHL), I _{OH} =0mA		V _{DD1} - 0.1			V
Low-level Output Voltage	V _{OL}	STHR(STHL), I _{OL} =0mA				0.1	V
γ-Corrected Supply Current	I _γ	V ₀ to V ₄ = 4.0V	V ₀ pin, V ₅ pin	189	252	325	μA
		V ₅ to V ₉ = 4.0V	V ₄ pin, V ₉ pin	-325	-252	-189	μA
Output Voltage Deviation	ΔV ₀	V _{DD1} =3.3V, V _{DD2} =8.5V,			±5	±15	mV
Output Voltage Range	V ₀	All Input data		0.1		V _{DD2} - 0.1	V
Logic Part Dynamic Current Consumption	I _{DD1}	V _{DD1} , with no load			3.0	6.0	mA
Driver Part Dynamic Current Consumption	I _{DD21}	V _{DD2} = 7-12V, with no load LPC=H			3.0	4.0	mA
	I _{DD22}	V _{DD2} = 7-12V, with no load LPC=L			2.2	2.7	mA

Cautions: 1. The STB cycle is defined to be $20\mu\text{s}$ at $F_{CLK} = 40\text{MHz}$.

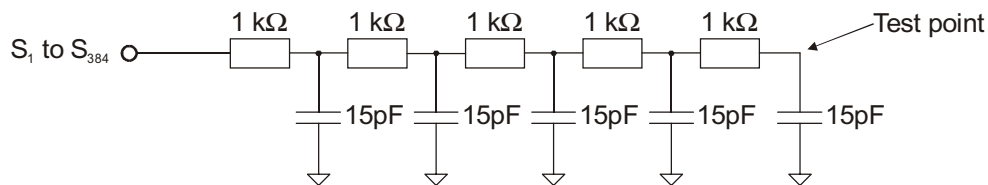
Switching Characteristics ($T_A = -30$ to $+75^\circ\text{C}$, $V_{DD1} = 2.3\text{V}$ to 3.6V , $V_{DD2} = 7$ to 12V , $V_{SS1}=V_{SS2}=0\text{V}$, Unless otherwise specified, the input level is defined to be LPC= H or Open)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	T_{SD}	$C_L = 10\text{pF}$, $V_{DD1} = 2.3\text{V}$ to 3.6V		10	15	ns
		$C_L = 10\text{pF}$, $V_{DD1} = 3.0\text{V}$ to 3.6V		7	9	ns
Driver Output Delay Time	T_{DD1}	$C_L = 75\text{pF}$, $R_L = 5\text{k}\Omega$		1	1.5	μs
	T_{DD2}			5	7	μs
Input Capacitance	C_{L1}	STHR (STHL) excluded, $T_A = +25^\circ\text{C}$		5	10	pF
	C_{L2}	STHR (STHL), $T_A = +25^\circ\text{C}$		8	10	pF

Load condition: Start pulse delay Time T_{SD} on Enable output pin



Load condition: Driver Output Delay Time T_{DD1} , T_{DD2} on output buffers

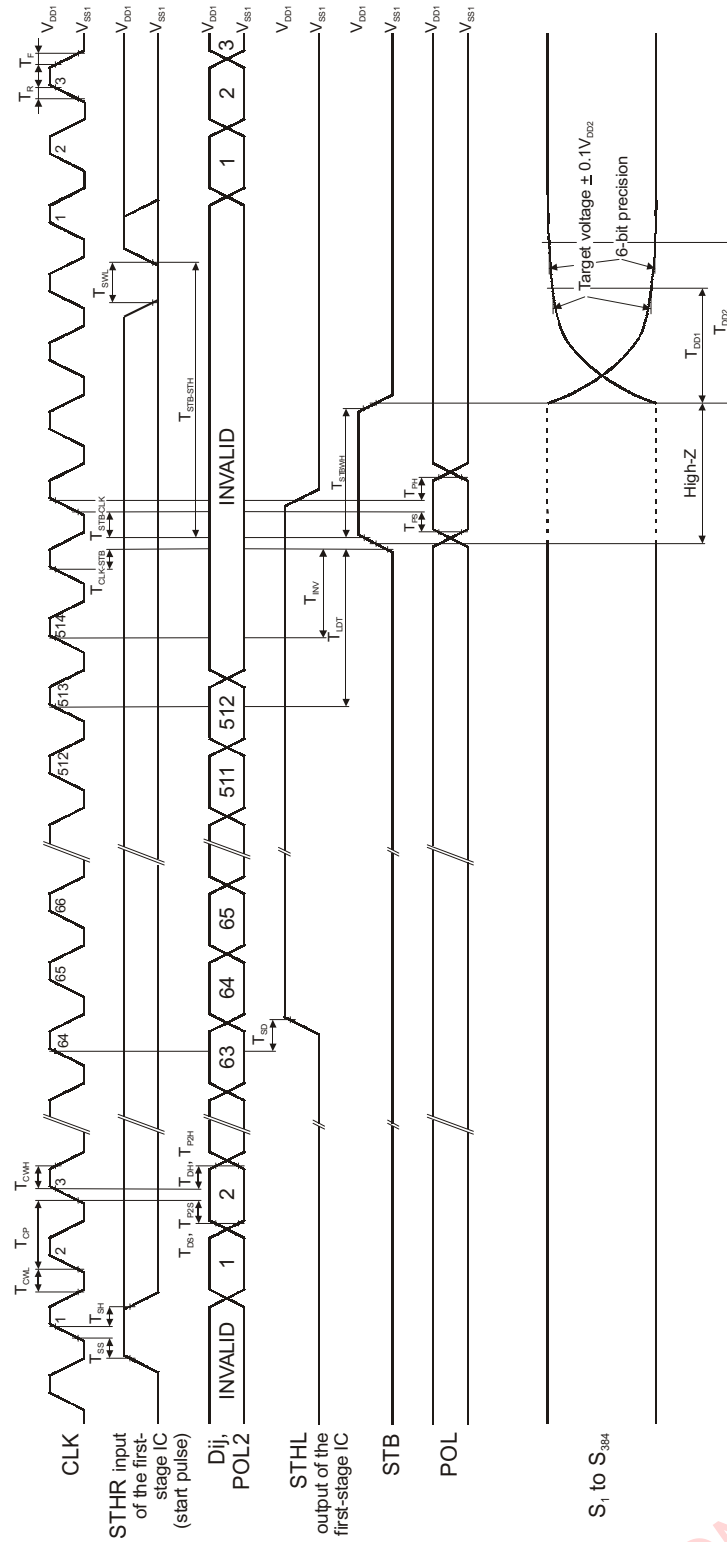


Timing Requirement ($T_A = -30$ to $+75^\circ\text{C}$, $V_{DD1} = 2.3\text{V}$ to 3.6V , $V_{SS1} = V_{SS2} = 0\text{V}$, $T_r = T_f = 8.0\text{ns}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Period	T_{CP}	$V_{DD1} = 2.3\text{V}$ to 3.6V	20			ns
		$V_{DD1} = 3.0\text{V}$ to 3.6V	15			ns
Clock high-level width	T_{CWH}		4			ns
Clock low-level width	T_{CWL}	$V_{DD1} = 2.3\text{V}$ to 3.6V	6			ns
		$V_{DD1} = 3.0\text{V}$ to 3.6V	4			ns
Data Setup Time	T_{DS}		4			ns
Data Hold Time	T_{DH}		0			ns
POL2 Setup Time	T_{P2S}		4			ns
POL2 Hold Time	T_{P2H}		0			ns
Start Pulse Setup Time	T_{SS}		4			ns
Start Pulse Hold Time	T_{SH}		0			ns
Start Pulse low-level width Time	T_{SWL}		6			ns
STB Pulse Width	T_{STBWH}		2			CLK
					4	μs
Data Invalid Period	T_{INV}		1			CLK
Last Data Timing	T_{LDT}		2			CLK
CLK-STB Timing	$T_{CLK-STB}$	$\text{CLK}\uparrow \rightarrow \text{STB}\uparrow$	2			ns
STB-CLK Timing	$T_{STB-CLK}$	$\text{STB}\uparrow \rightarrow \text{CLK}\uparrow$ $V_{DD1} = 2.3\text{V}$ to 3.6V	4			ns
		$\text{STB}\uparrow \rightarrow \text{CLK}\uparrow$ $V_{DD1} = 3.0$ to 3.6V	2			ns
Time Between STB and Start Pulse	$T_{STB-STH}$	$\text{STB}\uparrow \rightarrow \text{STHR}(\text{STHL})\uparrow$	2			CLK
POL Setup Time	T_{PS}		-5			ns
POL Hold Time	T_{PH}		6			ns

13. SWITCHING CHARACTERISTICS WAVEFORM

Unless otherwise specified, the input level is defined to $V_{IH} = 0.7 V_{DD1}$, $V_{IL} = 0.3 V_{DD1}$



14. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the EK7402.
Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

EK7402: TCP(TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C: heating for 2 to 3 Seconds: pressure 100g(per solder)
	ACF (Anisotropic Conductive Film)	Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm ² : time 3 to 5 seconds. Real bonding 165 to 180°C: pressure 25 to 45 Kg/cm ² : time 30 to 40 seconds.

15. LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Eureka customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Eureka for any damages resulting from such improper use or sale.