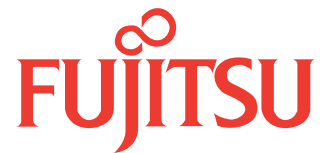


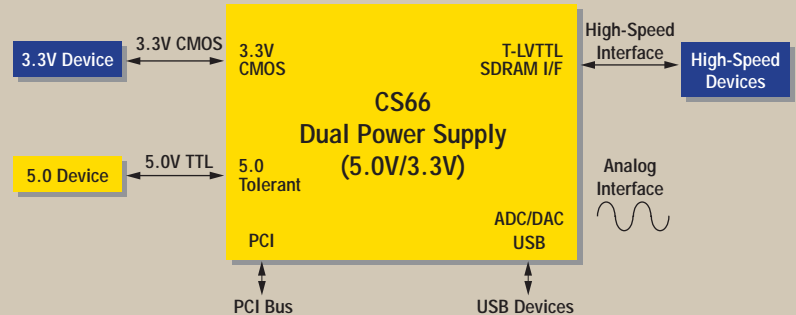
CS66 Series Standard Cell

0.35 μ m CMOS Technology



Features

- 0.28 μ m L_{eff} (0.34 μ m drawn)
- Propagation delay of 98 ps
- 0.3 μ W/gate/MHz power dissipation @ 3.3V
- Mixed-signal macros: A/D and D/A converters
- High-density diffused RAMs and ROMs
- Separate core and I/O supply voltages
- I/Os: 5V, 3.3V, 5V tolerant
- Core power supply voltage: 3.3V, 2.5V~2.0V
- Junction temperature: -40°C~125°C
- 100 μ m inline pad pitch for core-limited designs
- Special I/Os: PCI, I²C, USB
- Analog and digital PLLs
- Packaging options: QFP, HQFP, LQFP, TQFP, PBGA, FBGA
- Support for major third party EDA tools
- High-performance SRAM and DRAM



Description

Fujitsu's CS66, a 0.35 μ m (0.28 μ m L_{eff}) standard cell product is based on the state-of-the-art Fujitsu CMOS process technology—a process designed for high integration and cost effective solutions. The cell-based design enables the realization of “system-on-silicon” applications that include the following:

- User-defined logic
- Sophisticated analog functions
- High-density memory
- Intelligent peripherals
- Cores

The CS66 technology is based on an enhanced 3.3V process that provides fast performance along with 3.3V power savings. The CS66 standard cell library is an aggressive and optimal library for implementing today's high-performance deep submicron systems-on-silicon. The CS66 supports dense, high-clock frequency, system-level designs that meet the performance, integration, and power management requirements of networking, telecommunication, electronic data processing, and digital video applications. The library also supports the most popular third-party tools and data exchange file standards.

The core operates at 3.3V and 2.5V~2.0V, with I/Os operating at 3.3V, 5V, and 5V tolerant, or any combination of these. In addition to the traditional QFP packages, the CS66 family is available in Ball Grid Array. The CS66 also offers a

rich set of ADCs and DACs, analog and digital PLLs, and high-speed RAMs, ROMs, and DRAMs, along with a variety of other embedded functions.

Design Methodology

Fujitsu's design methodology ensures first-silicon success by integrating proprietary point tools with the most popular sign-off quality, industry-standard CAD tools.

Fujitsu's clock-driven design methodology offers low power and low skew. It identifies the best-suited clock distribution strategy for a given design and predicts performance in advance. Fujitsu supports co-simulation, emulation, and high-level floorplanning to ease the power, timing, and size estimation of the design. This enables the designer to make effective architectural-level decisions to achieve optimal design solutions.

Fujitsu's design methodology supports cycle-based simulators and formal verification, as well as static timing analysis and the more conventional VHDL and Verilog simulators. Fujitsu's design-for-test strategy includes boundary scan (JTAG), full and partial scan, as well as a built-in self-test for memory.

Applications

High-performance transmission and switching applications and power-sensitive applications, such as mobile computing and mobile communications, can benefit from this technology.

CS66 Series Standard Cell

Mixed-Signal Macros

D/A Converters

- 8-bit: 220 MHz (video)
- 8-bit: 50 MHz (video)
- 8-bit: 1.5 MHz (general purpose)
- 10-bit: 30 MHz (general purpose)
- 10-bit: 1.5 MHz (general purpose)

A/D Converters

- 6-bit: 300 MHz (disk)
- 8-bit: 50 MHz (video)
- 10-bit: 20 MHz (general purpose)
- 10-bit: 1 MHz (general purpose)

Multiplier Compiler

- Multiplicand (m): $4 < m < 32$
- Multiplier (n): $4 < n < 32$ (even numbers only)

Memory Macros

- SRAM Compiler: single and dual port (1 R/W, 1R), up to 72K bits per block, partial write option
- ROM Compiler: up to 512K bits per block
- Delay line: up to 32K bits

Phase-Locked Loops

- Analog: 50-200 MHz
- Digital: 180-360 MHz (Preliminary)

I/Os

- 3.3V, 5V, and 5V tolerant
- Slew-rate controlled
- CMOS, TTL, LVTTTL, T-LVTTTL, SDRAM I/E, PCI, I²C, USB

SOC IP Cores

ARC 32-bit RISC

832/833/835 SPARClite Hard Macros

Oak DSP Hard Macro

10/100 MAC

64/256 QAM

MPEG2 Decoder/Demultiplexer

8VSB TV Demodulator

AC-3 Dolby Voice Decoder

JPEG Encoder and Decoder

PCI-33/66 MHz, 32/64-bit cores

USB Host Controller/Device

I²C

IDE (ATA3) Host Controller

Smart Card I/F

IRDA I/R Interface

More IPs are being added

ASIC Design Kit and EDA Support

Verilog Logic Simulators from Cadence, Synopsys, and Mentor	Verilog-XL, NC-Verilog, VCS, Model-sim (Verilog)
VHDL/VITAL Logic Simulators from Synopsys, Cadence, and Mentor	VSS, Model-sim (VHDL), V-System, Leapfrog
Synthesis, power, DFT, and STA tools from Synopsys	Design Compiler, Design Power, Test Compiler, PrimeTime, MOTIVE, and Sunrise TestGen
Other EDA tools	Chrysalis Design Verifier

PACKAGE AVAILABILITY

No. of Pins	Frame Size
TQFP	
100	P1, P2, P3, P4, P5, P6, P7, P8, P9, PA, PB, PC, PD, PE, PF, S1, S2
LQFP	
100	P1, P2, P3, P4, P5, P6, P7, P8, P9, PA, PB, PC, PD, PE, PF, S1, S2
144	P1, P2, P3, P4, P5, P6, P7, P8, P9, PA, PB, PC, PD, PE, PF, S1, S2
176	P3, P4, P5, P6, P7, P8, P9, PA, PB, PC, PD, PE, PF
208	P6, P7, P8, P9, PA, PB, PC, PD, S5, S6, S7
QFP	
120	P1, P2, P3, P4, P5, P6, P7, P8, P9, PA, PB, PC, PD, PE, PF, S1, S2
144	P1, P2, P3, P4, P5, P6, P7, P8, P9, PA, PB, PC, PD, PE, PF, S1, S2
160	P2, P3, P4, P5, P6, P7, P8, P9, PA, PB, PC, PD, PE, PF, S2, S3, S4
176	P3, P4, P5, P6, P7, P8, P9, PA, PB, PC, PD, PE, PF, S3, S4
208	P5, P6, P7, P8, P9, PA, PB, PC, PD, PE, PF, S5, S6
240	P8, P9, PA, PB, PC, PD, PE, PF, S7, S8
256	P9, PA, PB, PC, PD, PE, PF
HQFP	
208	P5, P6, P7, P8, P9, PA, PB, PC, PD, PE, PF, S5, S6
240	P8, P9, PA, PB, PC, PD, PE, PF, S7, S8
256	P9, PA, PB, PC, PD, PE, PF, S8
304	PC, PD, PE, PF, S9, SA
PBGA	
256	P9, PA, PB, PC, PD, PE, PF, S7, S8
352	PF, SA
FBGA	
112	P2, P3, P4, P5, P6, P7, S1, S2, S3
144	P3, P4, P5, P6, P7, S1, S2, S3, S4
168	P6, P7, P8, P9, S3, S4, S5, S6, S7
176	P3, P4, P5, P6, P7, P8, P9, PA, PB, PC, PD, S3, S4
192	P4, P5, P6, P7, P8, P9, PA, PB, PC, PD, PE, PF, S4, S5
224	P7, P8, P9, PA, PB, PC, PD, PE, PF, S6, S7
288	PC, PD, PE, PF, S8, S9, SA

FUJITSU MICROELECTRONICS AMERICA, INC.

Corporate Headquarters

1250 East Arques Avenue, Sunnyvale, California 94088-3470

Tel: (800) 866-8608 Fax: (408) 737-5999

E-mail: inquiry@fma.fujitsu.com Web Site: <http://www.fma.fujitsu.com>

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