

ASSP

Fractional-N PLL Frequency Synthesizer

MB15F88UL

■ DESCRIPTION

The Fujitsu MB15F88UL is Fractional-N Phase Locked Loop (PLL) frequency synthesizer with fast lock up function. The Fractional-N PLL operating up to 2600 MHz and the integer PLL operating up to 1200 MHz are integrated on one chip.

The MB15F88UL is used as charge pump which is well-balanced output current with 1.5 mA and 6 mA selectable by serial data, direct power save control and digital lock detector. In addition, the MB15F88UL adopts a new architecture to achieve fast lock.

The new package (Thin Bump Chip Carrier20) decreases a mount area of the MB15F88UL more than 30% comparing with the former B.C.C.16 (for dual PLL, MB15F08SL) .

The MB15F88UL is ideally suited for wireless mobile communications, such as W-CDMA.

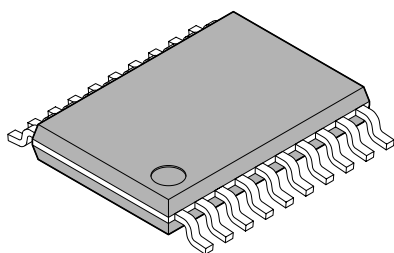
■ FEATURES

- High frequency operation : RX synthesizer : 2600 MHz Max
TX synthesizer : 1200 MHz Max
- Low power supply voltage : $V_{CC} = 2.7 \text{ V}$ to 3.6 V
- Ultra Low power supply current : $I_{CC} = 6.0 \text{ mA Typ}$ ($V_{CC} = V_P = 3.0 \text{ V}$, $T_a = +25^\circ\text{C}$, $SW = 0$ in TX and RX locking state)
- 23-bit shift register input control

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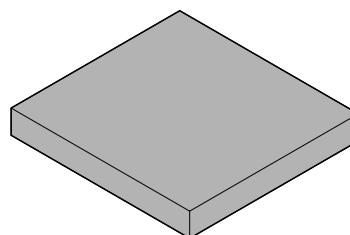
■ PACKAGES

20-pin, plastic TSSOP



(FPT-20P-M06)

20-pad, plastic BCC



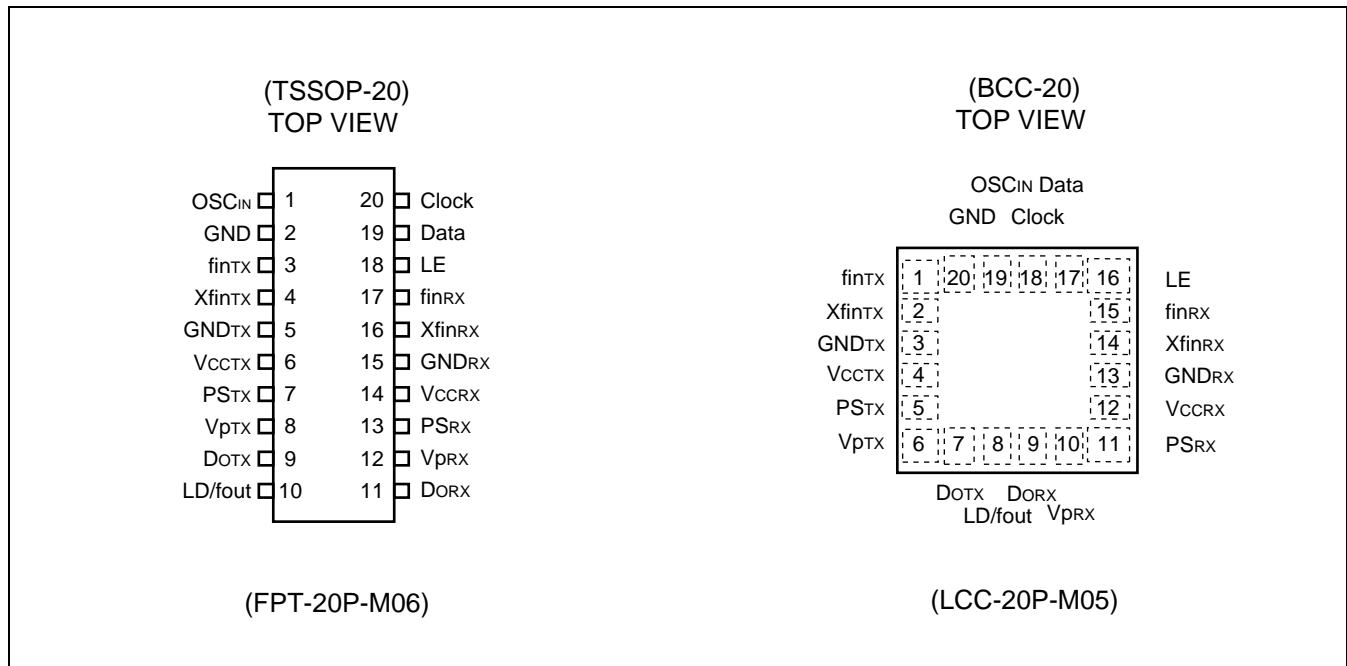
(LCC-20P-M05)

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- Direct power saving function : Power supply current in power saving mode
Typ 0.1 μ A ($V_{CC} = V_p = 3.0$ V, $T_a = +25$ °C) , Max 10 μ A ($V_{CC} = V_p = 3.0$ V)
- Fractional function : selectable modulo 5 or 8/Achieving fast lock and low phase noise (implemented in RX)
- Dual modulus prescaler : 2600 MHz prescaler (32/33 fixed) /1200 MHz prescaler (16/17 or 32/33)
- Serial input 14-bit programmable reference divider : R = 8 to 16,383
- Serial input programmable divider consisting of :
RX section - Binary 5-bit swallow counter : 0 to 31
- Binary 10-bit programmable counter : 34 to 1,023
- Binary 4-bit fractional counter numerator : 0 to 15
TX section - Binary 5-bit swallow counter : 0 to 31
- Binary 11-bit programmable counter : 3 to 2,047
- On-chip phase comparator for fast lock and low noise
- Operating temperature : $T_a = -40$ °C to $+85$ °C
- Small package Bump Chip Carrier.0 (3.4 mm \times 3.6 mm \times 0.6 mm)

PIN ASSIGNMENTS

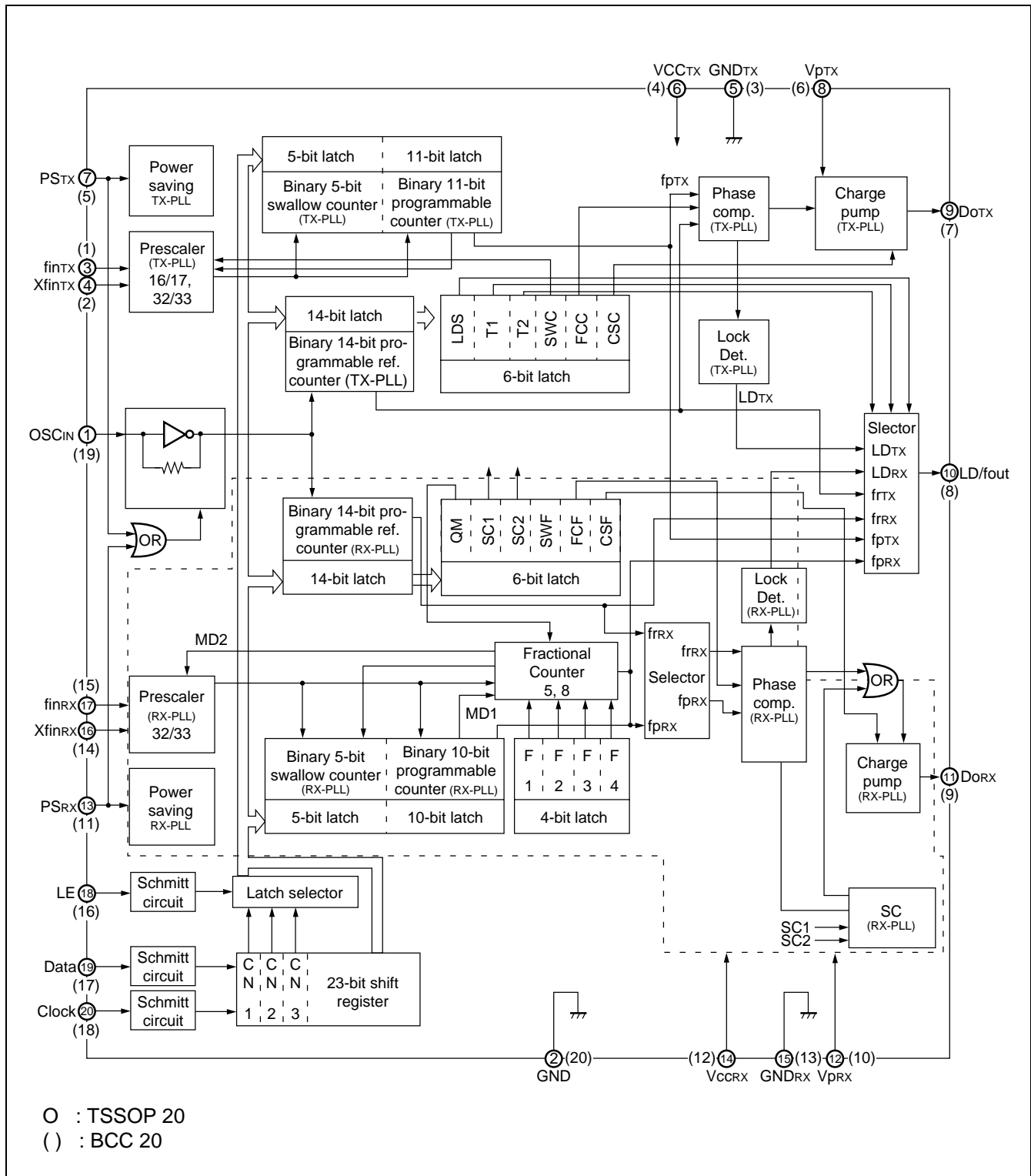


■ PIN DESCRIPTION

Pin no.		Pin name	I/O	Descriptions
TSSOP	BCC			
1	19	OSC _{IN}	I	The programmable reference divider input pin. TCXO should be connected with an AC coupling capacitor.
2	20	GND	—	Ground pin for OSC input buffer and the shift register circuit.
3	1	fin _{TX}	I	Prescaler input pin for the TX-PLL. Connection to an external VCO should be AC coupling.
4	2	Xfin _{TX}	I	Prescaler complimentary input pin for the TX-PLL section. This pin should be grounded via a capacitor.
5	3	GND _{TX}	—	Ground pin for the TX-PLL section.
6	4	V _{CCTX}	—	Power supply voltage input pin for the TX-PLL section (except for the charge pump circuit) , the shift register and the oscillator input buffer. When power is OFF, latched data of TX-PLL is lost.
7	5	PS _{TX}	I	Power saving mode control pin for the TX-PLL section. This pin must be set at “L” when the power supply is started up. (Open is prohibited.) PS _{TX} = “H” ; Normal mode, PS _{TX} = “L” ; Power saving mode
8	6	V _{pTX}	—	Power supply voltage input pin for the TX-PLL charge pump.
9	7	Do _{TX}	O	Charge pump output pin for the TX-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
10	8	LD/fout	O	Look detect signal output (LD) /phase comparator monitoring output (fout) pins. The output signal is selected by an LDS bit in a serial data. LDS bit = “H” ; outputs fout signal, LDS bit = “L” ; outputs LD signal
11	9	Do _{RX}	O	Charge pump output pin for the RX-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
12	10	V _{pRX}	—	Power supply voltage input pin for the RX-PLL charge pump.
13	11	PS _{RX}	I	Power saving mode control pin for the RX-PLL section. This pin must be set at “L” when the power supply is started up. (Open is prohibited.) PS _{RX} = “H” ; Normal mode, PS _{RX} = “L” ; Power saving mode
14	12	V _{CCRX}	—	Power supply voltage input pin for the RX-PLL section (except for the charge pump circuit) .
15	13	GND _{RX}	—	Ground pin for the RX-PLL section.
16	14	Xfin _{RX}	I	Prescaler complimentary input pin for the RX-PLL section. This pin should be grounded via a capacitor.
17	15	fin _{RX}	I	Prescaler input pin for the RX-PLL. Connection to an external VCO should be AC coupling.
18	16	LE	I	Load enable signal input pin (with the schmitt trigger circuit.) On a rising edge of load enable, data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.
19	17	Data	I	Serial data input pin (with the schmitt trigger circuit.) A data is transferred to the corresponding latch (TX-ref counter, TX-prog. counter, RX-ref. counter, RX-prog. counter) according to the control bit in a serial data.
20	18	Clock	I	Clock input pin for the 23-bit shift register (with the schmitt trigger circuit.) One bit data is shifted into the shift register on a rising edge of the clock.

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■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating		Unit
			Min	Max	
Power supply voltage		V_{CC}	-0.5	+4.0	V
		V_p	V_{CC}	+4.0	V
Input voltage		V_i	-0.5	$V_{CC} + 0.5$	V
Output voltage	LD/fout	V_o	GND	V_{CC}	V
	Do	V_{DO}	GND	V_p	V
Storage temperature		T_{stg}	-55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	$V_{CCR\bar{X}} = V_{CC\bar{T}X}$
	V_p	V_{CC}	3.0	3.6	V	
Input voltage	V_i	GND	—	V_{CC}	V	
Operating temperature	T_a	-40	—	+85	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

($V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $T_a = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power supply current		I_{CCTX}^{*1}	$f_{inTX} = 910 \text{ MHz}$, $SW_C = 0$, $V_{CCTX} = V_{pTX} = 3.0 \text{ V}$	1.3	2.0	2.8	mA
		I_{CCRX}^{*1}	$f_{inRX} = 2500 \text{ MHz}$, $V_{CCRX} = V_{pRX} = 3.0 \text{ V}$	2.6	4.0	5.6	mA
Power saving current		I_{PSTX}	PS = "L"	—	0.1^{*2}	10	μA
		I_{PSRX}	PS = "L"	—	0.1^{*2}	10	μA
Operating frequency	f_{inTX}^{*3}	f_{inTX}	TX PLL	100	—	1200	MHz
	f_{inRX}^{*3}	f_{inRX}	RX PLL	1700	—	2600	MHz
	OSC _{IN}	f_{OSC}	—	3	—	40	MHz
Input sensitivity	f_{inTX}	$P_{f_{inTX}}$	TX PLL, 50 Ω system	-15	—	+2	dBm
	f_{inRX}	$P_{f_{inRX}}$	RX PLL, 50 Ω system	-15	—	+2	dBm
	OSC _{IN}	V_{OSC}	—	0.5	—	V_{CC}	Vp-p
"H" level input voltage	Data, Clock, LE	V_{IH}	Schmitt trigger input	$0.7V_{CC}$ + 0.4	—	—	V
"L" level input voltage		V_{IL}	Schmitt trigger input	—	—	$0.3V_{CC}$ - 0.4	
"H" level input voltage	PS _{TX}	V_{IH}	—	$0.7V_{CC}$	—	—	V
"L" level input voltage	PS _{RX}	V_{IL}	—	—	—	$0.3V_{CC}$	
"H" level input current	Data, Clock, LE, PS _{TX} , PS _{RX}	I_{IH}^{*4}	—	-1.0	—	+1.0	μA
"L" level input current		I_{IL}^{*4}	—	-1.0	—	+1.0	
"H" level input current	OSC _{IN}	I_{IH}	—	0	—	+100	μA
"L" level input current		I_{IL}^{*4}	—	-100	—	0	
"H" level output voltage	LD/ f _{out}	V_{OH}	$V_{CC} = V_p = 3.0 \text{ V}$, $I_{OH} = -1 \text{ mA}$	$V_{CC} - 0.4$	—	—	V
"L" level output voltage		V_{OL}	$V_{CC} = V_p = 3.0 \text{ V}$, $I_{OL} = 1 \text{ mA}$	—	—	0.4	
"H" level output voltage	Do _{TX}	V_{DOH}	$V_{CC} = V_p = 3.0 \text{ V}$, $I_{DOH} = -0.5 \text{ mA}$	$V_p - 0.4$	—	—	V
"L" level output voltage	Do _{RX}	V_{DOL}	$V_{CC} = V_p = 3.0 \text{ V}$, $I_{DOL} = 0.5 \text{ mA}$	—	—	0.4	
High impedance cutoff current	Do _{TX} Do _{RX}	I_{OFF}	$V_{CC} = V_p = 3.0 \text{ V}$, $V_{OFF} = 0.5 \text{ V to } V_p - 0.5 \text{ V}$	—	—	2.5	nA
"H" level output current	LD/ f _{out}	I_{OH}^{*4}	$V_{CC} = V_p = 3.0 \text{ V}$	—	—	-1.0	mA
"L" level output current		I_{OL}^{*4}	$V_{CC} = V_p = 3.0 \text{ V}$	1.0	—	—	

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($V_{CC} = 2.7 \text{ V}$ to 3.6 V , $T_a = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

Parameter		Symbol	Condition		Value			Unit
					Min	Typ	Max	
“H” level output current	DoTX DoRX	IDOH *4	VCC = Vp = 3.0 V, VDOH = Vp / 2, Ta = +25 °C	CS bit = “H”	−8.2	−6.0	−4.1	mA
				CS bit = “L”	−2.2	−1.5	−0.8	mA
IDOL		VCC = Vp = 3.0 V, VDOL = Vp / 2, Ta = +25 °C	CS bit = “H”	4.1	6.0	8.2	mA	
			CS bit = “L”	0.8	1.5	2.2	mA	
Charge pump current rate	IDOL/IDOH	IDOMT *5	VDO = Vp / 2		—	3	—	%
	vs VDO	IDOVD *6	0.5 V ≤ VDO ≤ Vp − 0.5 V		—	10	—	%
	vs Ta	IDOTA *7	−40 °C ≤ Ta ≤ +85 °C, VDO = Vp / 2		—	5	—	%

*1 : Conditions ; fosc = 13 MHz, T_a = +25 °C in locking state.

*2 : V_{CCTX} = V_{pTX} = V_{CCRX} = V_{pRX} = 3.0 V, fosc = 13 MHz, T_a = +25 °C, in power saving mode.

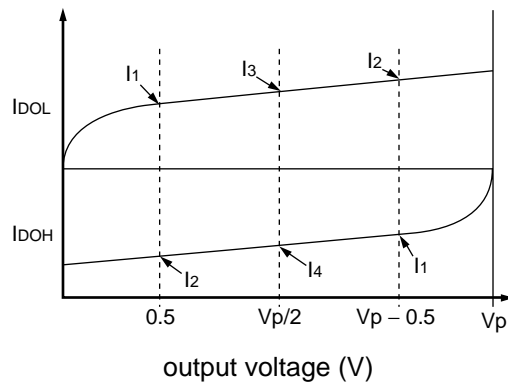
*3 : AC coupling. 1000 pF capacitor is connected.

*4 : The symbol “−” (minus) means direction of current flow.

*5 : V_{CC} = V_p = 3.0 V, T_a = +25 °C $(|I_3| - |I_4|) / [(|I_3| + |I_4|) / 2] \times 100 (\%)$

*6 : V_{CC} = V_p = 3.0 V, T_a = +25 °C $[(|I_2| - |I_1|) / 2] / [(|I_1| + |I_2|) / 2] \times 100 (\%)$ (Applied to each I_{DOL} and I_{DOH})

*7 : V_{CC} = V_p = 3.0 V, T_a = +25 °C $[(|I_{DO(+85\text{ }^{\circ}\text{C})}| - |I_{DO(-40\text{ }^{\circ}\text{C})}|) / 2] / [(|I_{DO(+85\text{ }^{\circ}\text{C})}| + |I_{DO(-40\text{ }^{\circ}\text{C})}|) / 2] \times 100 (\%)$
(Applied to each I_{DOL} and I_{DOH})



FUNCTIONAL DESCRIPTION

1. Serial Data Input

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of TX/RX-PLL sections and programmable reference dividers of TX/RX-PLL sections are controlled individually.

Serial data of binary code is entered through Data pin.

On a rising edge of clock, one bit of serial data is transferred into the shift register. On a rising edge of load enable signal, the data stored in the shift register is transferred to one of latches depending upon the control bit data setting.

	The programmable reference counter for the TX-PLL	The programmable counter and the swallow counter for the TX-PLL	The programmable reference counter for the RX-PLL	The programmable counter and the swallow counter for the RX-PLL
CN1	0	1	0	1
CN2	0	0	1	1
CN3	0	0	0	0

Note : CN3 = 1 is prohibited

(1) Serial data format

LSB Direction of data shift → MSB																						
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0	0	0	Rc1	Rc2	Rc3	Rc4	Rc5	Rc6	Rc7	Rc8	Rc9	Rc10	Rc11	Rc12	Rc13	Rc14	LDS	T1	T2	SWc	FCc	CSc
1	0	0	Ac1	Ac2	Ac3	Ac4	Ac5	0	0	Nc1	Nc2	Nc3	Nc4	Nc5	Nc6	Nc7	Nc8	Nc9	Nc10	Nc11	X	X
0	1	0	Rf1	Rf2	Rf3	Rf4	Rf5	Rf6	Rf7	Rf8	Rf9	Rf10	Rf11	Rf12	Rf13	Rf14	QM	SC1	SC2	1	FCF	CSF
1	1	0	Af1	Af2	Af3	Af4	Af5	Nf1	Nf2	Nf3	Nf4	Nf5	Nf6	Nf7	Nf8	Nf9	Nf10	F1	F2	F3	F4	0

Control bit (CN3) → bit 3

Control bit (CN2) → bit 2

Control bit (CN1) → bit 1

Rc1 to Rc14 : Divide ratio setting bits for the reference counter of the TX (8 to 16383)

Ac1 to Ac5 : Divide ratio setting bits for the swallow counter of the TX (0 to 31, A < N)

Nc1 to Nc11 : Divide ratio setting bits for the programmable counter of the TX (3 to 2047)

LDS, T1, T2 : Select bits for the lock detect output or a monitoring phase comparison frequency

SWc : Divide ratio setting for the prescaler of the TX

FCc : Phase control bit for the phase detector of the TX

CSc : Charge pump current select bit of the TX

Rf1 to Rf14 : Divide ratio setting bits for the reference counter of the RX (8 to 16383)

Af1 to Af5 : Divide ratio setting bits for the swallow counter of the RX (0 to 31, A < N - 2)

Nf1 to Nf10 : Divide ratio setting bits for the programmable counter of the RX (34 to 1023)

F1 to F4 : Fractional-N increment setting bit for the fractional accumulator (0 to 15, F < Q)

QM : Fractional-N modulus selection bit. "1" modulus = 8, "0" modulus = 5

SC1, SC2 : Spurious cancel set bit of the RX.

FCF : Phase control bit for the phase detector of the RX.

CSF : Charge pump current select bit of the RX

X : Dummy bit (Set "0" or "1")

Note: Data input with MSB first.

(2) Data Setting

• RX synthesizer Data Setting (Fractional-N)

The divide ratio can be calculated using the following equation :

$$f_{VCO_{RX}} = N_{TOTAL} \times f_{osc} \div R$$

$$N_{TOTAL} = P \times N + A + F / Q \quad (A < N - 2, F < Q)$$

- $f_{VCO_{RX}}$: Output frequency of external voltage controlled oscillator (VCO)
 N_{TOTAL} : Total division ratio from prescaler input to the phase detector input
 f_{osc} : Output frequency of the reference frequency oscillator
 R : Preset divide ratio of binary 14 bit reference counter (8 to 16383)
 P : Preset divide ratio of modulus prescaler (32 fixed)
 N : Preset divide ratio of binary 10 bit programmable counter (34 to 1023)
 A : Preset divide ratio of binary 5 bit swallow counter (0 to 31)
 F : A numerator of fractional-N (0 to 15)
 Q : A denominator of fractional-N "QM bit = 1" modulo 8, "QM bit = 0" modulo 5

• Binary 14-bit Programmable Reference Counter Data Setting (R_{F1} to R_{F14})

Divide ratio (R)	R _{F14}	R _{F13}	R _{F12}	R _{F11}	R _{F10}	R _{F9}	R _{F8}	R _{F7}	R _{F6}	R _{F5}	R _{F4}	R _{F3}	R _{F2}	R _{F1}
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
52	0	0	0	0	0	0	0	0	1	1	0	1	0	0
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note : Divide ratio less than 8 is prohibited.

• Fractional-N increment of the fractional accumulator Data Setting (F1 to F4)

Setting value(F)	F4	F3	F2	F1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
—	—	—	—	—
15	1	1	1	1

Note : F < Q, F5 = 0

• Fractional-N modulo Data Setting (Q)

QM	Modulo-Q
0	5
1	8

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• Binary 10-bit Programable Counter Data Setting (N_{F1} to N_{F10})

Divide ratio (N)	N _{F10}	N _{F9}	N _{F8}	N _{F7}	N _{F6}	N _{F5}	N _{F4}	N _{F3}	N _{F2}	N _{F1}
34	0	0	0	0	1	0	0	0	1	0
35	0	0	0	0	1	0	0	0	1	1
—	—	—	—	—	—	—	—	—	—	—
64	0	0	0	1	0	0	0	0	0	0
—	—	—	—	—	—	—	—	—	—	—
1023	1	1	1	1	1	1	1	1	1	1

Note : Divide ratio less than 34 is prohibited.

• Binary 5-bit Swallow Counter Data Setting (A_{F1} to A_{F5})

Divide ratio (A)	A _{F5}	A _{F4}	A _{F3}	A _{F2}	A _{F1}
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
—	—	—	—	—	—
31	1	1	1	1	1

Note : A < N – 2

• Spurious cancel Bit Setting

Spurious cancel amount	SC1	SC2
Large	0	0
Midium	0	1
Small	1	0

Note : The bits set how much the amount of spurious cancel.

If the Large is selected, a spurious is tended to become small.

• Phase Comparator Phase Switching Data Setting

	FC _F = "1"	FC _F = "0"
	D _o	D _o
fr > fp	H	L
fr < fp	L	H
fr = fp	Z	Z
VCO polarity	1	2

Notes : • Z = High-Z

• Depending upon the VCO and LPF polarity, FC bit should be set.

• Charge pump current select Bit Setting

CS _F	Current value
1	±6.0 mA
0	±1.5 mA

• TX synthesizer Data Setting (Integer)

The divide ratio can be calculated using the following equation :

$$f_{VCO_{TX}} = [(P \times N) + A] \times f_{osc} \div R \quad (A < N)$$

$f_{VCO_{TX}}$: Output frequency of external voltage controlled oscillator (VCO)

P : Preset divide ratio of modulus prescaler (16 or 32)

N : Preset divide ratio of binary 11 bit programmable counter (3 to 2047)

A : Preset divide ratio of binary 5 bit swallow counter (0 to 31)

f_{osc} : Output frequency of the reference frequency oscillator

R : Preset divide ratio of binary 14 bit reference counter (8 to 16383)

• Binary 14-bit Programmable Reference Counter Data Setting (Rc1 to Rc14)

Divide ratio (R)	Rc14	Rc13	Rc12	Rc11	Rc10	Rc9	Rc8	Rc7	Rc6	Rc5	Rc4	Rc3	Rc2	Rc1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note : Divide ratio less than 8 is prohibited.

• Binary 11-bit Programmable Counter Data Setting (Nc1 to Nc11)

Divide ratio (N)	Nc11	Nc10	Nc9	Nc8	Nc7	Nc6	Nc5	Nc4	Nc3	Nc2	Nc1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
—	—	—	—	—	—	—	—	—	—	—	—
2047	1	1	1	1	1	1	1	1	1	1	1

Note : Divide ratio less than 3 is prohibited.

• Binary 5-bit Swallow Counter Data Setting (Ac1 to Ac5)

Divide ratio (A)	Ac5	Ac4	Ac3	Ac2	Ac1
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
—	—	—	—	—	—
31	1	1	1	1	1

Note : $A < N$, Ac6 to Ac7 = 0

• Prescaler Data Setting (SWc)

SWc	Prescaler divide ratio
1	16/17
0	32/33

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• Phase Comparator Phase Switching Data Setting

	FC _C = "1"	FC _C = "0"
	D _o	D _o
fr > fp	H	L
fr < fp	L	H
fr = fp	Z	Z
VCO polarity	1	2

Notes : • Z = High-Z

- Depending upon the VCO and LPF polarity, FC bit should be set.

• Charge pump current select Data Setting (CS_C)

CS _C	D _o current
1	±6.0 mA
0	±1.5 mA

• Common Setting

• LD/fout Output Select Data Setting

LD/fout		LDS	T1	T2
LD output		0	—	—
fout output	fr _{TX}	1	0	0
	fr _{RX}	1	1	0
	fp _{TX}	1	0	1
	fp _{RX}	1	1	1

• FC Bit Setting

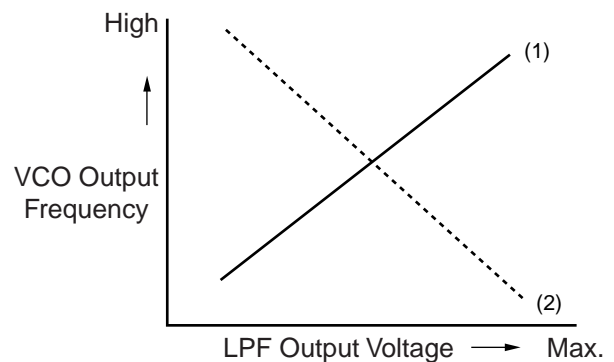
When designing a synthesizer, the FC bit setting depends on the VCO and LPF characteristics

When the LPF and VCO characteristics are similar to (1) ,

FC : "H".

When the VCO characteristics are similar to (2) ,

FC : "L".



2. Power Saving Mode (Intermittent Mode Control)

• PS Pin Setting

PS pin	Status
H	Normal mode
L	Power saving mode

The intermittent mode control circuit reduces the PLL power consumption.

By setting the PS pin low, the device enters the power saving mode, reducing the current consumption. See “■ELECTRICAL CHARACTERISTICS” for the specific value.

The phase detector output, Do, becomes high impedance.

For the single PLL, the lock detector, LD, remains high, indicating a locked condition.

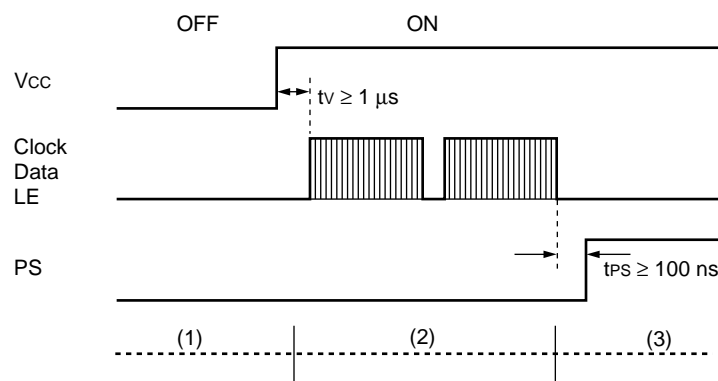
For the dual PLL, the lock detector, LD, is shown in “■PHASE DETECTOR OUTPUT WAVEFORM the LD Output Logic table” .

Setting the PS pin high releases the power saving mode, and the device works normally.

The intermittent mode control circuit also ensures a smooth start-up when the device returns to normal operation. When the PLL is returned to normal operation, the phase comparator output signal is unpredictable. This is because of the unknown relationship between the comparison frequency (f_p) and the reference frequency (f_r) which can cause a major change in the comparator output, resulting in a VCO frequency jump and an increase in lockup time.

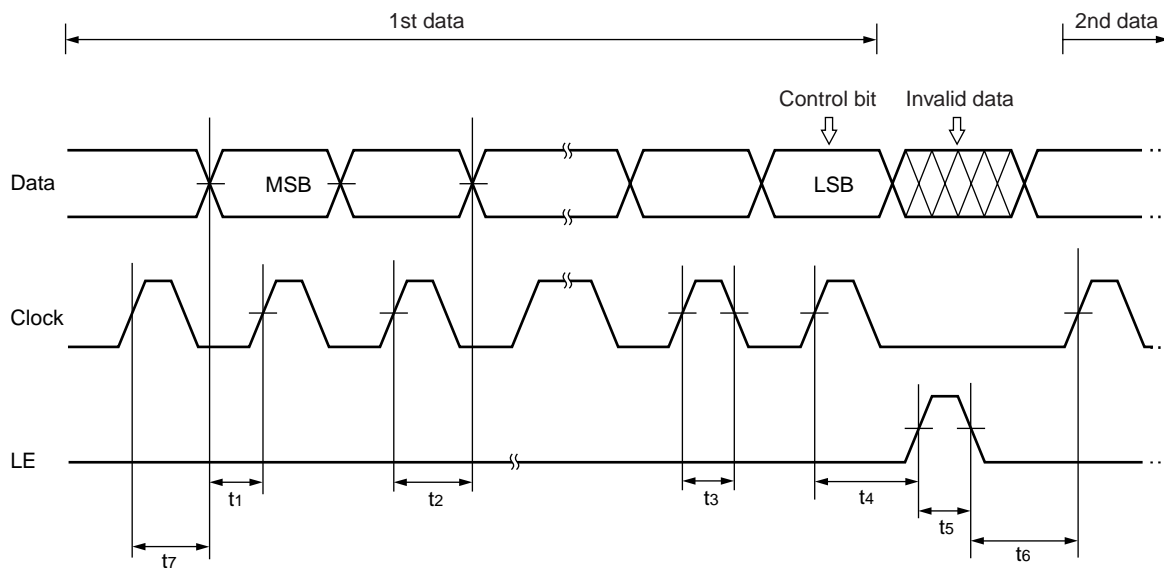
To prevent a major VCO frequency jump, the intermittent mode control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

- Notes :
- When power (V_{CC}) is first applied, the device must be in standby mode and PS = Low, for at least 1 μs .
 - PS pin must be set “L” for Power ON.



- (1) PS = L (power saving mode) at Power ON
- (2) Set serial data 1 μs after power supply remains stable ($V_{CC} \geq 2.2 V$) .
- (3) Release power saving mode (PS : L \rightarrow H) 100 ns after setting serial data.

3. Serial Data Input Timing



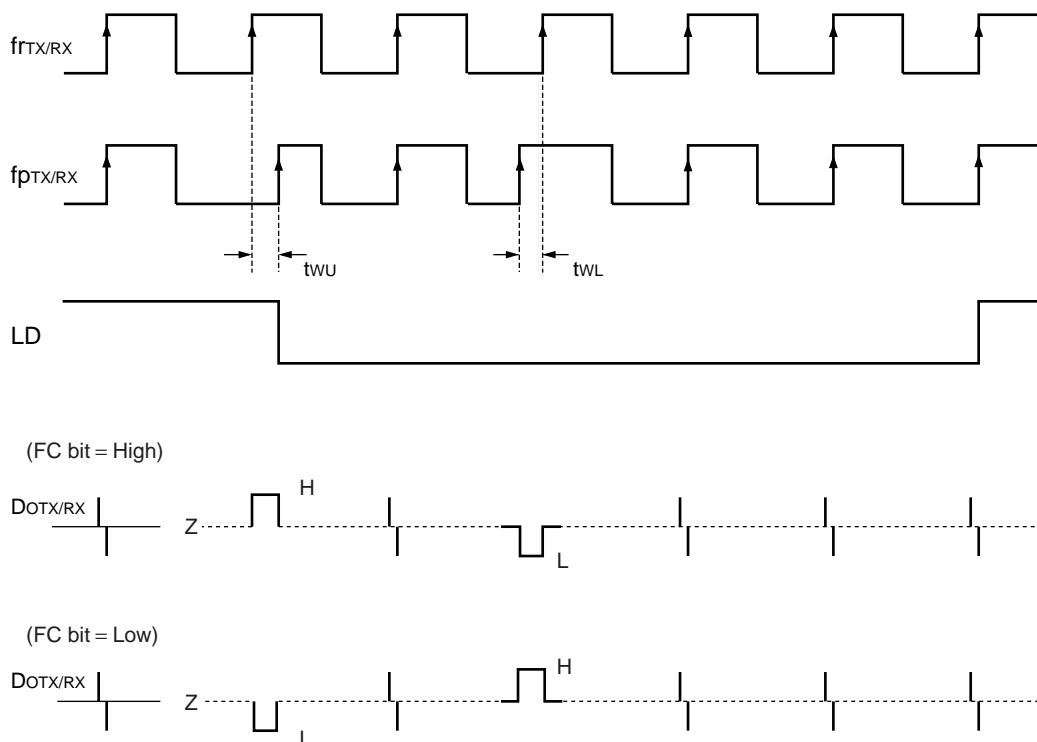
On the rising edge of the clock, one bit of data is transferred into shift register.

Parameter	Min	Typ	Max	Unit
t ₁	20	—	—	ns
t ₂	20	—	—	ns
t ₃	30	—	—	ns
t ₄	30	—	—	ns

Parameter	Min	Typ	Max	Unit
t ₅	100	—	—	ns
t ₆	20	—	—	ns
t ₇	100	—	—	ns

Note : LE should be "L" when the data is transferred into the shift register.

■ PHASE DETECTOR OUTPUT WAVEFORM



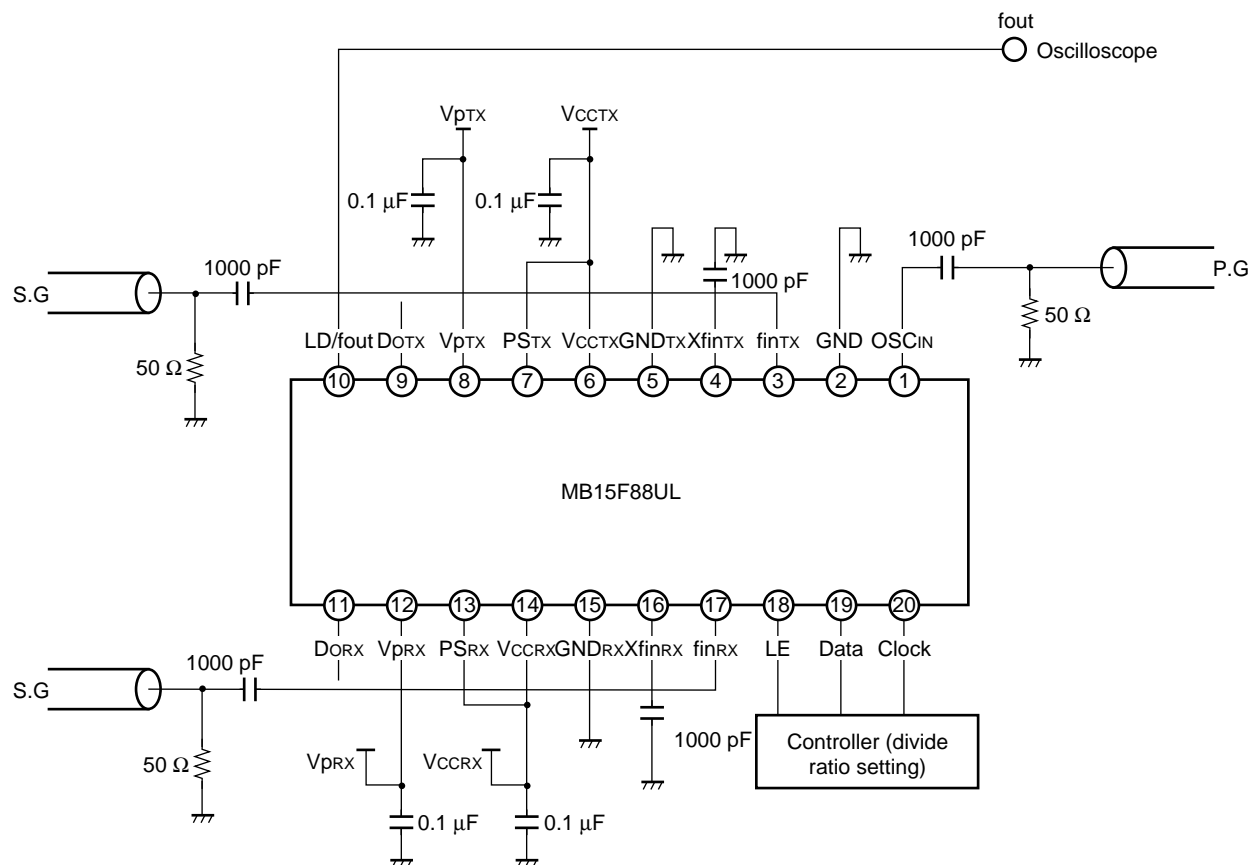
LD Output Logic Table

TX-PLL section	RX-PLL section	LD output
Locking state/Power saving state	Locking state/Power saving state	H
Locking state/Power saving state	Unlocking state	L
Unlocking state	Locking state/Power saving state	L
Unlocking state	Unlocking state	L

- Notes :
- Phase error detection range = -2π to $+2\pi$
 - Pulses on $Do_{TX/RX}$ signals are output to prevent dead zone.
 - LD output becomes low when phase error is t_{WU} or more.
 - LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
 - t_{WU} and t_{WL} depend on OSC_{IN} input frequency as follows.
 $t_{WU} \geq 2/f_{osc}$: i.e. $t_{WU} \geq 153.8$ ns when $f_{osc} = 13$ MHz
 $t_{WL} \leq 4/f_{osc}$: i.e. $t_{WL} \leq 307.6$ ns when $f_{osc} = 13$ MHz

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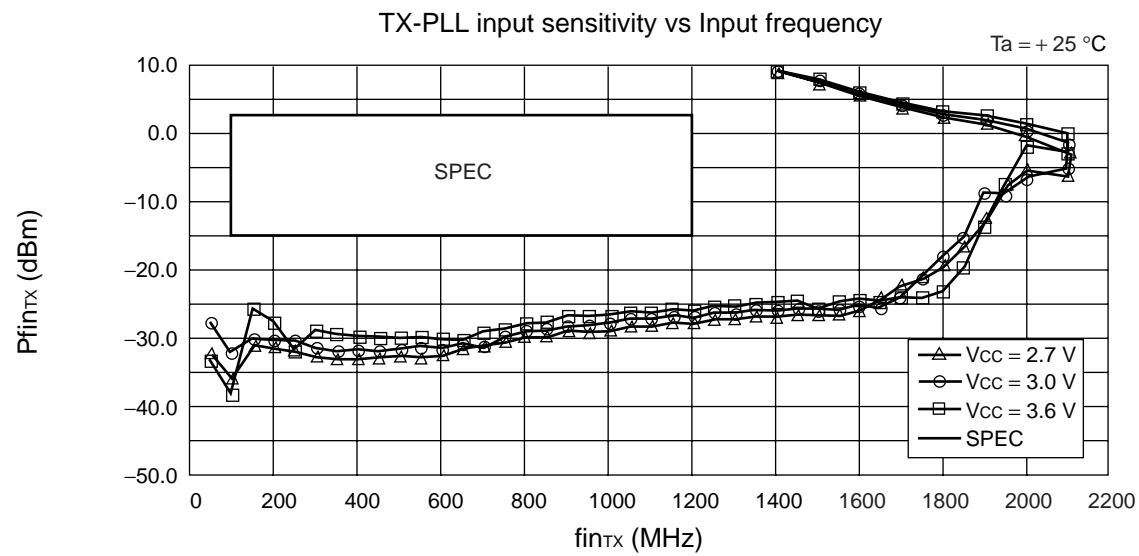
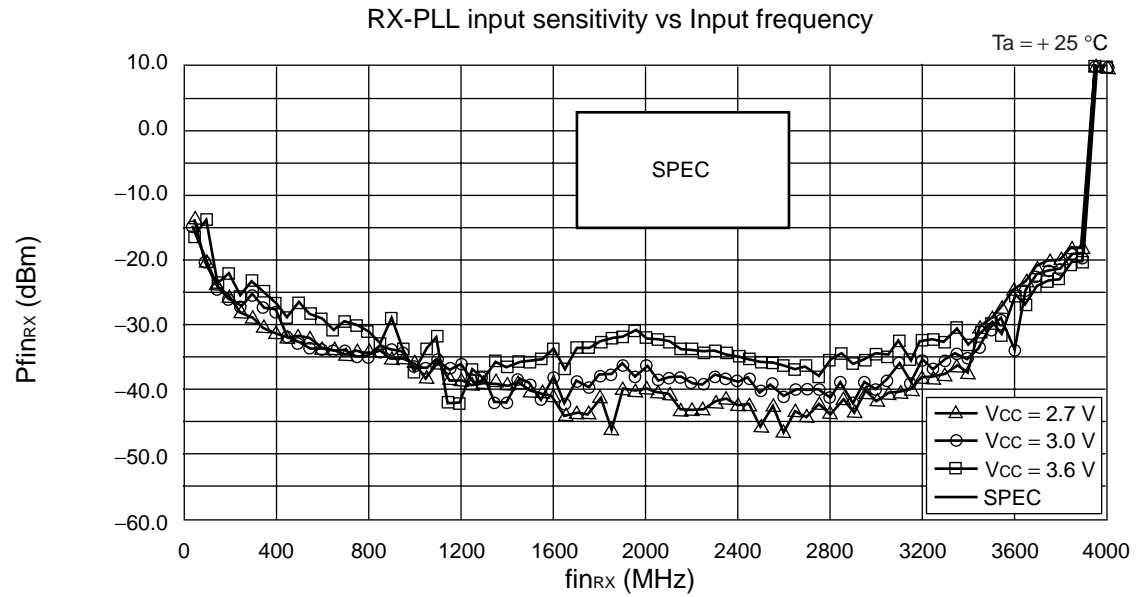
■ TEST CIRCUIT (for Measuring Input Sensitivity fin/OSC_{IN})



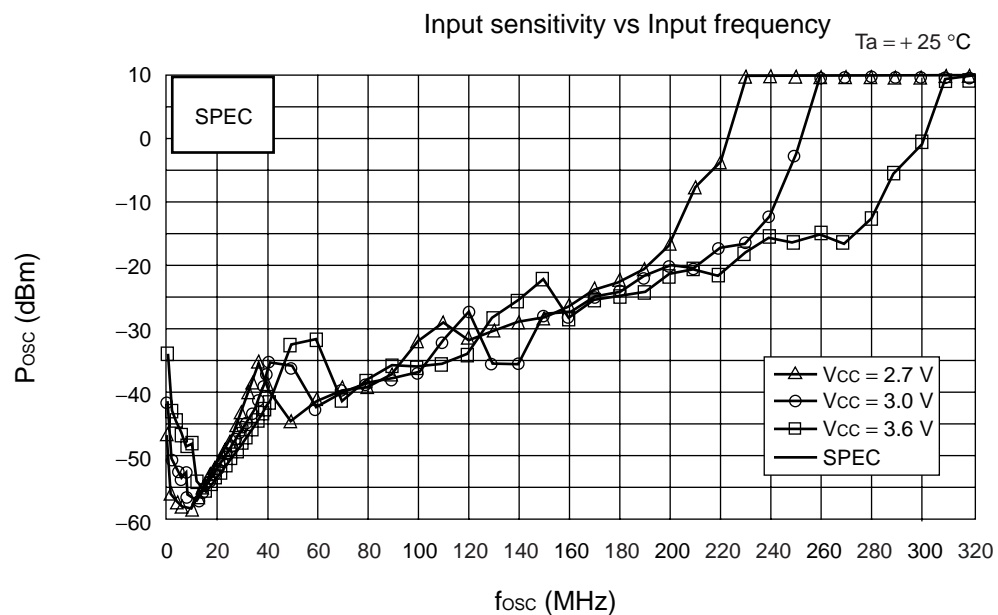
Note : TSSOP-20

■ TYPICAL CHARACTERISTICS

1. fin input sensitivity

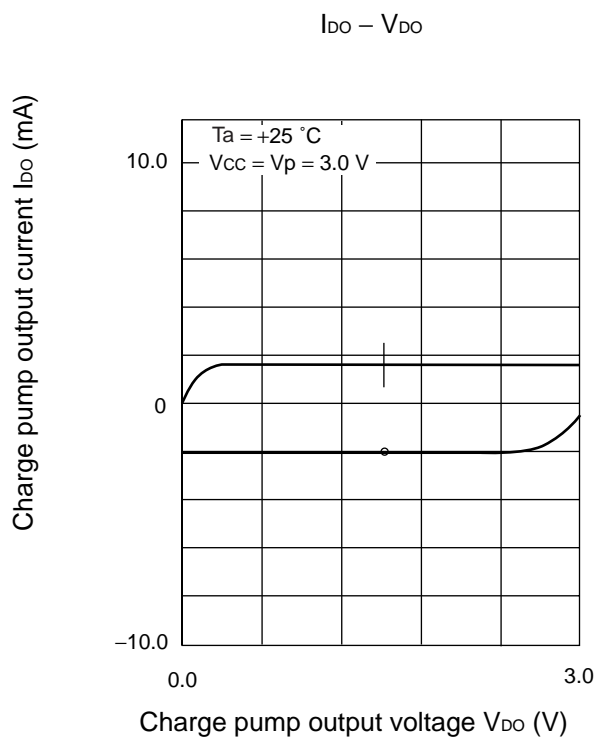


2. OSC_{IN} input sensitivity

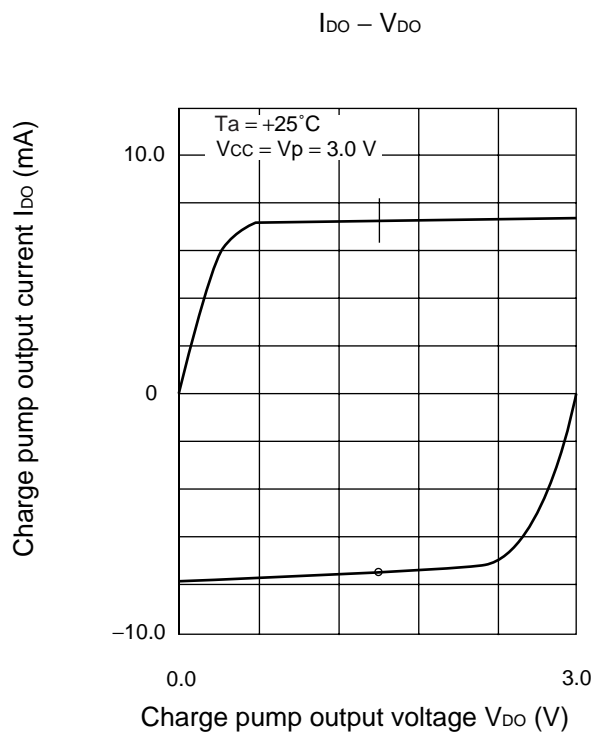


3. RX-PLL Do output current

- 1.5 mA mode

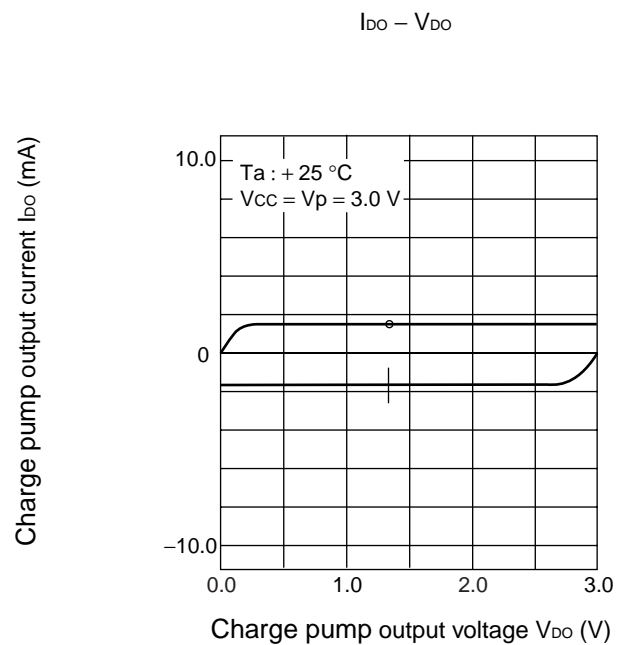


- 6.0 mA mode

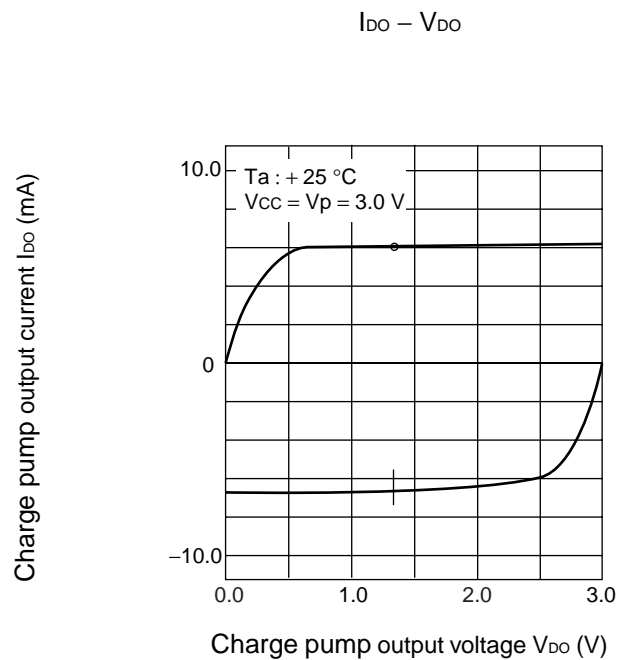


4. TX-PLL Do output current

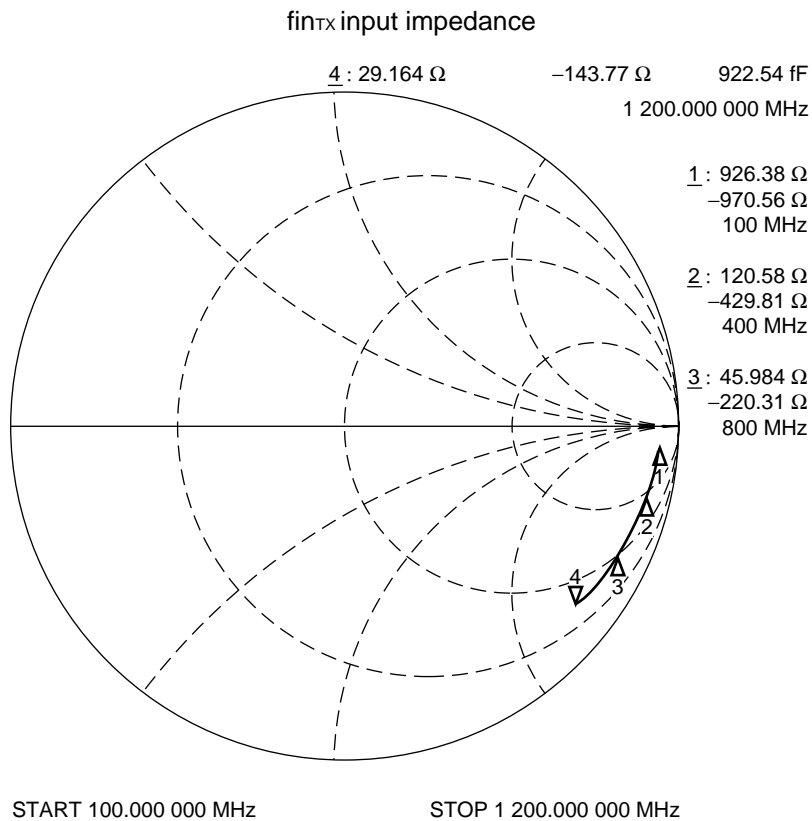
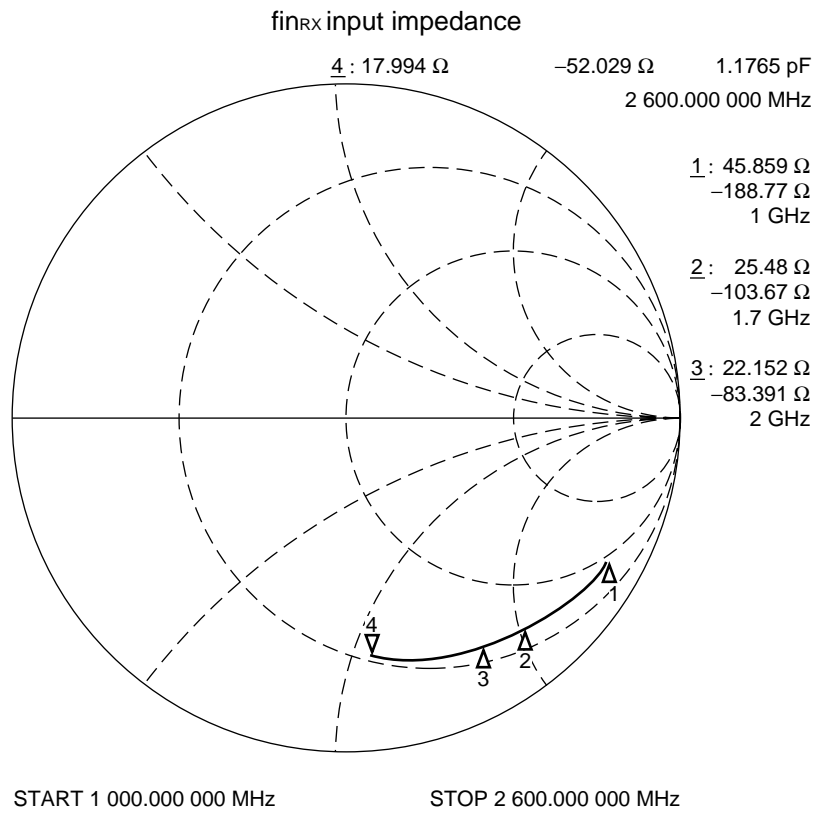
- 1.5 mA mode



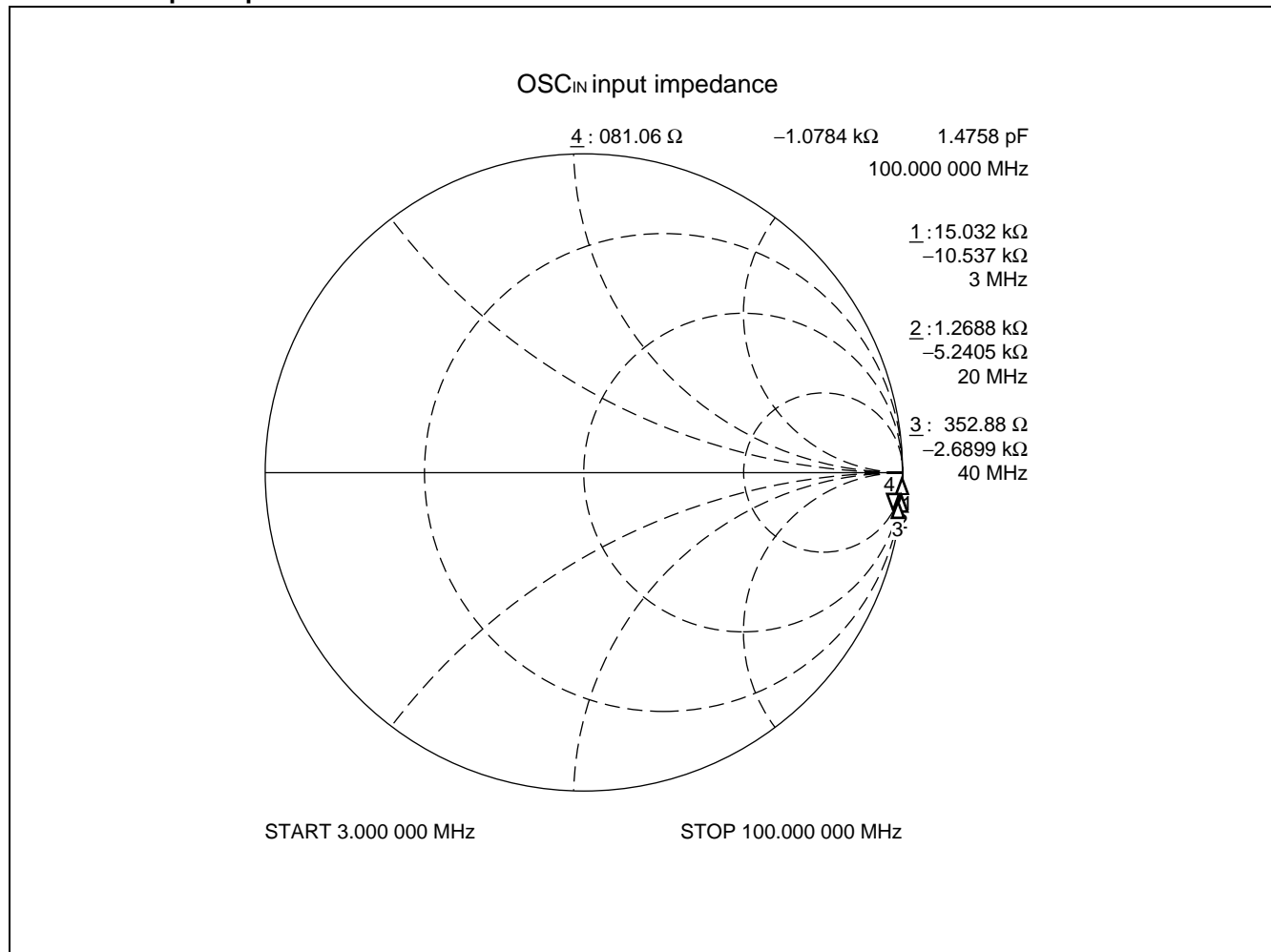
- 6.0 mA mode



5. fin input impedance

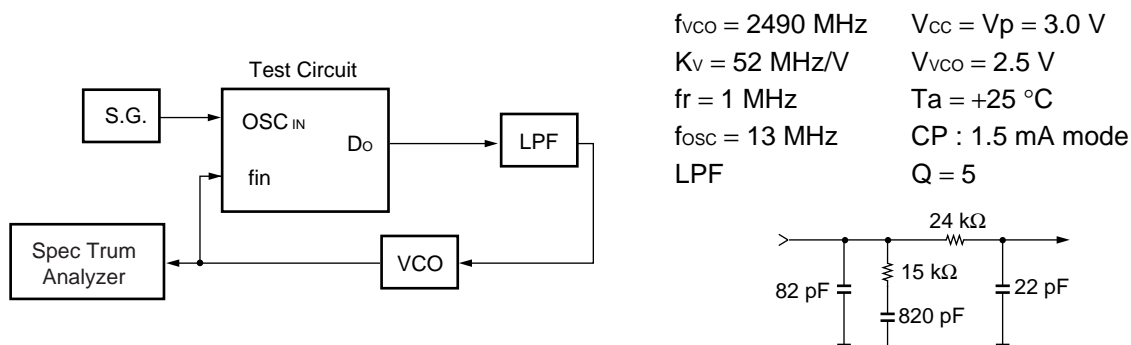


6. OSC_{IN} input impedance

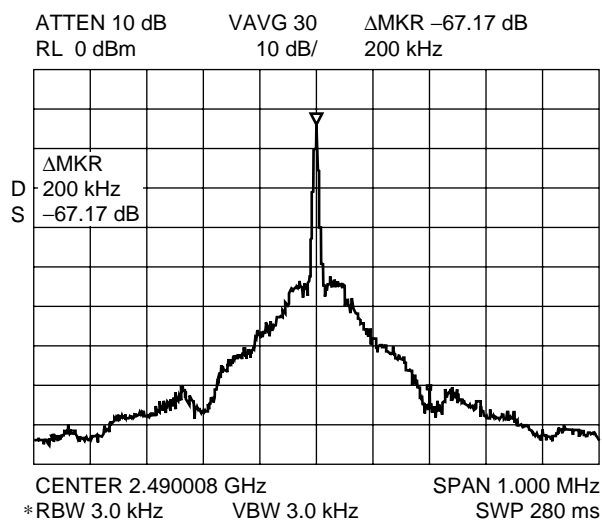


REFERENCE INFORMATION

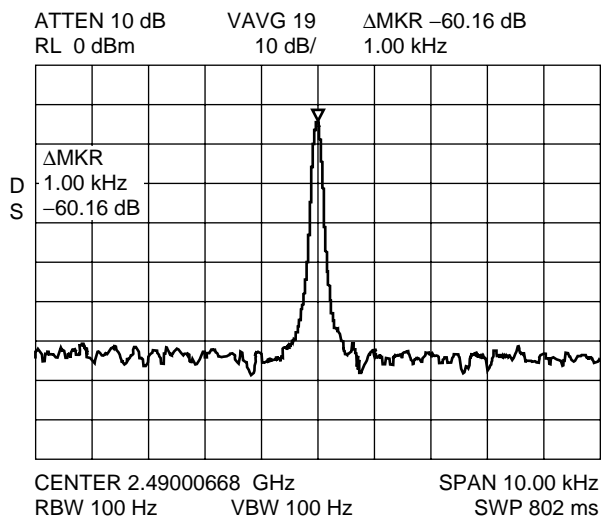
(for Lock-up Time, Phase Noise and Reference Leakage)



• PLL Reference Leakage



• PLL Phase Noise

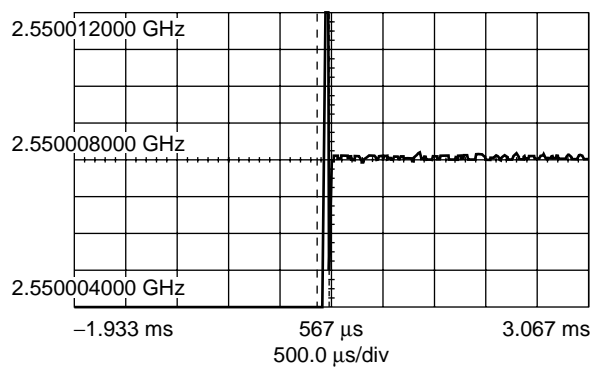


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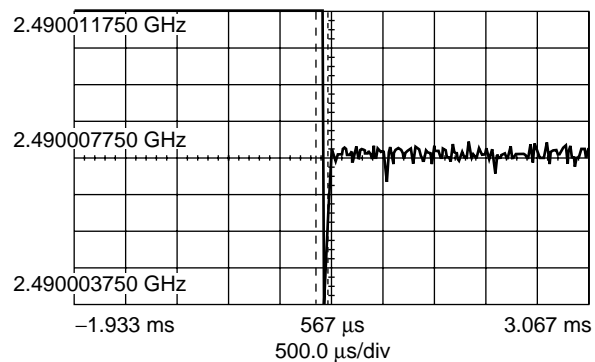
• PLL Lock Up time

2490 MHz \rightarrow 2550 MHz within ± 1 kHz
Lch \rightarrow Hch 144 μ s

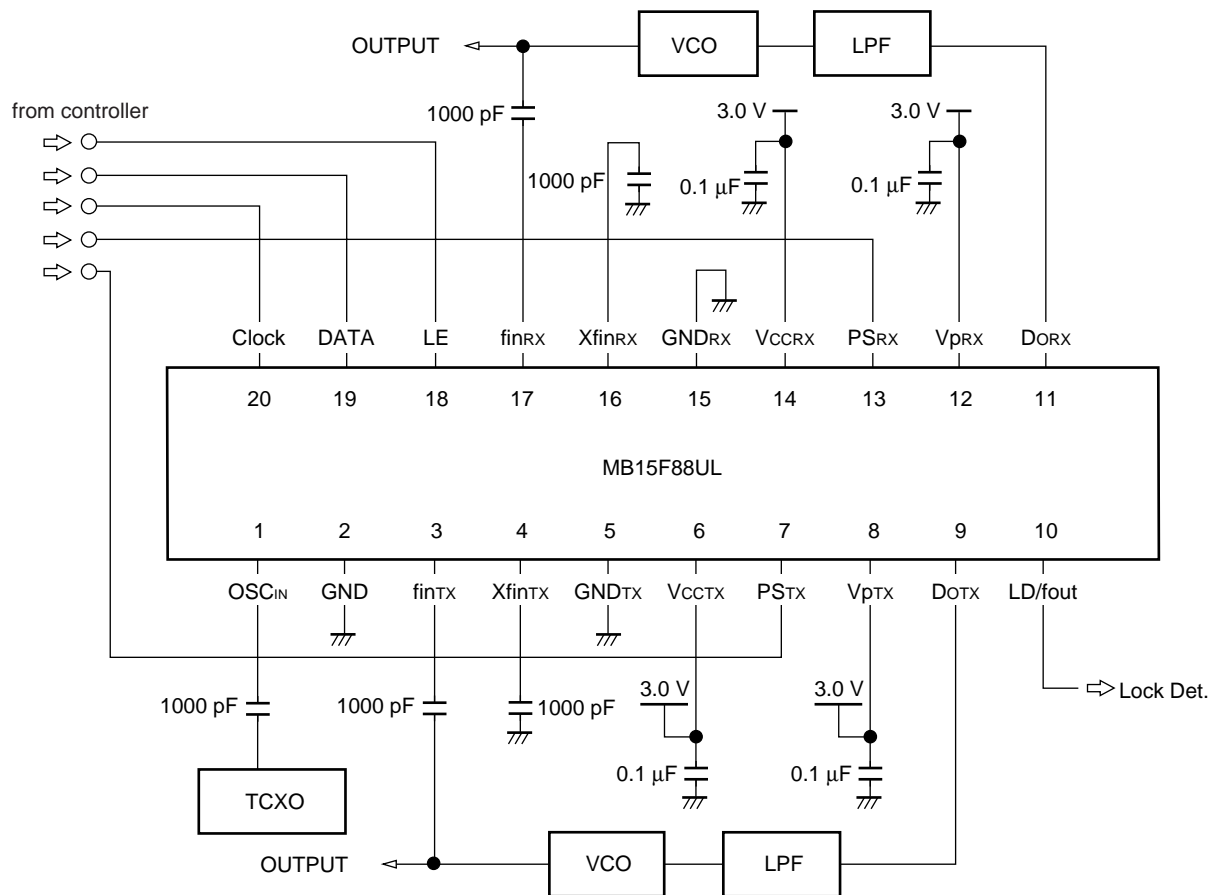


• PLL Lock Up time

2550 MHz \rightarrow 2490 MHz within ± 1 kHz
Hch \rightarrow Lch 133 μ s



APPLICATION EXAMPLE



- Notes :
- Clock, Data, LE : Schmit trigger circuit is provided (insert a pull-down or pull-up resistor to prevent oscillation when open-circuited in the input) .
 - TSSOP-20

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■ USAGE PRECAUTIONS

(1) $V_{CCR\text{X}}$, $V_{p\text{RX}}$, $V_{CCT\text{X}}$ and $V_{p\text{TX}}$ must be equal voltage.

Even if either RX-PLL or TX-PLL is not used, power must be supplied to $V_{CCR\text{X}}$, $V_{p\text{RX}}$, $V_{CCT\text{X}}$ and $V_{p\text{TX}}$ to keep them equal. It is recommended that the non-use PLL is controlled by power saving function.

(2) To protect against damage by electrostatic discharge, note the following handling precautions :

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

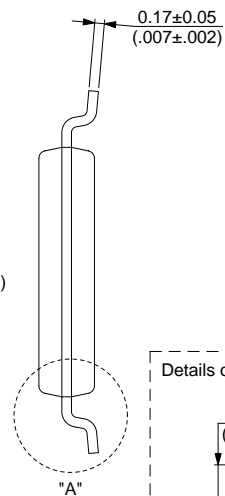
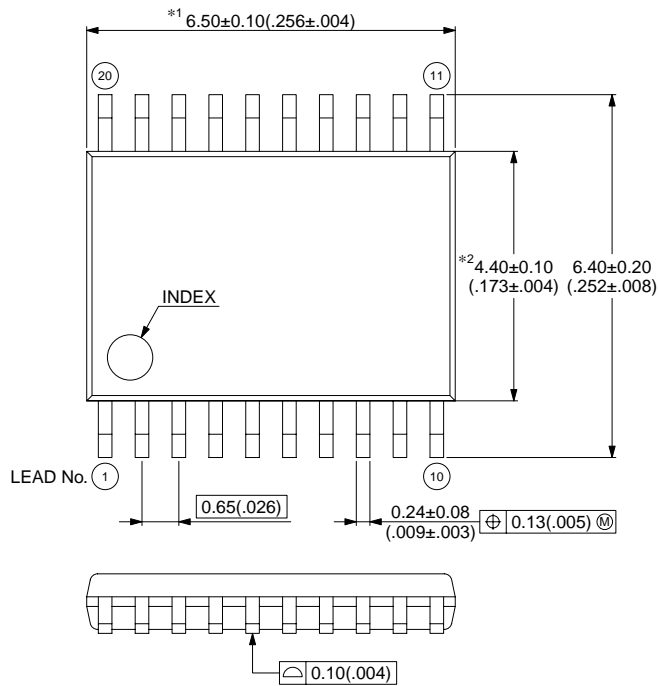
■ ORDERING INFORMATION

Part number	Package	Remarks
MB15F88ULPFT	20-pin plastic TSSOP (FPT-20P-M06)	
MB15F88ULPVA	20-pad plastic BCC (LCC-20P-M05)	

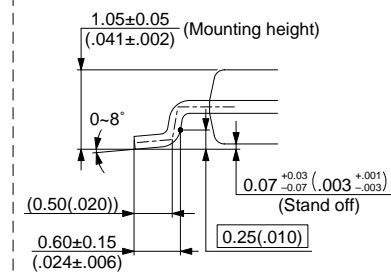
■ PACKAGE DIMENSIONS

20-pin plastic TSSOP
(FPT-20P-M06)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max) .
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Details of "A" part



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Dimensions in mm (inches)

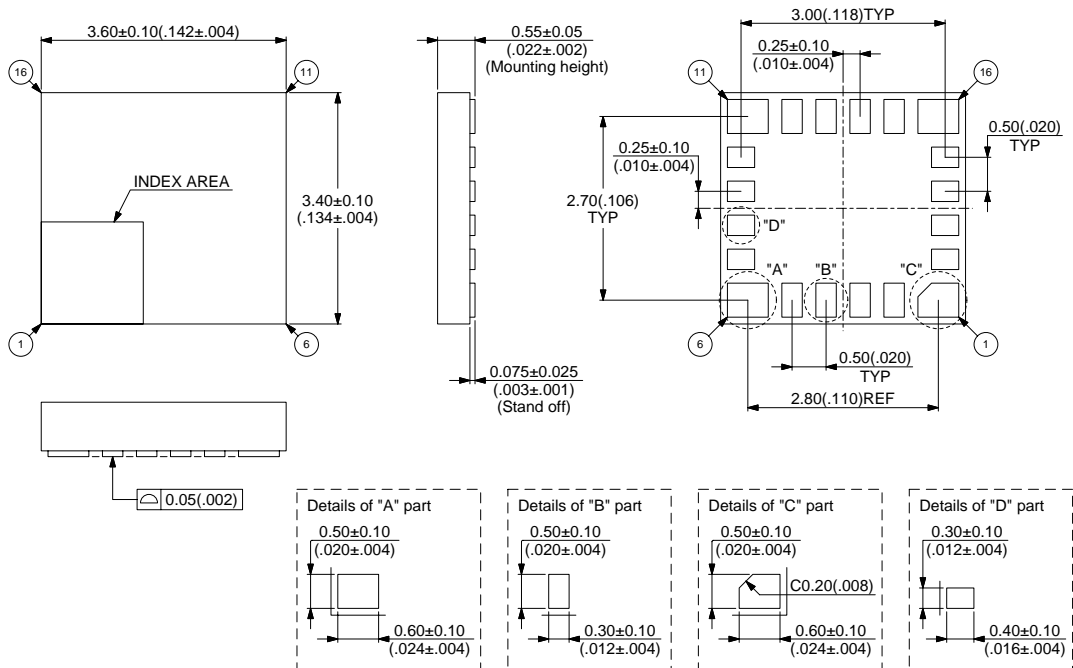
Note : The values in parentheses are reference values.

(Continued)

MB15F88UL

(Continued)

20-pad plastic BCC
(LCC-20P-M05)



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Dimensions in mm (inches)

Note : The values in parentheses are reference values.

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