

# PAGE MODE FLASH MEMORY

CMOS

## 96M (6M × 16) BIT

### MBM29QM96DF-65/80

#### ■ GENERAL DESCRIPTION

The MBM29QM96DF is 96M-bit, 3.0 V-only Page mode and dual operation Flash memory organized as 6M words by 16 bits. The device is offered in a 80-ball FBGA package. This device is designed to be programmed in-system with the standard system 3.0 V  $V_{CC}$  supply. 12.0 V  $V_{PP}$  and 5.0 V  $V_{CC}$  are not required for program or erase operations. The device can also be reprogrammed in standard EPROM programmers.

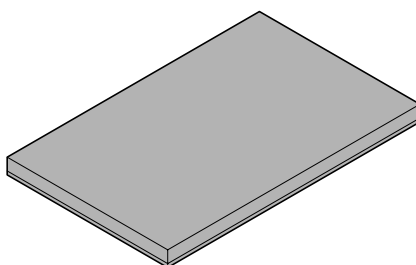
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#### ■ PRODUCT LINEUP

Part No.	MBM29QM96DF	
Ordering Part Number Suffix	65	80
$V_{CC}$ (V)	2.7 to 3.1	2.7 to 3.1
$V_{CCQ}$ (V)	$V_{CC}$	1.65 to $V_{CC}$
Max Random Address Access Time (ns)	65	80
Max Page Address Access Time (ns)	25	30
Max $\overline{CE}$ Access Time (ns)	65	80
Max $\overline{OE}$ Access Time (ns)	25	30

#### ■ PACKAGE

80-ball plastic FBGA



(BGA-80P-M03)

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The device provides truly high performance non-volatile Flash memory solution. The device offers fast page access times of 25 ns with random access times of 65 ns , allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ( $\overline{CE}$ ), write enable ( $\overline{WE}$ ), and output enable ( $\overline{OE}$ ) controls. The page size is 8 words.

The dual operation function provides simultaneous operation by dividing the memory space into four banks. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from the other bank with zero latency. This releases the system from waiting for the completion of program or erase operations.

The device is command set compatible with JEDEC standard E<sup>2</sup>PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the program and erase operations. Reading data out of the device is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The device is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm™ which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margins. Typically, each 32K words sector can be programmed and verified in about 0.3 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm™ which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margins.

Any individual sector is typically erased and verified in 0.5 second. (If already preprogrammed.)

The device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The device is erased when shipped from the factory.

The Enhanced V<sub>I/O</sub> (V<sub>CCQ</sub>) feature allows the output voltage generated on the device to be determined based on the V<sub>I/O</sub> level. This feature allows this device to operate in the 1.8 V I/O environment, driving and receiving signals to and from other 1.8 V devices on the same bus.

The device features single 3.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V<sub>CC</sub> detector automatically inhibits program and erase operations on the loss of power. The end of program or erase is detected by  $\overline{\text{Data}}$  Polling of DQ<sub>7</sub>, by the Toggle Bit feature on DQ<sub>6</sub>, output pin. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

Fujitsu's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability, and cost effectiveness. The device memory electrically erases all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The words are programmed one word at a time using the EPROM programming mechanism of hot electron injection.

## ■ FEATURES

- **0.17  $\mu$ m Process Technology**
- **Single 3.0 V Read, Program and Erase**  
Minimized system level power requirements
- **Simultaneous Read/Write (Program and Erase) Operations (Dual Bank)**
- **FlexBank™\*1**  
Bank A: 12 Mbit (4K words  $\times$  8 and 32K words  $\times$  23)  
Bank B: 36 Mbit (32K words  $\times$  72)  
Bank C: 36 Mbit (32K words  $\times$  72)  
Bank D: 12 Mbit (4K words  $\times$  8 and 32K words  $\times$  23)
- **Enhanced V<sub>IO</sub> (V<sub>CCQ</sub>) Feature**  
Input/Output voltage generated on the device is determined based on the V<sub>IO</sub> level
- **High Performance Page Mode**  
25 ns maximum page access time (65 ns random access time)
- **8 Words Page Size**
- **Compatible with JEDEC-Standard Commands**  
Uses same software commands as E<sup>2</sup>PROMs
- **Minimum 100,000 Program/Erase Cycles**
- **Sector Erase Architecture**  
Eight 4K words, a hundred ninety 32K words, eight 4K words sectors  
Any combination of sectors can be concurrently erased. Also supports full chip erase
- **Dual Boot Block**  
16 by 4K words bootblock sectors, 8 at the top of the address range and 8 at the bottom of the address range
- **HiddenROM Region**  
256 byte of HiddenROM, accessible through a new “HiddenROM Enable” command sequence  
Factory serialized and protected to provide a secure electronic serial number (ESN)
- **WP/ACC Input Pin**  
At V<sub>IL</sub>, allows protection of “outermost” 2  $\times$  4K words on both ends of boot sectors, regardless of sector protection/unprotection status  
At V<sub>IH</sub>, allows removal of boot sector protection  
At V<sub>ACC</sub>, increases program performance
- **Embedded Erase™\*2 Algorithms**  
Automatically preprograms and erases the chip or any sector
- **Embedded Program™\*2 Algorithms**  
Automatically programs and verifies data at specified address
- **Data Polling and Toggle Bit Feature for detection of program or erase cycle completion**
- **Ready/Busy Output (RY/BY)**  
Hardware method for detection of program or erase cycle completion
- **Automatic Sleep Mode**  
When addresses remain stable, the device automatically switches itself to low power mode.
- **Low V<sub>CC</sub> Write Inhibit  $\leq$  V<sub>LKO</sub>**
- **Program Suspend/Resume**  
Suspends the program operation to allow a read in another word
- **Erase Suspend/Resume**  
Suspends the erase operation to allow a read data and/or program in another sector within the same device

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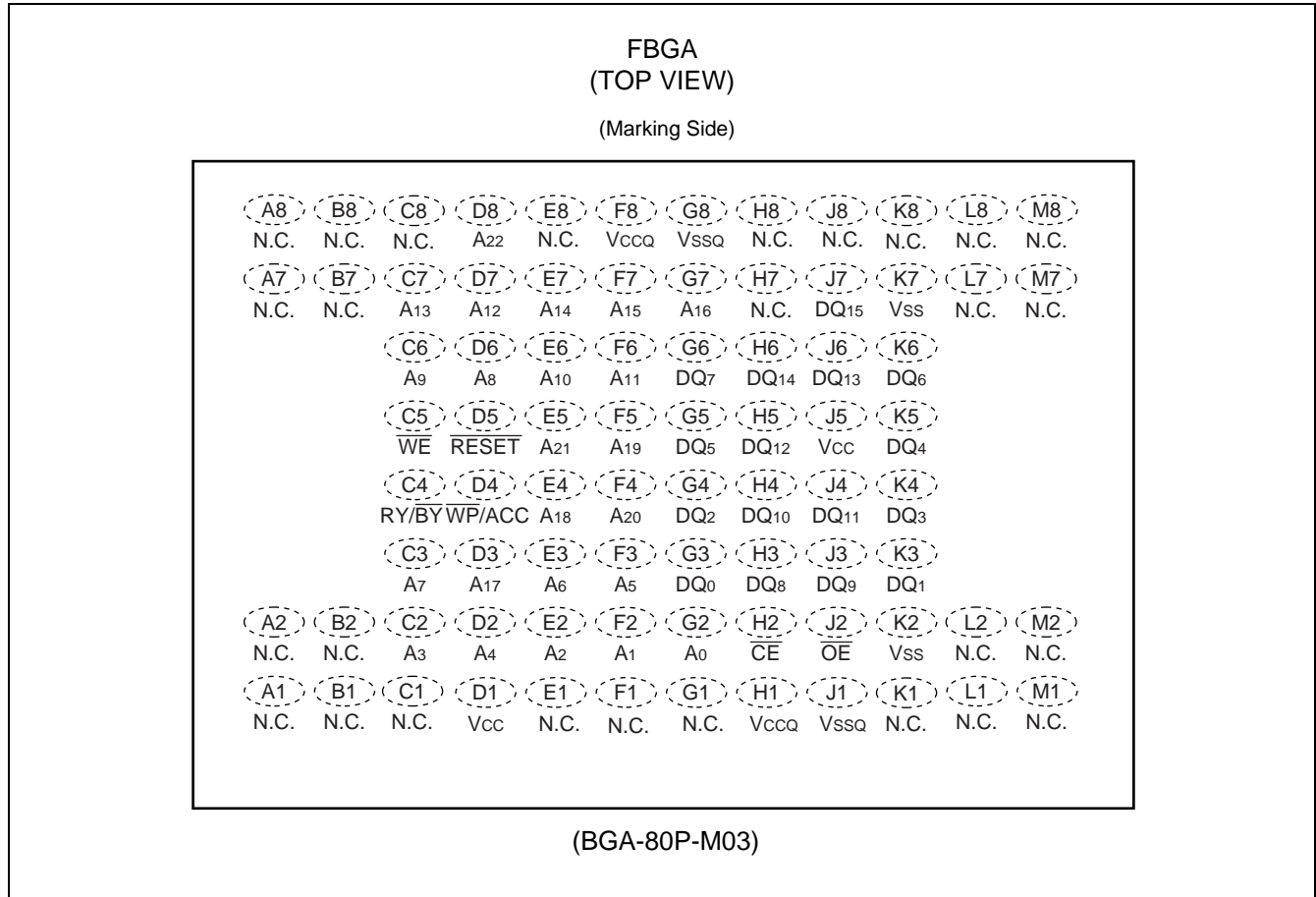
\*1 : FlexBank™ is a trademark of Fujitsu Limited.

\*2 : Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

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- In accordance with CFI (Common Elash Memory Interface)
- Hardware Reset Pin (RESET)  
Hardware method to reset the device for reading array data
- New Sector Protection
  - Persistent Sector Protection
  - Password Sector Protection

## PIN ASSIGNMENT

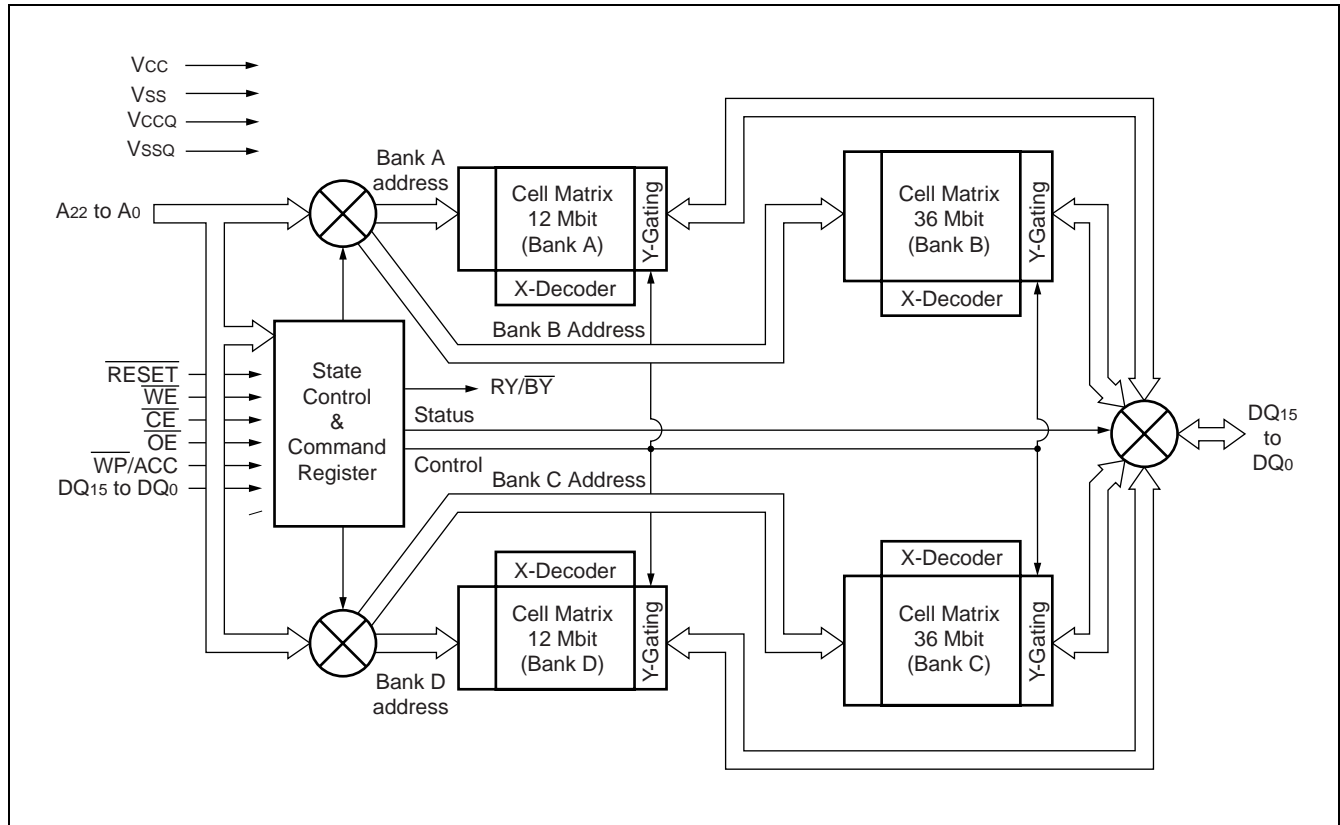


## PIN DESCRIPTIONS

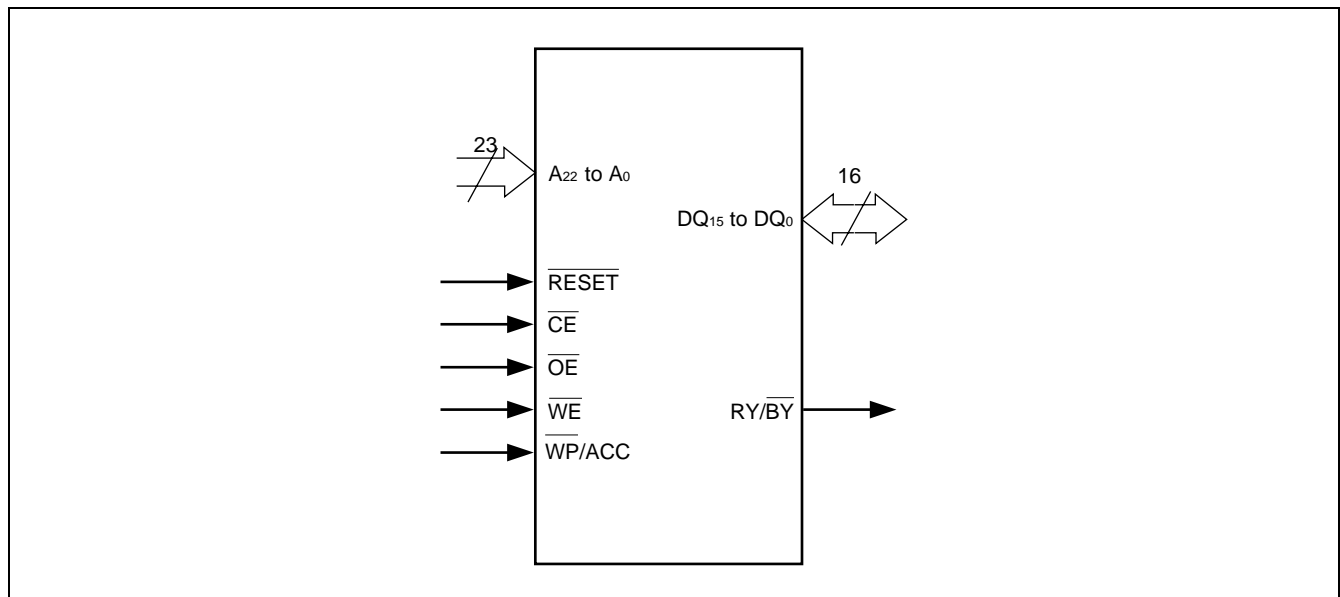
MBM29QM96DF Pin Configuration

Pin	Function
A22 to A0	Address Inputs
DQ15 to DQ0	Data Inputs/Outputs
CE	Chip Enable
OE	Output Enable
WE	Write Enable
RESET	Hardware Reset
WP/ACC	Hardware Write Protection/Program Acceleration
RY/BY	Ready/Busy Output
N.C.	Pin Not Connected Internally
Vss	Device Ground
Vcc	Device Power Supply
Vssq	Output Buffer Ground
Vccq	Output Buffer Power Supply

## ■ BLOCK DIAGRAM




## ■ LOGIC SYMBOL



## ■ DEVICE BUS OPERATION

MBM29QM96DF User Bus Operations Table

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{WP/ACC}$	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	A <sub>4</sub>	A <sub>5</sub>	A <sub>6</sub>	A <sub>9</sub>	DQ <sub>15</sub> to DQ <sub>0</sub>	$\overline{RESET}$
Autoselect Manufacturer Code *1	L	L	H	X	L	L	L	L	X	X	L	V <sub>ID</sub>	Code	H
Autoselect Device Code *1	L	L	H	X	H	L	L	L	X	X	L	V <sub>ID</sub>	Code	H
Extended Autoselect Device Code *1	L	L	H	X	L	H	H	H	X	X	L	V <sub>ID</sub>	Code	H
	L	L	H	X	H	H	H	H	X	X	L	V <sub>ID</sub>	Code	H
Read *3	L	L	H	X	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	A <sub>4</sub>	A <sub>5</sub>	A <sub>6</sub>	A <sub>9</sub>	D <sub>OUT</sub>	H
Standby	H	X	X	X	X	X	X	X	X	X	X	X	High-Z	H
Output Disable	L	H	H	X	X	X	X	X	X	X	X	X	High-Z	H
Write (Program/Erase)	L	H	L	X	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	A <sub>4</sub>	A <sub>5</sub>	A <sub>6</sub>	A <sub>9</sub>	D <sub>IN</sub>	H
Enable Sector Group Protection *2,*4	L	V <sub>ID</sub>		X	L	H	L	H	H	H	L	V <sub>ID</sub>	X	H
Verify Sector Group Protection *2, *4	L	L	H	H	L	H	L	H	H	H	L	V <sub>ID</sub>	Code	H
Boot Block Sector Write Protection *5	X	X	X	L	X	X	X	X	X	X	X	X	X	H
Temporary Sector Group Unprotection *6	X	X	X	H	X	X	X	X	X	X	X	X	X	V <sub>ID</sub>
Reset	X	X	X	X	X	X	X	X	X	X	X	X	High-Z	L

**Legend:** L = V<sub>IL</sub>, H = V<sub>IH</sub>, X = V<sub>IL</sub> or V<sub>IH</sub>,  = Pulse input. See "DC CHARACTERISTICS" for voltage levels.

\*1 : Manufacturer and device codes may also be accessed via a command register write sequence.  
See "MBM29QM96DF Command Definitions Table" in "■ DEVICE BUS OPERATION".

\*2 : Refer to section on "Sector Group Protection".

\*3 :  $\overline{WE}$  can be V<sub>IL</sub> if  $\overline{OE}$  is V<sub>IL</sub>,  $\overline{OE}$  at V<sub>IH</sub> initiates the program and erase operations.

\*4 : V<sub>CC</sub> = 2.7 V to 3.1 V.

\*5 : Protects "outermost" 2x 4K words on both end of the boot block sectors. (SA0, SA1, SA204, and SA205)

\*6 : Also used for "Extended Sector Group Protection".

MBM29QM96DF Command Definitions Table

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle		Seventh Bus Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset *1	2	XXXh	F0h	RA	RD	—	—	—	—	—	—	—	—	—	—
Read/Reset *1	4	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—	—	—
Autoselect	3	555h	AAh	2AAh	55h	(BA) 555h	90h	—	—	—	—	—	—	—	—
Program	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—	—	—
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h	—	—
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h	—	—
Program/Erase Suspend	1	BA	B0h	—	—	—	—	—	—	—	—	—	—	—	—
Program/Erase Resume	1	BA	30h	—	—	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—	—	—
Fast Program *2	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—	—	—
Reset from Fast Mode *2	2	BA	90h	XXXh	F0h *6	—	—	—	—	—	—	—	—	—	—
Extended Sector Group Protection*3	4	XXXh	60h	SGA	60h	SGA	40h	SGA	SD	—	—	—	—	—	—
Query *4	1	(BA) 55h	98h	—	—	—	—	—	—	—	—	—	—	—	—
HiddenROM Entry	3	555h	AAh	2AAh	55h	555h	88h	—	—	—	—	—	—	—	—
HiddenROM Program *5	4	555h	AAh	2AAh	55h	555h	A0h	(HRA) PA	PD	—	—	—	—	—	—
HiddenROM Exit *5	4	555h	AAh	2AAh	55h	(HR-BA) 555h	90h	XXXh	00h	—	—	—	—	—	—
HiddenROM Protect *5	6	555h	AAh	2AAh	55h	555h	60h	OPBP	68h	OPBP	48h	XXXh	RD (0)	—	—
Password Program *7	4	555h	AAh	2AAh	55h	555h	38h	XX0h	PD0	—	—	—	—	—	—
								XX1h	PD1	—	—	—	—	—	—
								XX2h	PD2	—	—	—	—	—	—
								XX3h	PD3	—	—	—	—	—	—
Password Unlock	7	555h	AAh	2AAh	55h	555h	28h	XX0h	PD0	XX1h	PD1	XX2h	PD2	XX3h	PD3
Password Verify	4	555h	AAh	2AAh	55h	555h	C8h	PWA	PWD	—	—	—	—	—	—

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Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle		Seventh Bus Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Password Mode Locking Bit Program	6	555h	AAh	2AAh	55h	555h	60h	PL	68h	PL	48h	XXh	RD (0)	—	—
Persistent Protection Mode Locking Bit Program	6	555h	AAh	2AAh	55h	555h	60h	SPML	68h	SPML	48h	XXh	RD (0)	—	—
PPB Program	6	555h	AAh	2AAh	55h	555h	60h	SA+ WP	68h	SA+ WP	48h	XXh	RD (0)	—	—
PPB Verify	4	555h	AAh	2AAh	55h	555h	90h	SA+ x02	RD (0)	—	—	—	—	—	—
All PPB Erase *8	6	555h	AAh	2AAh	55h	555h	60h	SA+ WP	60h	SA+ WP	40h	XXh	RD (0)	—	—
PPB Lock Bit Set	3	555h	AAh	2AAh	55h	555h	78h	—	—	—	—	—	—	—	—
PPB Lock Bit Verify	4	555h	AAh	2AAh	55h	555h	58h	SA	RD (1)	—	—	—	—	—	—
DPB Write	4	555h	AAh	2AAh	55h	555h	48h	SA	X1h	—	—	—	—	—	—
DPB Erase	4	555h	AAh	2AAh	55h	555h	48h	SA	X0h	—	—	—	—	—	—
DPB Verify	4	555h	AAh	2AAh	55h	555h	58h	SA	RD (0)	—	—	—	—	—	—

## Legend:

- RA = Address of the memory location to be read
- PA = Address of the memory location to be programmed  
Addresses are latched on the falling edge of the write pulse.
- SA = Address of the sector
- BA = Bank Address
- RD = Data read from location RA during read operation.
- PD = Data to be programmed at location PA. Data is latched on the rising edge of write pulse.
- SGA = Sector group address to be protected. Set sector group address and (A<sub>6</sub>, A<sub>5</sub>, A<sub>4</sub>, A<sub>3</sub>, A<sub>2</sub>, A<sub>1</sub>, A<sub>0</sub>) = (0, 1, 1, 1, 0, 1, 0)
- SD = Sector group protection verify data. Output 01h at protected sector group addresses and output 00h at unprotected sector group addresses.
- HRA = Address of the HiddenROM area (000000h to 00007Fh)
- HRBA = Bank Address of the HiddenROM area (A<sub>22</sub> = A<sub>21</sub> = A<sub>20</sub> = A<sub>19</sub> = A<sub>18</sub> = V<sub>IL</sub>)
- RD (0) = DQ<sub>0</sub> data, RD (1) = DQ<sub>1</sub> data. PPB Lock bit is read on DQ<sub>1</sub> and PPB or DPB are read on DQ<sub>0</sub>.  
If set, DQ<sub>0</sub>/DQ<sub>1</sub> = 1. If cleared, DQ<sub>0</sub>/DQ<sub>1</sub> = 0.
- OPBP = (A<sub>6</sub>, A<sub>5</sub>, A<sub>4</sub>, A<sub>3</sub>, A<sub>2</sub>, A<sub>1</sub>, A<sub>0</sub>) is (X, 0, 1, 1, 0, 1, 0)
- SLA = Address of the sector to be locked. Set sector address (SA) and either A<sub>6</sub> = 1 for unlocked or A<sub>6</sub> = 0 for locked
- PWA/PWD = Password Address/Password Data
- PL = (A<sub>6</sub>, A<sub>5</sub>, A<sub>4</sub>, A<sub>3</sub>, A<sub>2</sub>, A<sub>1</sub>, A<sub>0</sub>) is (X, 0, 0, 1, 0, 1, 0)
- SPML = (A<sub>6</sub>, A<sub>5</sub>, A<sub>4</sub>, A<sub>3</sub>, A<sub>2</sub>, A<sub>1</sub>, A<sub>0</sub>) is (X, 0, 1, 0, 0, 1, 0)
- WP = (A<sub>6</sub>, A<sub>5</sub>, A<sub>4</sub>, A<sub>3</sub>, A<sub>2</sub>, A<sub>1</sub>, A<sub>0</sub>) is (X, 1, 1, 1, 0, 1, 0)

- \*1 : Both of these reset commands are equivalent.
- \*2 : This command is valid during Fast Mode.
- \*3 : This command is valid while  $\overline{\text{RESET}} = V_{\text{ID}}$ .
- \*4 : The valid addresses are  $A_6$  to  $A_0$ .
- \*5 : This command is valid during HiddenROM mode.
- \*6 : The data "00h" is also acceptable.
- \*7 : Data before fourth cycle also need to be programmed repeating from first cycle to third cycle.
- \*8 : RD(0) of the sixth cycle shows PPB erase status. When RD(0) is "1", programming must be repeated from the beginning of first cycle to the fourth cycle; both fifth and the sixth validate full completion of erase.

Notes :

- Address bits  $A_{22}$  to  $A_{11} = X = \text{"H"}$  or  $\text{"L"}$  for all address commands except for PA, SA, BA, SGA, OPBP, SLA, PWA, PL, SPML, WP.
- Bus operations are defined in "MBM29QM96DF User Bus Operation Table" in "■ DEVICE BUS OPERATION".
- The system should generate the following address patterns:  
555h or 2AAh to addresses  $A_{10}$  to  $A_0$
- Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.
- Command combinations not described in Command Definitions table are illegal.

**MBM29QM96DF Autoselect Codes**

Type	A <sub>22</sub> to A <sub>12</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Code (HEX)
Manufacture's Code	BA* <sup>2</sup>	V <sub>IL</sub>	x	x	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	04h
Device Code	BA* <sup>2</sup>	V <sub>IL</sub>	x	x	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	227Eh
Extended Device Code* <sup>3</sup>	BA* <sup>2</sup>	V <sub>IL</sub>	x	x	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IL</sub>	2217h
	BA* <sup>2</sup>	V <sub>IL</sub>	x	x	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IH</sub>	2201h
Sector Group Protection* <sup>1</sup>	Sector Group Addresses	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	01h* <sup>1</sup>

\*1 : Sector Group can be protected by "Sector Group Protection", "Extended Sector Group Protection" and "New Sector Protection(PPB Protection)". Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

\*2 : When V<sub>ID</sub> is applied to A<sub>9</sub>, both Bank 1 and Bank 2 are put into Autoselect mode, which makes simultaneous operation unable to be executed. Consequently, specifying the bank address is not required. However, the bank address needs to be indicated when Autoselect mode is read out at command mode, because then it enables to activate simultaneous operation.

\*3 : A read cycle at address (BA) 01h outputs device code. When 227Eh is output, it indicates that two additional codes, called Extended Device Codes, will be required. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh, as well as at (BA) 0Fh

**Extended Auteselect Code Table**

Type	Code	DQ <sub>15</sub>	DQ <sub>14</sub>	DQ <sub>13</sub>	DQ <sub>12</sub>	DQ <sub>11</sub>	DQ <sub>10</sub>	DQ <sub>9</sub>	DQ <sub>8</sub>	DQ <sub>7</sub>	DQ <sub>6</sub>	DQ <sub>5</sub>	DQ <sub>4</sub>	DQ <sub>3</sub>	DQ <sub>2</sub>	DQ <sub>1</sub>	DQ <sub>0</sub>
Manufacturer's Code	04h	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	227Eh	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	0
Extended Device Code	2217h	0	0	1	0	0	0	1	0	0	0	0	1	0	1	1	1
	2201h	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	1
PPB Protection	01h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
PPB Unprotection	00h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

## ■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

Sector Address Table (Bank A)

Bank	Sector	Sector Address											Sector Size (Kwords)	Address Range
		Bank Address					A <sub>17</sub>	A <sub>16</sub>	A <sub>15</sub>	A <sub>14</sub>	A <sub>13</sub>	A <sub>12</sub>		
		A <sub>22</sub>	A <sub>21</sub>	A <sub>20</sub>	A <sub>19</sub>	A <sub>18</sub>								
Bank A	SA0	0	0	0	0	0	0	0	0	0	0	0	4	000000h to 000FFFh
	SA1	0	0	0	0	0	0	0	0	0	0	1	4	001000h to 001FFFh
	SA2	0	0	0	0	0	0	0	0	0	1	0	4	002000h to 002FFFh
	SA3	0	0	0	0	0	0	0	0	0	1	1	4	003000h to 003FFFh
	SA4	0	0	0	0	0	0	0	0	1	0	0	4	004000h to 004FFFh
	SA5	0	0	0	0	0	0	0	0	1	0	1	4	005000h to 005FFFh
	SA6	0	0	0	0	0	0	0	0	1	1	0	4	006000h to 006FFFh
	SA7	0	0	0	0	0	0	0	0	1	1	1	4	007000h to 007FFFh
	SA8	0	0	0	0	0	0	0	1	X	X	X	32	008000h to 00FFFFh
	SA9	0	0	0	0	0	0	1	0	X	X	X	32	010000h to 017FFFh
	SA10	0	0	0	0	0	0	1	1	X	X	X	32	018000h to 01FFFFh
	SA11	0	0	0	0	0	1	0	0	X	X	X	32	020000h to 027FFFh
	SA12	0	0	0	0	0	1	0	1	X	X	X	32	028000h to 02FFFFh
	SA13	0	0	0	0	0	1	1	0	X	X	X	32	030000h to 037FFFh
	SA14	0	0	0	0	0	1	1	1	X	X	X	32	038000h to 03FFFFh
	SA15	0	0	0	0	1	0	0	0	X	X	X	32	040000h to 047FFFh
	SA16	0	0	0	0	1	0	0	1	X	X	X	32	048000h to 04FFFFh
	SA17	0	0	0	0	1	0	1	0	X	X	X	32	050000h to 057FFFh
	SA18	0	0	0	0	1	0	1	1	X	X	X	32	058000h to 05FFFFh
	SA19	0	0	0	0	1	1	0	0	X	X	X	32	060000h to 067FFFh
	SA20	0	0	0	0	1	1	0	1	X	X	X	32	068000h to 06FFFFh
	SA21	0	0	0	0	1	1	1	0	X	X	X	32	070000h to 077FFFh
	SA22	0	0	0	0	1	1	1	1	X	X	X	32	078000h to 07FFFFh
	SA23	0	0	0	1	0	0	0	0	X	X	X	32	080000h to 087FFFh
	SA24	0	0	0	1	0	0	0	1	X	X	X	32	088000h to 08FFFFh
	SA25	0	0	0	1	0	0	1	0	X	X	X	32	090000h to 097FFFh
	SA26	0	0	0	1	0	0	1	1	X	X	X	32	098000h to 09FFFFh
	SA27	0	0	0	1	0	1	0	0	X	X	X	32	0A0000h to 0A7FFFh
	SA28	0	0	0	1	0	1	0	1	X	X	X	32	0A8000h to 0AFFFFh
	SA29	0	0	0	1	0	1	1	0	X	X	X	32	0B0000h to 0B7FFFh
	SA30	0	0	0	1	0	1	1	1	X	X	X	32	0B8000h to 0BFFFFh

**Sector Address Table (Bank B)**

Bank	Sector	Sector Address											Sector Size (Kwords)	Address Range
		Bank Address					A <sub>17</sub>	A <sub>16</sub>	A <sub>15</sub>	A <sub>14</sub>	A <sub>13</sub>	A <sub>12</sub>		
		A <sub>22</sub>	A <sub>21</sub>	A <sub>20</sub>	A <sub>19</sub>	A <sub>18</sub>								
Bank B	SA31	0	0	0	1	1	0	0	0	X	X	X	32	0C0000h to 0C7FFFh
	SA32	0	0	0	1	1	0	0	1	X	X	X	32	0C8000h to 0CFFFFh
	SA33	0	0	0	1	1	0	1	0	X	X	X	32	0D0000h to 0D7FFFh
	SA34	0	0	0	1	1	0	1	1	X	X	X	32	0D8000h to 0DFFFFh
	SA35	0	0	0	1	1	1	0	0	X	X	X	32	0E0000h to 0E7FFFh
	SA36	0	0	0	1	1	1	0	1	X	X	X	32	0E8000h to 0EFFFFh
	SA37	0	0	0	1	1	1	1	0	X	X	X	32	0F0000h to 0F7FFFh
	SA38	0	0	0	1	1	1	1	1	X	X	X	32	0F8000h to 0FFFFFFh
	SA39	0	0	1	0	0	0	0	0	X	X	X	32	100000h to 107FFFh
	SA40	0	0	1	0	0	0	0	1	X	X	X	32	108000h to 10FFFFh
	SA41	0	0	1	0	0	0	1	0	X	X	X	32	110000h to 117FFFh
	SA42	0	0	1	0	0	0	1	1	X	X	X	32	118000h to 11FFFFh
	SA43	0	0	1	0	0	1	0	0	X	X	X	32	120000h to 127FFFh
	SA44	0	0	1	0	0	1	0	1	X	X	X	32	128000h to 12FFFFh
	SA45	0	0	1	0	0	1	1	0	X	X	X	32	130000h to 137FFFh
	SA46	0	0	1	0	0	1	1	1	X	X	X	32	138000h to 13FFFFh
	SA47	0	0	1	0	1	0	0	0	X	X	X	32	140000h to 147FFFh
	SA48	0	0	1	0	1	0	0	1	X	X	X	32	148000h to 14FFFFh
	SA49	0	0	1	0	1	0	1	0	X	X	X	32	150000h to 157FFFh
	SA50	0	0	1	0	1	0	1	1	X	X	X	32	158000h to 15FFFFh
	SA51	0	0	1	0	1	1	0	0	X	X	X	32	160000h to 167FFFh
	SA52	0	0	1	0	1	1	0	1	X	X	X	32	168000h to 16FFFFh
	SA53	0	0	1	0	1	1	1	0	X	X	X	32	170000h to 177FFFh
	SA54	0	0	1	0	1	1	1	1	X	X	X	32	178000h to 17FFFFh
	SA55	0	0	1	1	0	0	0	0	X	X	X	32	180000h to 187FFFh
	SA56	0	0	1	1	0	0	0	1	X	X	X	32	188000h to 18FFFFh
	SA57	0	0	1	1	0	0	1	0	X	X	X	32	190000h to 197FFFh
	SA58	0	0	1	1	0	0	1	1	X	X	X	32	198000h to 19FFFFh
	SA59	0	0	1	1	0	1	0	0	X	X	X	32	1A0000h to 1A7FFFh
	SA60	0	0	1	1	0	1	0	1	X	X	X	32	1A8000h to 1AFFFFh
	SA61	0	0	1	1	0	1	1	0	X	X	X	32	1B0000h to 1B7FFFh
	SA62	0	0	1	1	0	1	1	1	X	X	X	32	1B8000h to 1BFFFFh
SA63	0	0	1	1	1	0	0	0	X	X	X	32	1C0000h to 1C7FFFh	
SA64	0	0	1	1	1	0	0	1	X	X	X	32	1C8000h to 1CFFFFh	
SA65	0	0	1	1	1	0	1	0	X	X	X	32	1D0000h to 1D7FFFh	
SA66	0	0	1	1	1	0	1	1	X	X	X	32	1D8000h to 1DFFFFh	
SA67	0	0	1	1	1	1	0	0	X	X	X	32	1E0000h to 1E7FFFh	
SA68	0	0	1	1	1	1	0	1	X	X	X	32	1E8000h to 1EFFFFh	
SA69	0	0	1	1	1	1	1	0	X	X	X	32	1F0000h to 1F7FFFh	
SA70	0	0	1	1	1	1	1	1	X	X	X	32	1F8000h to 1FFFFFFh	
SA71	0	1	0	0	0	0	0	0	X	X	X	32	200000h to 207FFFh	

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(Continued)

Bank	Sector	Sector Address											Sector Size (Kwords)	Address Range
		Bank Address					A <sub>17</sub>	A <sub>16</sub>	A <sub>15</sub>	A <sub>14</sub>	A <sub>13</sub>	A <sub>12</sub>		
		A <sub>22</sub>	A <sub>21</sub>	A <sub>20</sub>	A <sub>19</sub>	A <sub>18</sub>								
Bank B	SA72	0	1	0	0	0	0	0	1	X	X	X	32	208000h to 20FFFFh
	SA73	0	1	0	0	0	0	1	0	X	X	X	32	210000h to 217FFFh
	SA74	0	1	0	0	0	0	1	1	X	X	X	32	218000h to 21FFFFh
	SA75	0	1	0	0	0	1	0	0	X	X	X	32	220000h to 227FFFh
	SA76	0	1	0	0	0	1	0	1	X	X	X	32	228000h to 22FFFFh
	SA77	0	1	0	0	0	1	1	0	X	X	X	32	230000h to 237FFFh
	SA78	0	1	0	0	0	1	1	1	X	X	X	32	238000h to 23FFFFh
	SA79	0	1	0	0	1	0	0	0	X	X	X	32	240000h to 247FFFh
	SA80	0	1	0	0	1	0	0	1	X	X	X	32	248000h to 24FFFFh
	SA81	0	1	0	0	1	0	1	0	X	X	X	32	250000h to 257FFFh
	SA82	0	1	0	0	1	0	1	1	X	X	X	32	258000h to 25FFFFh
	SA83	0	1	0	0	1	1	0	0	X	X	X	32	260000h to 267FFFh
	SA84	0	1	0	0	1	1	0	1	X	X	X	32	268000h to 26FFFFh
	SA85	0	1	0	0	1	1	1	0	X	X	X	32	270000h to 277FFFh
	SA86	0	1	0	0	1	1	1	1	X	X	X	32	278000h to 27FFFFh
	SA87	0	1	0	1	0	0	0	0	X	X	X	32	280000h to 287FFFh
	SA88	0	1	0	1	0	0	0	1	X	X	X	32	288000h to 28FFFFh
	SA89	0	1	0	1	0	0	1	0	X	X	X	32	290000h to 297FFFh
	SA90	0	1	0	1	0	0	1	1	X	X	X	32	298000h to 29FFFFh
	SA91	0	1	0	1	0	1	0	0	X	X	X	32	2A0000h to 2A7FFFh
	SA92	0	1	0	1	0	1	0	1	X	X	X	32	2A8000h to 2AFFFFh
	SA93	0	1	0	1	0	1	1	0	X	X	X	32	2B0000h to 2B7FFFh
	SA94	0	1	0	1	0	1	1	1	X	X	X	32	2B8000h to 2BFFFFh
	SA95	0	1	0	1	1	0	0	0	X	X	X	32	2C0000h to 2C7FFFh
	SA96	0	1	0	1	1	0	0	1	X	X	X	32	2C8000h to 2CFFFFh
	SA97	0	1	0	1	1	0	1	0	X	X	X	32	2D0000h to 2D7FFFh
SA98	0	1	0	1	1	0	1	1	X	X	X	32	2D8000h to 2DFFFFh	
SA99	0	1	0	1	1	1	0	0	X	X	X	32	2E0000h to 2E7FFFh	
SA100	0	1	0	1	1	1	0	1	X	X	X	32	2E8000h to 2EFFFFh	
SA101	0	1	0	1	1	1	1	0	X	X	X	32	2F0000h to 2F7FFFh	
SA102	0	1	0	1	1	1	1	1	X	X	X	32	2F8000h to 2FFFFFh	

Sector Address Table (Bank C)

Bank	Sector	Sector Address											Sector Size (Kwords)	Address Range
		Bank Address					A <sub>17</sub>	A <sub>16</sub>	A <sub>15</sub>	A <sub>14</sub>	A <sub>13</sub>	A <sub>12</sub>		
		A <sub>22</sub>	A <sub>21</sub>	A <sub>20</sub>	A <sub>19</sub>	A <sub>18</sub>								
Bank C	SA103	0	1	1	0	0	0	0	0	X	X	X	32	300000h to 307FFFh
	SA104	0	1	1	0	0	0	0	1	X	X	X	32	308000h to 30FFFFh
	SA105	0	1	1	0	0	0	1	0	X	X	X	32	310000h to 317FFFh
	SA106	0	1	1	0	0	0	1	1	X	X	X	32	318000h to 31FFFFh
	SA107	0	1	1	0	0	1	0	0	X	X	X	32	320000h to 327FFFh
	SA108	0	1	1	0	0	1	0	1	X	X	X	32	328000h to 32FFFFh
	SA109	0	1	1	0	0	1	1	0	X	X	X	32	330000h to 337FFFh
	SA110	0	1	1	0	0	1	1	1	X	X	X	32	338000h to 33FFFFh
	SA111	0	1	1	0	1	0	0	0	X	X	X	32	340000h to 347FFFh
	SA112	0	1	1	0	1	0	0	1	X	X	X	32	348000h to 34FFFFh
	SA113	0	1	1	0	1	0	1	0	X	X	X	32	350000h to 357FFFh
	SA114	0	1	1	0	1	0	1	1	X	X	X	32	358000h to 35FFFFh
	SA115	0	1	1	0	1	1	0	0	X	X	X	32	360000h to 367FFFh
	SA116	0	1	1	0	1	1	0	1	X	X	X	32	368000h to 36FFFFh
	SA117	0	1	1	0	1	1	1	0	X	X	X	32	370000h to 377FFFh
	SA118	0	1	1	0	1	1	1	1	X	X	X	32	378000h to 37FFFFh
	SA119	0	1	1	1	0	0	0	0	X	X	X	32	380000h to 387FFFh
	SA120	0	1	1	1	0	0	0	1	X	X	X	32	388000h to 38FFFFh
	SA121	0	1	1	1	0	0	1	0	X	X	X	32	390000h to 397FFFh
	SA122	0	1	1	1	0	0	1	1	X	X	X	32	398000h to 39FFFFh
	SA123	0	1	1	1	0	1	0	0	X	X	X	32	3A0000h to 3A7FFFh
	SA124	0	1	1	1	0	1	0	1	X	X	X	32	3A8000h to 3AFFFFh
	SA125	0	1	1	1	0	1	1	0	X	X	X	32	3B0000h to 3B7FFFh
	SA126	0	1	1	1	0	1	1	1	X	X	X	32	3B8000h to 3BFFFFh
	SA127	0	1	1	1	1	0	0	0	X	X	X	32	3C0000h to 3C7FFFh
	SA128	0	1	1	1	1	0	0	1	X	X	X	32	3C8000h to 3CFFFFh
	SA129	0	1	1	1	1	0	1	0	X	X	X	32	3D0000h to 3D7FFFh
	SA130	0	1	1	1	1	0	1	1	X	X	X	32	3D8000h to 3DFFFFh
	SA131	0	1	1	1	1	1	0	0	X	X	X	32	3E0000h to 3E7FFFh
	SA132	0	1	1	1	1	1	0	1	X	X	X	32	3E8000h to 3EFFFFh
	SA133	0	1	1	1	1	1	1	0	X	X	X	32	3F0000h to 3F7FFFh
	SA134	0	1	1	1	1	1	1	1	X	X	X	32	3F8000h to 3FFFFFh
	SA135	1	0	0	0	0	0	0	0	X	X	X	32	400000h to 407FFFh
	SA136	1	0	0	0	0	0	0	1	X	X	X	32	408000h to 40FFFFh
	SA137	1	0	0	0	0	0	1	0	X	X	X	32	410000h to 417FFFh
	SA138	1	0	0	0	0	0	1	1	X	X	X	32	418000h to 41FFFFh
	SA139	1	0	0	0	0	1	0	0	X	X	X	32	420000h to 427FFFh
	SA140	1	0	0	0	0	1	0	1	X	X	X	32	428000h to 42FFFFh
	SA141	1	0	0	0	0	1	1	0	X	X	X	32	430000h to 437FFFh
	SA142	1	0	0	0	0	1	1	1	X	X	X	32	438000h to 43FFFFh
	SA143	1	0	0	0	1	0	0	0	X	X	X	32	440000h to 447FFFh

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Bank	Sector	Sector Address											Sector Size (Kwords)	Address Range
		Bank Address												
		A <sub>22</sub>	A <sub>21</sub>	A <sub>20</sub>	A <sub>19</sub>	A <sub>18</sub>								
Bank C	SA144	1	0	0	0	1	0	0	1	X	X	X	32	448000h to 44FFFFh
	SA145	1	0	0	0	1	0	1	0	X	X	X	32	450000h to 457FFFh
	SA146	1	0	0	0	1	0	1	1	X	X	X	32	458000h to 45FFFFh
	SA147	1	0	0	0	1	1	0	0	X	X	X	32	460000h to 467FFFh
	SA148	1	0	0	0	1	1	0	1	X	X	X	32	468000h to 46FFFFh
	SA149	1	0	0	0	1	1	1	0	X	X	X	32	470000h to 477FFFh
	SA150	1	0	0	0	1	1	1	1	X	X	X	32	478000h to 47FFFFh
	SA151	1	0	0	1	0	0	0	0	X	X	X	32	480000h to 487FFFh
	SA152	1	0	0	1	0	0	0	1	X	X	X	32	488000h to 48FFFFh
	SA153	1	0	0	1	0	0	1	0	X	X	X	32	490000h to 497FFFh
	SA154	1	0	0	1	0	0	1	1	X	X	X	32	498000h to 49FFFFh
	SA155	1	0	0	1	0	1	0	0	X	X	X	32	4A0000h to 4A7FFFh
	SA156	1	0	0	1	0	1	0	1	X	X	X	32	4A8000h to 4AFFFFh
	SA157	1	0	0	1	0	1	1	0	X	X	X	32	4B0000h to 4B7FFFh
	SA158	1	0	0	1	0	1	1	1	X	X	X	32	4B8000h to 4BFFFFh
	SA159	1	0	0	1	1	0	0	0	X	X	X	32	4C0000h to 4C7FFFh
	SA160	1	0	0	1	1	0	0	1	X	X	X	32	4C8000h to 4CFFFFh
	SA161	1	0	0	1	1	0	1	0	X	X	X	32	4D0000h to 4D7FFFh
	SA162	1	0	0	1	1	0	1	1	X	X	X	32	4D8000h to 4DFFFFh
	SA163	1	0	0	1	1	1	0	0	X	X	X	32	4E0000h to 4E7FFFh
	SA164	1	0	0	1	1	1	0	1	X	X	X	32	4E8000h to 4EFFFFh
	SA165	1	0	0	1	1	1	1	0	X	X	X	32	4F0000h to 4F7FFFh
	SA166	1	0	0	1	1	1	1	1	X	X	X	32	4F8000h to 4FFFFFh
	SA167	1	0	1	0	0	0	0	0	X	X	X	32	500000h to 507FFFh
	SA168	1	0	1	0	0	0	0	1	X	X	X	32	508000h to 50FFFFh
	SA169	1	0	1	0	0	0	1	0	X	X	X	32	510000h to 517FFFh
	SA170	1	0	1	0	0	0	1	1	X	X	X	32	518000h to 51FFFFh
	SA171	1	0	1	0	0	1	0	0	X	X	X	32	520000h to 527FFFh
	SA172	1	0	1	0	0	1	0	1	X	X	X	32	528000h to 52FFFFh
	SA173	1	0	1	0	0	1	1	0	X	X	X	32	530000h to 537FFFh
	SA174	1	0	1	0	0	1	1	1	X	X	X	32	538000h to 53FFFFh



Sector Address Table (Bank D)

Bank	Sector	Sector Address											Sector Size (Kwords)	Address Range
		Bank Address					A <sub>17</sub>	A <sub>16</sub>	A <sub>15</sub>	A <sub>14</sub>	A <sub>13</sub>	A <sub>12</sub>		
		A <sub>22</sub>	A <sub>21</sub>	A <sub>20</sub>	A <sub>19</sub>	A <sub>18</sub>								
Bank D	SA175	1	0	1	0	1	0	0	0	X	X	X	32	540000h to 547FFFh
	SA176	1	0	1	0	1	0	0	1	X	X	X	32	548000h to 54FFFFh
	SA177	1	0	1	0	1	0	1	0	X	X	X	32	550000h to 557FFFh
	SA178	1	0	1	0	1	0	1	1	X	X	X	32	558000h to 55FFFFh
	SA179	1	0	1	0	1	1	0	0	X	X	X	32	560000h to 567FFFh
	SA180	1	0	1	0	1	1	0	1	X	X	X	32	568000h to 56FFFFh
	SA181	1	0	1	0	1	1	1	0	X	X	X	32	570000h to 577FFFh
	SA182	1	0	1	0	1	1	1	1	X	X	X	32	578000h to 57FFFFh
	SA183	1	0	1	1	0	0	0	0	X	X	X	32	580000h to 587FFFh
	SA184	1	0	1	1	0	0	0	1	X	X	X	32	588000h to 58FFFFh
	SA185	1	0	1	1	0	0	1	0	X	X	X	32	590000h to 597FFFh
	SA186	1	0	1	1	0	0	1	1	X	X	X	32	598000h to 59FFFFh
	SA187	1	0	1	1	0	1	0	0	X	X	X	32	5A0000h to 5A7FFFh
	SA188	1	0	1	1	0	1	0	1	X	X	X	32	5A8000h to 5AFFFFh
	SA189	1	0	1	1	0	1	1	0	X	X	X	32	5B0000h to 5B7FFFh
	SA190	1	0	1	1	0	1	1	1	X	X	X	32	5B8000h to 5BFFFFh
	SA191	1	0	1	1	1	0	0	0	X	X	X	32	5C0000h to 5C7FFFh
	SA192	1	0	1	1	1	0	0	1	X	X	X	32	5C8000h to 5CFFFFh
	SA193	1	0	1	1	1	0	1	0	X	X	X	32	6D0000h to 5D7FFFh
	SA194	1	0	1	1	1	0	1	1	X	X	X	32	6D8000h to 5DFFFFh
	SA195	1	0	1	1	1	1	0	0	X	X	X	32	5E0000h to 5E7FFFh
	SA196	1	0	1	1	1	1	0	1	X	X	X	32	5E8000h to 5EFFFFh
	SA197	1	0	1	1	1	1	1	0	X	X	X	32	5F0000h to 5F7FFFh
	SA198	1	0	1	1	1	1	1	1	0	0	0	4	5F8000h to 5F8FFFh
	SA199	1	0	1	1	1	1	1	1	0	0	1	4	5F9000h to 5F9FFFh
SA200	1	0	1	1	1	1	1	1	0	1	0	4	5FA000h to 5FAFFFh	
SA201	1	0	1	1	1	1	1	1	0	1	1	4	5FB000h to 5FBFFFh	
SA202	1	0	1	1	1	1	1	1	1	0	0	4	5FC000h to 5FCFFFh	
SA203	1	0	1	1	1	1	1	1	1	0	1	4	5FD000h to 5FDFFFh	
SA204	1	0	1	1	1	1	1	1	1	1	0	4	5FE000h to 5FEFFFh	
SA205	1	0	1	1	1	1	1	1	1	1	1	4	5FF000h to 5FFFFFh	

**Sector Group Address Table**

Sector Group	A <sub>22</sub>	A <sub>21</sub>	A <sub>20</sub>	A <sub>19</sub>	A <sub>18</sub>	A <sub>17</sub>	A <sub>16</sub>	A <sub>15</sub>	A <sub>14</sub>	A <sub>13</sub>	A <sub>12</sub>	Sectors
SGA0	0	0	0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	0	0	0	1	X	X	X	SA8 to SA10
							1	0				
							1	1				
SGA9	0	0	0	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	0	0	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	0	0	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	0	0	0	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	0	0	0	1	0	1	X	X	X	X	X	SA27 to SA30
SGA14	0	0	0	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	0	0	0	1	1	1	X	X	X	X	X	SA35 to SA38
SGA16	0	0	1	0	0	0	X	X	X	X	X	SA39 to SA42
SGA17	0	0	1	0	0	1	X	X	X	X	X	SA43 to SA46
SGA18	0	0	1	0	1	0	X	X	X	X	X	SA47 to SA50
SGA19	0	0	1	0	1	1	X	X	X	X	X	SA51 to SA54
SGA20	0	0	1	1	0	0	X	X	X	X	X	SA55 to SA58
SGA21	0	0	1	1	0	1	X	X	X	X	X	SA59 to SA62
SGA22	0	0	1	1	1	0	X	X	X	X	X	SA63 to SA66
SGA23	0	0	1	1	1	1	X	X	X	X	X	SA67 to SA70
SGA24	0	1	0	0	0	0	X	X	X	X	X	SA71 to SA74
SGA25	0	1	0	0	0	1	X	X	X	X	X	SA75 to SA78
SGA26	0	1	0	0	1	0	X	X	X	X	X	SA79 to SA82
SGA27	0	1	0	0	1	1	X	X	X	X	X	SA83 to SA86
SGA28	0	1	0	1	0	0	X	X	X	X	X	SA87 to SA90
SGA29	0	1	0	1	0	1	X	X	X	X	X	SA91 to SA94
SGA30	0	1	0	1	1	0	X	X	X	X	X	SA95 to SA98
SGA31	0	1	0	1	1	1	X	X	X	X	X	SA99 to SA102
SGA32	0	1	1	0	0	0	X	X	X	X	X	SA103 to SA106

(Continued)

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Sector Group	A <sub>22</sub>	A <sub>21</sub>	A <sub>20</sub>	A <sub>19</sub>	A <sub>18</sub>	A <sub>17</sub>	A <sub>16</sub>	A <sub>15</sub>	A <sub>14</sub>	A <sub>13</sub>	A <sub>12</sub>	Sectors
SGA33	0	1	1	0	0	1	X	X	X	X	X	SA107 to SA110
SGA34	0	1	1	0	1	0	X	X	X	X	X	SA111 to SA114
SGA35	0	1	1	0	1	1	X	X	X	X	X	SA115 to SA118
SGA36	0	1	1	1	0	0	X	X	X	X	X	SA119 to SA122
SGA37	0	1	1	1	0	1	X	X	X	X	X	SA123 to SA126
SGA38	0	1	1	1	1	0	X	X	X	X	X	SA127 to SA130
SGA39	0	1	1	1	1	1	X	X	X	X	X	SA131 to SA134
SGA40	1	0	0	0	0	0	X	X	X	X	X	SA135 to SA138
SGA41	1	0	0	0	0	1	X	X	X	X	X	SA139 to SA142
SGA42	1	0	0	0	1	0	X	X	X	X	X	SA143 to SA146
SGA43	1	0	0	0	1	1	X	X	X	X	X	SA147 to SA150
SGA44	1	0	0	1	0	0	X	X	X	X	X	SA151 to SA154
SGA45	1	0	0	1	0	1	X	X	X	X	X	SA155 to SA158
SGA46	1	0	0	1	1	0	X	X	X	X	X	SA159 to SA162
SGA47	1	0	0	1	1	1	X	X	X	X	X	SA163 to SA166
SGA48	1	0	1	0	0	0	X	X	X	X	X	SA167 to SA170
SGA49	1	0	1	0	0	1	X	X	X	X	X	SA171 to SA174
SGA50	1	0	1	0	1	0	X	X	X	X	X	SA175 to SA178
SGA51	1	0	1	0	1	1	X	X	X	X	X	SA179 to SA182
SGA52	1	0	1	1	0	0	X	X	X	X	X	SA183 to SA186
SGA53	1	0	1	1	0	1	X	X	X	X	X	SA187 to SA190
SGA54	1	0	1	1	1	0	X	X	X	X	X	SA191 to SA194
SGA55	1	0	1	1	1	1	0	0	X	X	X	SA195 to SA197
							0	1				
							1	0				
SGA56	1	0	1	1	1	1	1	1	0	0	0	SA198
SGA57	1	0	1	1	1	1	1	1	0	0	1	SA199
SGA58	1	0	1	1	1	1	1	1	0	1	0	SA200
SGA59	1	0	1	1	1	1	1	1	0	1	1	SA201
SGA60	1	0	1	1	1	1	1	1	1	0	0	SA202
SGA61	1	0	1	1	1	1	1	1	1	0	1	SA203
SGA62	1	0	1	1	1	1	1	1	1	1	0	SA204
SGA63	1	0	1	1	1	1	1	1	1	1	1	SA205

**Common Flash Memory Interface Code Table**

Description	A <sub>6</sub> to A <sub>0</sub>	DQ <sub>15</sub> to DQ <sub>0</sub>
Query-unique ASCII string "QRY"	10h 11h 12h	0051h 0052h 0059h
Primary OEM Command Set 02h: AMD/FJ standard type	13h 14h	0002h 0000h
Address for Primary Extended Table	15h 16h	0040h 0000h
Alternate OEM Command Set (00h = not applicable)	17h 18h	0000h 0000h
Address for Alternate OEM Extended Table	19h 1Ah	0000h 0000h
V <sub>CC</sub> Min (write/erase) DQ <sub>7</sub> to DQ <sub>4</sub> : 1V, DQ <sub>3</sub> to DQ <sub>0</sub> : 100 mV	1Bh	0027h
V <sub>CC</sub> Max (write/erase) DQ <sub>7</sub> to DQ <sub>4</sub> : 1V, DQ <sub>3</sub> to DQ <sub>0</sub> : 100 mV	1Ch	0031h
V <sub>PP</sub> Min voltage	1Dh	0000h
V <sub>PP</sub> Max voltage	1Eh	0000h
Typical timeout per single byte/word write 2 <sup>N</sup> μs	1Fh	0004h
Typical timeout for Min size buffer write 2 <sup>N</sup> μs	20h	0000h
Typical timeout per individual block erase 2 <sup>N</sup> ms	21h	0009h
Typical timeout for full chip erase 2 <sup>N</sup> ms	22h	0000h
Max timeout for byte/word write 2 <sup>N</sup> times typical μs	23h	0005h
Max timeout for buffer write 2 <sup>N</sup> times typical μs	24h	0000h
Max timeout per individual block erase 2 <sup>N</sup> times typical ms	25h	0004h
Max timeout for full chip erase 2 <sup>N</sup> times typical ms	26h	0000h
Device Size = 2 <sup>N</sup> byte	27h	0018h
Flash Device Interface description 01h: x16	28h 29h	0001h 0000h
Max number of byte in multi-byte write = 2 <sup>N</sup>	2Ah 2Bh	0000h 0000h
Number of Erase Block Regions within device	2Ch	0003h
Erase Block Region 1 Information	2Dh 2Eh 2Fh 30h	0007h 0000h 0020h 0000h
Erase Block Region 2 Information	31h 32h 33h 34h	00BDh 0000h 0000h 0001h
Erase Block Region 3 Information	35h 36h 37h 38h	00BDh 0000h 0020h 0000h
Erase Block Region 4 Information	39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h

(Continued)

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Description	A <sub>6</sub> to A <sub>0</sub>	DQ <sub>15</sub> to DQ <sub>0</sub>
Query-unique ASCII string "PRI"	40h 41h 42h	0050h 0052h 0049h
Major version number, ASCII	43h	0031h
Minor version number, ASCII	44h	0033h
Address Sensitive Unlock 04h = Required and 0.17μm technology	45h	0004h
Erase Suspend 02h = To Read & Write	46h	0002h
Sector Protection 00h = Not Supported X = Number of sectors in per group	47h	0001h
Sector Temporary Unprotection 01h = Supported	48h	0001h
Sector Protection Algorithm	49h	0007h
Simultaneous Operation 00h = Not Supported, X = Total number of sectors in all Banks except Bank A	4Ah	00AFh
Burst Mode Type 00h = Not Supported	4Bh	0000h
Page Mode Type 02h = 8 Word Page	4Ch	0002h
V <sub>ACC</sub> (Acceleration) Supply Minimum 00h = Not Supported DQ <sub>7</sub> to DQ <sub>4</sub> : 1V, DQ <sub>3</sub> to DQ <sub>0</sub> : 100 mV	4Dh	0085h
V <sub>ACC</sub> (Acceleration) Supply Maximum 00h = Not Supported DQ <sub>7</sub> to DQ <sub>4</sub> : 1V, DQ <sub>3</sub> to DQ <sub>0</sub> : 100 mV	4Eh	0095h
Boot Type	4Fh	0001h
Program Suspend 01h = Supported	50h	0001h
Bank Organization X = Number of Banks	57h	0004h
Bank A Region Information	58h	001Fh
Bank B Region Information	59h	0048h
Bank C Region Information	5Ah	0048h
Bank D Region Information	5Bh	001Fh

## ■ FUNCTIONAL DESCRIPTION

### Simultaneous Operation

The device features functions that enable data reading from one memory bank while a program or erase operation is in progress in the other memory bank (simultaneous operation) , in addition to conventional features (read, program, erase, erase-suspend read, and erase-suspend program) . The bank is selected by bank address (  $A_{22}$ ,  $A_{21}$ ,  $A_{20}$ ,  $A_{19}$ ,  $A_{18}$  ) with zero latency. The device consists of the following four banks :

Bank A :  $8 \times 4KW$  and  $23 \times 32KW$ ; Bank B :  $72 \times 32 KW$ ; Bank C :  $72 \times 32KW$ ; Bank D :  $8 \times 4KW$  and  $23 \times 32KW$ .

The device can execute simultaneous operations between Bank 1, a bank chosen from among the four banks, and Bank 2, a bank consisting of the three remaining banks. See “FlexBank™ Architecture Table” in “■ FUNCTIONAL DESCRIPTION” below. This is what we call “FlexBank”, for example the rest of banks B, C and D to let the system read while Bank A is in the process of program (or erase) operation. However the different types of operations for the three banks are not allowed, e.g. Bank A programming, Bank B erasing, and Bank C reading out. With this “FlexBank”, as described in “Example of Virtual Banks Combination Table” in “■ FUNCTIONAL DESCRIPTION”, the system gets to select from four combinations of data volume for Bank 1 and Bank 2, which works well to meet the system requirement. The simultaneous operation cannot execute multi-function mode in the same bank. Refer to “Bank-to-Bank Read/Write(Program and Erase) Timing Diagram” in “■ TIMING DIAGRAM”.

**FlexBank™ Architecture**

Bank Splits	Bank 1		Bank 2	
	Bank Size	Combination	Bank Size	Combination
1	12 Mbit	Bank A	84 Mbit	Bank B, C, D
2	36 Mbit	Bank B	60 Mbit	Bank A, C, D
3	36 Mbit	Bank C	60 Mbit	Bank A, B, D
4	12 Mbit	Bank D	84 Mbit	Bank A, B, C

**Example of Virtual Banks Combination**

Bank Splits	Bank 1			Bank 2		
	Bank Size	Combination of Memory Bank	Sector Sizes	Bank Size	Combination of Memory Bank	Sector Sizes
1	12 Mbit	Bank A	Eight 4K words, Twenty-three 32K words	84 Mbit	Bank B + Bank C + Bank D	Eight 4K words, One hundred sixty-seven 32K words
2	24 Mbit	Bank A +Bank D	Sixteen 4K words, Forty-six 32K words	72 Mbit	Bank B + Bank C	One hundred forty-four 32K words
3	36 Mbit	Bank B	Seventy-two 32K words	60 Mbit	Bank A + Bank C + Bank D	Sixteen 4K words, One hundred eighteen 32K words
4	48 Mbit	Bank A + Bank B	Eight 4K words, Ninety-five 32Kwords	48 Mbit	Bank C + Bank D	Eight 4K words, Ninety-five 32Kwords

Note : When multiple sector erase over several banks is operated, the system cannot read out of the bank to which a sector being erased belongs. For example, suppose that erasing is taking place at both Bank A and Bank B, neither Bank A nor Bank B is read out they output the sequence flag once they are selected.

Meanwhile the system would get to read from either Bank C or Bank D.

## Simultaneous Operation

Case	Bank 1 Status	Bank 2 Status
1	Read mode	Read mode
2	Read mode	Autoselect mode
3	Read mode	Program mode
4	Read mode	Erase mode
5	Autoselect mode	Read mode
6	Program mode	Read mode
7	Erase mode	Read mode

Note : Bank 1 and Bank 2 are divided for the sake of convenience at Simultaneous Operation. The Bank consists of 4 banks, Bank A, Bank B, BankC and Bank D. Bank Address (BA) means to specify each of the Banks.

## Read Mode

The device has two control functions required to obtain data at the outputs.  $\overline{CE}$  is the power control and used for a device selection.  $\overline{OE}$  is the output control and used to gate data to the output pins if a device is selected.

Address access time ( $t_{ACC}$ ) is equal to the delay from stable addresses to valid output data. The chip enable access time ( $t_{CE}$ ) is the delay from stable addresses and stable  $\overline{CE}$  to valid data at the output pins. The output enable access time is the delay from the falling edge of  $\overline{OE}$  to valid data at the output pins. Assuming the addresses have been stable for at least  $t_{ACC} - t_{OE}$  time. When reading out a data without changing addresses after power-up, input hardware reset or to change  $\overline{CE}$  pin from "H" or "L".

## Page Mode Read

The device is capable of fast Page mode read and are compatible with the Page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The Page size of the device is 8 words, within the appropriate Page being selected by the higher address bits  $A_{22}$  to  $A_3$  and the LSB bits  $A_2$  to  $A_0$  determining the specific word within that page. This is an asynchronous operation with the microprocessor supplying the specific word location.

The random or initial page access is equal to  $t_{ACC}$  and subsequent Page read access (as long as the locations specified by the microprocessor fall within that Page) is equivalent to  $t_{PACC}$ . Here again,  $\overline{CE}$  selects the device and  $\overline{OE}$  is the output control and used to gate data to the output pins if the device is selected. Fast Page mode accesses are obtained by keeping  $A_{22}$  to  $A_3$  constant and changing  $A_2$  to  $A_0$  to select the specific word, within that page.

## Standby Mode

There are two ways to implement the standby mode on the device, one using both the  $\overline{CE}$  and  $\overline{RESET}$  pins, and the other via the  $\overline{RESET}$  pin only.

When using both pins, CMOS standby mode is achieved with  $\overline{CE}$  and  $\overline{RESET}$  input held at  $V_{CC} \pm 0.3$  V. Under this condition the current consumed is less than 5  $\mu$ A Max. During Embedded Algorithm operation,  $V_{CC}$  active current ( $I_{CC2}$ ) is required even when  $\overline{CE} = "H"$ . The device can be read with standard access time ( $t_{CE}$ ) from either of these standby modes.

When using the  $\overline{RESET}$  pin only, CMOS standby mode is achieved with  $\overline{RESET}$  input held at  $V_{SS} \pm 0.3$  V ( $\overline{CE} = "H"$  or "L"). Under this condition the current consumed is less than 5  $\mu$ A Max. Once the  $\overline{RESET}$  pin is set high, the device requires  $t_{RH}$  as a wake-up time for output to be valid for read access.

During standby mode, the output is in the high impedance state regardless of  $\overline{OE}$  input.

## Automatic Sleep Mode

Automatic sleep mode works to restrain power consumption during read-out of the device data. This is useful in the application such as a handy terminal which requires low power consumption.

To activate this mode, the device automatically switches itself to low power mode when addresses remain stable during access time of 150 ns. It is not necessary to control  $\overline{CE}$ ,  $\overline{WE}$ , and  $\overline{OE}$  on this mode. The current consumed is typically 1  $\mu$ A (CMOS Level).

During simultaneous operation,  $V_{CC}$  active current ( $I_{CC2}$ ) is required.

Since the data are latched during this mode, the data are continuously read out. When the addresses are changed, the mode is automatically canceled and the device reads the data for changed addresses.

## Output Disable

With the  $\overline{OE}$  input is at logic high level ( $V_{IH}$ ), output from the device is disabled. This causes the output pins to be in a high impedance state.

## Autoselect

Autoselect mode allows reading out of a binary code and identifies its manufacturer and type. It is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force  $V_{ID}$  on address pin  $A_9$ . Three identifier bytes may then be sequenced from the device outputs by toggling addresses. All addresses are DON'T CARES except  $A_6$ ,  $A_3$ ,  $A_2$ ,  $A_1$  and  $A_0$ . See "MBM29QM96DF User Bus Operation Table" in "■ DEVICE BUS OPERATION".

The manufacturer and device codes may also be read via the command register, for instances when the device is erased or programmed in a system without access to high voltage on the  $A_9$  pin. The command sequence is illustrated in "MBM29QM96DF Command Definitions Table" in "■ DEVICE BUS OPERATION".

In the command Autoselect mode, the bank addresses BA ( $A_{22}$ ,  $A_{21}$ ,  $A_{20}$ ,  $A_{19}$ ,  $A_{18}$ ) must point to a specific bank during the third write bus cycle of the Autoselect command. Then the Autoselect data are read from that bank while array data can be read from the other bank.

A read cycle from address 00h returns the manufacturer's code (Fujitsu = 04h). A read cycle at address 01h outputs device code. When 227Eh is output, it indicates that two additional codes, called Extended Device Codes is required. Therefore the system may continue reading out these Extended Device Codes at addresses of 0Eh and 0Fh. Refer to "MBM29QM96DF Autoselect Codes Table" and "Extended Autoselect Codes Table" in "■ DEVICE BUS OPERATION".

In the case of applying  $V_{ID}$  on  $A_9$ , because both Bank 1 and Bank 2 enter Autoselect mode, simultaneous operation cannot be executed.

## Write

Device erase and programming are accomplished via the command register. The contents of the register serve as input to the internal state machine. The state machine output dictates the device function.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing  $\overline{WE}$  to  $V_{IL}$ , while  $\overline{CE}$  is at  $V_{IL}$  and  $\overline{OE}$  is at  $V_{IH}$ . Addresses are latched on the falling edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever starts later, while data is latched on the rising edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever starts first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

## Accelerated Program Operation

The device offers accelerated program operation which enables the programming in high speed. If the system asserts  $V_{ACC}$  to the  $\overline{WP}/ACC$  pin, the device automatically enters the acceleration mode and the time required for program operation will reduce to about 60%. This function is primarily intended to allow high speed program, so caution is needed as the sector group becomes temporarily unprotected.



The system uses fast program command sequence when programming during acceleration mode. Set command to fast mode and reset command from fast mode are not necessary. When the device enters the acceleration mode, the device automatically set to fast mode. Therefore the present sequence is used for programming and detection of completion during acceleration mode.

Removing  $V_{ACC}$  from the  $\overline{WP}/ACC$  pin returns the device to normal operation. Do not remove  $V_{ACC}$  from  $\overline{WP}/ACC$  pin while programming. See “Accelerated Program Timing Diagram” in “■ TIMING DIAGRAM”.

### HiddenROM Region

Unlike previous flash memory devices, the MBM29QM96DF allows simultaneous operation while the HiddenROM is enabled. However, there are a number of restrictions associated with simultaneous operation and device operation when the HiddenROM is enabled:

- (1) The HiddenROM is not available for reading while the Password Unlock, any PPB program/erase operation, or Password programming are in progress. Reading to any location in the Bank D will return the status of these operations until these operations have completed execution.
- (2) Writing the corresponding Sector Protect latch associated with the overlaid bootblock sector results in the Sector Protect latch NOT being updated. This is only accomplished when the HiddenROM is not enabled.
- (3) Reading the corresponding DPB associated with the overlaid bootblock sector results in reading invalid data when the PPB Lock/DPB Verify command is issued. This function is only accomplished when the HiddenROM is not enabled.
- (4) All commands are available for execution when the HiddenROM is enabled except the following list. Issuing the following commands while the HiddenROM is enabled results in the command being ignored.
  - CFI
  - Set to Fast Mode
  - Fast Program
  - Reset from Fast Mode
  - Program and Sector Erase Suspend
  - Program and Sector Erase Resume
- (5) Executing the Sector Erase command is permitted when the HiddenROM is enabled, however, there is no provision for erasing the HiddenROM with the Sector Erase command, regardless of the protection status. The Sector Erase command will erase all other sectors when the HiddenROM is enabled. Erasing the HiddenROM with the Embedded Algorithm is accomplished by issuing the Chip Erase command. If the HiddenROM is the only sector requiring erasure, set the Sector Protect latches for the remaining sectors prior to issuing the Chip Erase command.
- (6) Executing the HiddenROM Entry command during program or erase suspend mode is allowed. Since the Sector Erase/Program Resume command is disabled while the HiddenROM is enabled, the user cannot resume programming or erase of the HiddenROM in place of the overlaid bootblock sector.

### HiddenROM Protection Bit

The HiddenROM Protection Bit prevents programming of the HiddenROM memory area. Once set, the HiddenROM memory area contents are non-modifiable.

### <Protection>

The MBM29QM96DF features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups:

#### (1) Write Protect ( $\overline{WP}/ACC$ )[Hardware Protection]

The device features a hardware protection option using a write protect pin that prevents programming or erasing, regardless of the state of the sector's Persistent or Dynamic Protection Bits. The  $\overline{WP}/ACC$  pin is associated with the “outermost”  $2 \times 4K$  words on both ends of boot sectors. The  $\overline{WP}/ACC$  pin has no effect on any other sector. When  $\overline{WP}/ACC$  is taken to  $V_{IL}$ , programming and erase operations of the “outermost”  $2 \times 4K$  words sectors on both end are disabled. By taking  $\overline{WP}/ACC$  back to  $V_{IH}$ , the “outermost”  $2 \times 4K$  words sectors are enabled for

program and erase operations, depending upon the status of the individual sector Persistent or Dynamic Protection Bits. If either of the two outermost sectors Persistent or Dynamic Protection Bits are programmed, program or erase operations are inhibited. If the sector Persistent or Dynamic Protection Bits are both erased, the two sectors are available for programming or erasing as long as  $\overline{WP}/ACC$  remains at  $V_{IH}$ . The user must hold the  $\overline{WP}/ACC$  pin at either  $V_{IH}$  or  $V_{IL}$  during the entire program or erase operation of the “outermost” two sectors on both end of boot sectors.

## (2) Sector Group Protection [Software Protection]

The device features hardware sector protection. This feature disables both program and erase operations in any number of sector groups. The sector protection feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected.

To activate this mode, the programming equipment must force  $V_{ID}$  on address pin  $A_9$  and control pin  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ ,  $(A_6, A_5, A_4, A_3, A_2, A_1, A_0) = (0, 1, 1, 1, 0, 1, 0)$ . The sector addresses pins  $(A_{22}, A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, \text{ and } A_{12})$  should be set to the sector to be protected. Programming of the protection circuitry begins on the falling edge of the  $\overline{WE}$  pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the  $\overline{WE}$  pulse. See “Sector Group Protection Timing Diagram” in “■ TIMING DIAGRAM” and “Sector Group Protection Algorithm” in “■ FLOW CHART” for sector protection waveforms and algorithms.

To verify programming of the protection circuitry, the programming equipment must force  $V_{ID}$  on address pin  $A_9$  with  $\overline{CE}$  and  $\overline{OE}$  at  $V_{IL}$  and  $\overline{WE}$  at  $V_{IH}$ . Scanning the sector addresses  $(A_{22}, A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, \text{ and } A_{12})$  while  $(A_6, A_5, A_4, A_3, A_2, A_1, A_0) = (0, 1, 1, 1, 0, 1, 0)$  produces logic “1” at device output  $DQ_0$  for a protected sector. Otherwise the device produces logic “0” for an unprotected sector. In this mode, the lower order addresses, except for  $A_0$ ,  $A_1$ , and  $A_6$  are DON'T CARES. Address locations with  $A_1 = V_{IL}$  are reserved for Autoselect manufacturer code.

It is also possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location  $XX02h$ , where the higher order addresses pins  $(A_{22}, A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, \text{ and } A_{12})$  represents the sector address will produce a logical “1” at  $DQ_0$  for a protected sector. See “MBM29QM96DF Autoselect Codes Table” and “Extended Autoselect Codes Table” in “■ DEVICE BUS OPERATION”.

## (3) Extended Sector Group Protection [Software Protection]

In addition to normal sector group protection, the device has Extended Sector Group Protection as extended function. This function enables protection of the sector group by forcing  $V_{ID}$  on  $\overline{RESET}$  pin and writes a command sequence. Unlike conventional procedures, it is not necessary to force  $V_{ID}$  and control timing for control pins. The only  $\overline{RESET}$  pin requires  $V_{ID}$  for sector group protection in this mode. The extended sector group protection requires  $V_{ID}$  on  $\overline{RESET}$  pin. With this condition the operation is initiated by writing the set-up command (60h) in the command register. Then the sector group addresses pins  $(A_{22}, A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, \text{ and } A_{12})$  and  $(A_6, A_5, A_4, A_3, A_2, A_1, A_0) = (0, 1, 1, 1, 0, 1, 0)$  should be set to the sector group to be protected (setting  $V_{IL}$  for the other addresses pins is recommended), and an extended sector group protection command (60h) should be written. A sector group is typically protected in 250  $\mu s$ . To verify programming of the protection circuitry, the sector group addresses pins  $(A_{22}, A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, \text{ and } A_{12})$  and  $(A_6, A_5, A_4, A_3, A_2, A_1, A_0) = (0, 1, 1, 1, 0, 1, 0)$  should be set a command (40h) should be written. Following the command write, logic “1” at device output  $DQ_0$  produces a protected sector in the read operation. If the output is logic “0”, write the extended sector group protection command (60h) again. To terminate the operation, it is necessary to set  $\overline{RESET}$  pin to  $V_{IH}$ . Refer to “Extended Sector Group Protection Timing Diagram” in “■ TIMING DIAGRAM” and “Extended Sector Group Protection Algorithm” in “■ FLOW CHART”.

## (4) New Sector Protection [Software Protection]

A command sector protection method that replaces the old  $V_{ID}$  controlled protection method in future. However MBM29QM96DF supports both  $V_{ID}$  protection and Persistent Sector Protection. Both Protect supported as a shift period.

The persistent Sector Protection and the old  $V_{ID}$  controlled protection can go back each other until Persistent Protection Lock Bit is settled.

**a) Persistent Protection Bit (PPB)**

A single Persistent (non-volatile) Protection Bit is assigned to a maximum four sectors (see the sector address tables for specific sector protection groupings). All 4 K words boot-block sectors have individual sector Persistent Protection Bits (PPBs) for greater flexibility. Each PPB is individually modifiable through the PPB Write Command.

Note: If a PPB requires erasure, all of the sector PPBs must first be preprogrammed prior to PPB erasing. All PPBs erase in parallel, unlike programming where individual PPBs are programmable. It is the responsibility of the user to perform the preprogramming operation. Otherwise, an already erased sector PPBs has the potential of being over-erased. There is no hardware mechanism to prevent sector PPBs over-erasure.

**b) Dynamic Protection Bit (DPB)**

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DPBs is "0". Each DPB is individually modifiable through the DPB Write Command.

When the parts are first shipped, the PPBs are cleared, the DPBs are cleared, and PPB Lock is defaulted to power up in the cleared state-meaning the PPBs are changeable.

When the device is first powered on the DPBs power up cleared (sectors not protected). The Protection State for each sector is determined by the logical OR of the PPB and the DPB related to that sector. For the sectors that have the PPBs cleared, the DPBs control whether or not the sector is protected or unprotected. By issuing the DPB Write/Erase command sequences, the DPBs will be set or cleared, thus placing each sector in the protected or unprotected state. These are the so-called Dynamic Locked or Unlocked states. They are called dynamic states because it is very easy to switch back and forth between the protected and unprotected conditions. This allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed. The DPBs maybe set or cleared as often as needed.

**PPB vs DPB**

The PPBs allow for a more static, and difficult to change, level of protection. The PPBs retain their state across power cycles because they are Non-Volatile. Individual PPBs are set with a command but must all be cleared as a group through a complex sequence of program and erasing commands. The PPBs are also limited to 100 erase cycles.

The PPB Lock bit adds an additional level of protection. Once all PPBs are programmed to the desired settings, the PPB Lock may be set to "1". Setting the PPB Lock disables all program and erase commands to the Non-Volatile PPBs. In effect, the PPB Lock Bit locks the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle. System boot code can determine if any changes to the PPB are needed e.g. to allow new system code to be downloaded. If no changes are needed then the boot code can set the PPB Lock to disable any further changes to the PPBs during system operation.

The  $\overline{WP}/ACC$  write protect pin adds a final level of hardware protection to the two outermost 4K words sectors. When this pin is low it is not possible to change the contents of these two sectors. These sectors generally hold system boot code. So, the  $\overline{WP}/ACC$  pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DPB Write command sequence is all that is necessary. The DPB write/erase command for the dynamic sectors switch the DPBs to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock bit must be disabled by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB lock bit once again will lock the PPBs, and the device operates normally again.

Note: to achieve the best protection, it's recommended to execute the PPB lock bit set command early in the boot code, and protect the boot code by holding  $\overline{WP}/ACC = V_{IL}$ .

DPB	PPB	PPB Lock	Sector State
0	0	0	Unprotected—PPB and DPB are changeable
1	0	0	Protected—PPB and DPB and DPB are changeable
0	1	0	Protected—PPB and DPB and DPB are changeable
1	1	0	Protected—PPB and DPB and DPB are changeable
0	0	1	Unprotected—PPB not changeable, DPB is changeable
1	0	1	Protected—PPB not changeable, DPB is changeable
0	1	1	Protected—PPB not changeable, DPB is changeable
1	1	1	Protected—PPB not changeable, DPB is changeable

The above table contains all possible combinations of the DPB, PPB, and PPB lock relating to the status of the sector.

In summary, if the PPB is set, and the PPB lock is set, the sector is protected and the protection can not be removed until the next power cycle clears the PBB lock. If the PPB is cleared, the sector can be dynamically locked or unlocked. The DPB then controls whether or not the sector is protected or unprotected.

If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program command to a protected sector enables status polling for approximately 1  $\mu$ s before the device returns to read mode without having modified the contents of the protected sector. An erase command to a protected sector enables status polling for approximately 50  $\mu$ s after which the device returns to read mode without having erased the protected sector.

The programming of the DPB, PPB, and PPB lock for a given sector can be verified by writing a DPB/PPB/PPB lock verify command to the device.

## –DPB Status

The programming of the DPB for a given sector can be verified by writing a DPB status verify command to the device.

## –PPB Status

The programming of the PPB for a given sector can be verified by writing a PPB status verify command to the device.

## –PPB Lock Bit Status

The programming of the PPB Lock Bit for a given sector can be verified by writing a PPB Lock Bit status verify command to the device.

## c) Persistent Protection Bit Lock (PPB Lock)

- **PPB Locked**
- **PPB Locked with Password**

A highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted.

All parts default to operate in the Persistent Sector Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method will be used. If the customer decides to continue using the Persistent Sector Protection method, they must set the Persistent Sector Protection Mode Locking Bit. This will permanently set the part to operate only using Persistent Sector Protection. If the customer decides to use the password method, they must set the Password Mode Locking Bit. This will permanently set the part to operate only using password sector protection.

It is important to remember that setting either the Persistent Sector Protection Mode Locking Bit or the Password Mode Locking Bit permanently selects the protection mode. It is not possible to switch between the two methods once a locking bit has been set. It is important that one mode is explicitly selected when the device is first programmed, rather than relying on the default mode alone. This is so that it is not possible for a system program or virus to later set the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode.

The  $\overline{WP}/ACC$  Hardware Protection feature is always available, independent of the software managed protection method chosen.

A global volatile bit. When set to “1”, the PPBs cannot be changed. When cleared (“0”), the PPBs are changeable. There is only one PPB Lock bit per device. The PPB Lock is cleared after power-up or hardware reset. There is no command sequence to unlock the PPB Lock.

The Persistent Protection Bit (PPB) Lock is a volatile bit that reflects the state of the Password Mode Locking Bit after power-up reset. If the Password Mode Locking Bit is set, which indicates the device is in Password Protection Mode, the PPB Lock Bit is also set after a hardware reset ( $\overline{RESET}$  asserted) or a power-up reset. The ONLY means for clearing the PPB Lock Bit in Password Protection Mode is to issue the Password Unlock command. Successful execution of the Password Unlock command clears the PPB Lock Bit, allowing for sector PPBs modifications. Asserting  $\overline{RESET}$ , taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit back to a “1”.

If the Password Mode Locking Bit is not set, indicating Persistent Sector Protection Mode, the PPB Lock Bit is cleared after power-up or hardware reset. The PPB Lock Bit is set by issuing the PPB Lock Bit Set command. Once set the only means for clearing the PPB Lock Bit is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Sector Protection Mode.

#### **-Password and Password Mode Locking Bit**

In order to select the Password sector protection scheme, the customer must first program the password. Fujitsu recommends that the password be somehow correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Verify operations.

Once the desired password is programmed in, the customer must then set the Password Mode Locking Bit. This operation achieves two objectives:

- (1) It permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.
- (2) It also disables all further commands to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Protection method is desired when setting the Password Mode Locking Bit. More importantly, the user must be sure that the password is correct when the Password Mode Locking Bit is set. Due to the fact that read operations are disabled, there is no means to verify what the password is afterwards. If the password is lost after setting the Password Mode Locking Bit, there will be no way to clear the PPB Lock bit.

The Password Mode Locking Bit, once set, prevents reading the 64-bit password on the DQ bus and further password programming. The Password Mode Locking Bit is not erasable. Once Password Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

#### **64-bit Password**

The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Verify commands (see “Password Verify Command”). The password function works in conjunction with the Password Mode Locking Bit, which when set, prevents the Password Verify command from reading the contents of the password on the pins of the device.

## **-Persistent Sector Protection Mode Locking Bit**

Like the password mode locking bit, a Persistent Sector Protection mode locking bit exists to guarantee that the device remain in software sector protection. Once set, the Persistent Sector Protection locking bit prevents programming of the password protection mode locking bit. This guarantees that a hacker could not place the device in password protection mode.

## **(5) Temporary Sector Group Unprotection**

This feature allows temporary unprotection of previously protected sectors of the device in order to change data. The Sector Unprotection mode is activated by setting the  $\overline{\text{RESET}}$  pin to high voltage ( $V_{\text{ID}}$ ). During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once the  $V_{\text{ID}}$  is taken away from the  $\overline{\text{RESET}}$  pin, all the previously protected sector groups will be protected again. While PPB Lock is set, this device cannot enter the Temporary Sector Unprotection mode.



## ■ COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Some commands require Bank Address (BA) input. When command sequences are input into bank reading, the commands have priority over the reading. “MBM29QM96DF Command Definitions Table” in “■ DEVICE BUS OPERATION” shows the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Also the Program Suspend (B0h) and Program Resume (30h) commands are valid only while the Program operation is in progress. Moreover, Read/Reset commands are functionally equivalent, resetting the device to the read mode. Please note that commands are always written at DQ<sub>7</sub> to DQ<sub>0</sub> and DQ<sub>15</sub> to DQ<sub>8</sub> bits are ignored.

### Read/Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits (DQ<sub>5</sub> = 1) to Read/Reset mode, verify mode of sector protect commands, the Read/Reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device automatically powers-up in the Read/Reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

### Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. Therefore manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A<sub>9</sub> to a higher voltage. However multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register.

The Autoselect command sequence is initiated first by writing two unlock cycles. This is followed by a third write cycle that contains the bank address (BA) and the Autoselect command. Then the manufacture and device codes can be read from the bank, and actual data from the memory cell can be read from another bank. The higher order address (A<sub>22</sub>, A<sub>21</sub>, A<sub>20</sub>, A<sub>19</sub>, A<sub>18</sub>) required for reading out the manufacture and device codes demands the bank address (BA) set at the third write cycle.

Following the command write, a read cycle from address (BA) 00h returns the manufacturer's code (Fujitsu = 04h). And a read cycle at address (BA) 01h outputs device code. When 227Eh is output, this indicates that two additional codes, called Extended Device Codes will be required. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh, as well as at (BA) 0Fh. Refer to “MBM29QM96DF Autoselect Codes Table” and “Extended Autoselect Codes Table” in “■ DEVICE BUS OPERATION”.

The sector state (PPB protection or PPB unprotection) is informed by address (SA) XX02h. Scanning the sector group addresses (A<sub>22</sub>, A<sub>21</sub>, A<sub>20</sub>, A<sub>19</sub>, A<sub>18</sub>, A<sub>17</sub>, A<sub>16</sub>, A<sub>15</sub>, A<sub>14</sub>, A<sub>13</sub>, and A<sub>12</sub>) while (A<sub>6</sub>, A<sub>5</sub>, A<sub>4</sub>, A<sub>3</sub>, A<sub>2</sub>, A<sub>1</sub>, A<sub>0</sub>) = (0, 1, 1, 1, 0, 1, 0) produces logic “1” at device output DQ<sub>0</sub> for a protected sector group. The programming verification should be performed by verifying sector group protection on the protected sector. See “MBM29QM96DF User Bus Operation Table” in “■ DEVICE BUS OPERATION”.

The manufacture and device codes can be read from the selected bank. To read the manufacture and device codes and sector protection status from a non-selected bank, it is necessary to write the Read/Reset command sequence into the register. Autoselect command should then be written into the bank to be read.

If the software (program code) for Autoselect command is stored in the Flash memory, the device and manufacture codes should be read from the other bank, which does not contain the software.

To terminate the operation, it is necessary to write the Read/Reset command sequence into the register. To execute the Autoselect command during the operation, Read/Reset command sequence must be written before the Autoselect command.

## Word Programming Command

The device is programmed on word-by-word basis. Programming is a four bus cycle operation. There are two “unlock” write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever happens later, and the data is latched on the rising edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever happens first. The rising edge of  $\overline{CE}$  or  $\overline{WE}$  (whichever happens first) starts programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device automatically provides adequate internally generated program pulses and verify programmed cell margin.

The system can determine the status of the program operation by using  $DQ_7$  ( $\overline{Data}$  Polling),  $DQ_6$  (Toggle Bit) or  $RY/BY$ . The  $\overline{Data}$  Polling and Toggle Bit must be performed at the memory location being programmed.

The automatic programming operation is completed when the data on  $DQ_7$  is equivalent to data written to this bit at which device returns to the read mode and addresses are no longer latched. See “Hardware Sequence Flags Table” in “■ COMMAND DEFINITIONS”. Therefore the device requires that a valid address to the device be supplied by the system in this particular instance. Hence  $\overline{Data}$  Polling must be performed at the memory location being programmed.

If hardware reset occurs during the programming operation, the data being written is not guaranteed.

Programming is allowed in any sequence and across sector boundaries. Beware that a data “0” cannot be programmed back to a “1”. Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from Read/Reset mode will show that the data is still “0”. Only erase operations can convert from “0”s to “1”s.

“Embedde Program™ Algorithm” in “■ FLOW CHART” illustrates the Embedded Program™ Algorithm using typical command strings and bus operations.

## Program Suspend/Resume Command

The Program Suspend command allows the system to interrupt a program operation so that data can be read from any address. Writing the Program Suspend command (B0h) during the Embedded Program operation immediately suspends the programming. The Program Suspend command may also be issued during a programming operation while an erase is suspended. The bank addresses of sector being programmed should be set when writing the Program Suspend command.

When the Program Suspend command is written during a programming process, the device halts the program operation within 1  $\mu$ s and updates the status bits.

After the program operation has been suspended, the system can read data from any address. The data at program-suspended address is not valid. Normal read timing and command definitions apply.

After the Program Resume command (30h) is written, the device reverts to programming. The bank addresses of sectors being suspended should be set when writing the Program Resume command. The system can determine the program operation status using the  $DQ_7$  or  $DQ_6$  status bits, just as in the standard program operation. See “Write Operation Status” for more information.

The system may also write the Autoselect command sequence in the Program Suspend mode. The device allows reading Autoselect codes at the addresses within programming sectors, since the codes are not stored in the memory. When the device exits from the Autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See “Autoselect Command Sequence” for more information.

The system must write the Program Resume command (address bits are “Bank Address”) to exit from the Program Suspend mode and continue programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device resumes programming.



## Chip Erase Command

Chip erase is a six-bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the chip erase command.

Chip erase does not require the user to program prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. (Preprogram Function) The system is not required to provide any controls or timings during these operations.

The system can determine the erase operation status by using DQ<sub>7</sub> ( $\overline{\text{Data}}$  Polling), or DQ<sub>6</sub> (Toggle Bit). The chip erase begins on the rising edge of the last  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$ , whichever happens first in the command sequence and terminates when the data on DQ<sub>7</sub> is “1” (See Write Operation Status section.) at which the device returns to read the mode.

Chip Erase Time; Sector Erase Time  $\times$  All sectors + Chip Program Time (Preprogramming)

“Embedde Erase™ Algorithm” in “■ FLOW CHART” illustrates the Embedded Erase™ Algorithm for typical command strings and bus operations.

## Sector Erase Command

Sector erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  whichever starts later, while the command (Data = 30h) is latched on the rising edge of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  whichever starts first. After time-out of “t<sub>row</sub>” from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors are erased concurrently by writing the six bus cycle operations on “MBM29QM96DF Command Definitions Table” in “■ DEVICE BUS OPERATION”. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than “t<sub>row</sub>” otherwise that command is not accepted and erasure does not start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of “t<sub>row</sub>” from the rising edge of last  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  whichever starts first initiates the execution of the Sector Erase command(s). If another falling edge of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$ , whichever starts first occurs within the “t<sub>row</sub>” time-out window the timer is reset. (Monitor DQ<sub>3</sub> to determine if the sector erase timer window is still open, see section DQ<sub>3</sub>, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this time-out period will reset the device to the read mode, ignoring the previous command string. Resetting the device once execution has begun may corrupt the data in the sector. In that case restart the erase on those sectors and allow them to complete. Refer to Write Operation Status section for Sector Erase Timer operation. Loading the sector erase buffer may be done in any sequence and with any number of sectors.

Sector erase does not require the user to program prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase (Preprogram function). When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ<sub>7</sub> ( $\overline{\text{Data}}$  Polling), or DQ<sub>6</sub> (Toggle Bit).

The sector erase begins after the “t<sub>row</sub>” time out from the rising edge of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  whichever starts first for the last sector erase command pulse and terminates when the data on DQ<sub>7</sub> is “1”. See Write Operation Status section. at which time the device returns to the read mode.  $\overline{\text{Data}}$  polling and Toggle Bit must be performed at an address within any of the sectors being erased.

Multiple Sector Erase Time; [Sector Erase Time + Sector Program Time (Preprogramming)]  $\times$  Number of Sector Erase.

In case of multiple sector erase across bank boundaries, a read from the bank (read-while-erase) to which sectors being erased belong cannot be performed.

“Embedde Erase™ Algorithm” in “■ FLOW CHART” illustrates the Embedded Erase™ Algorithm for typical command strings and bus operations.

## Erase Suspend/Resume Command

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads from or programs to a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time-out period for sector erase. The Erase Suspend command is ignored during the Chip Erase operation. Writing the Erase Suspend command (B0h) during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the Erase Resume command (30h) resumes the erase operation. The addresses are “DON'T CARES” when writing the Erase Suspend or Erase Resume command. When the Erase Suspend command is written during the Sector Erase operation, the device takes a maximum of “ $t_{SPD}$ ” to suspend the erase operation. When the device has entered the erase-suspended mode, the DQ<sub>7</sub> bit is at logic “1”, and DQ<sub>6</sub> stops toggling. The user must use the address of the erasing sector for reading DQ<sub>6</sub> and DQ<sub>7</sub> to determine if the erase operation is suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation is suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode causes DQ<sub>2</sub> to toggle. See the section on DQ<sub>2</sub>.

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Program. This program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-program mode causes DQ<sub>2</sub> to toggle. The end of the erase-suspended Program operation is detected by the Data polling of DQ<sub>7</sub> or by the Toggle Bit I (DQ<sub>6</sub>) which is the same as the regular Program operation. Note that DQ<sub>7</sub> must be read from the Program address while DQ<sub>6</sub> can be read from any address.

To resume the operation of Sector Erase, the Resume command (30h) should be written. Any further writes of the Resume command at this point is ignored. Another Erase Suspend command is written after the chip resumes erasing.

## Fast Mode

Fast Mode function dispenses with the initial two unlock cycles required in the standard program command sequence writing Fast Mode command into the command register. In this mode the required bus cycle for programming is two cycles instead of four bus cycles in standard program command. The read operation is also executed after exiting this mode. During the Fast mode, do not write any commands other than the Fast program/Fast mode reset command. To exit this mode, write Fast Mode Reset command into the command register. Refer to “Embedded Program Algorithm for Fast Mode” in “■ FLOW CHART”. The V<sub>CC</sub> active current is required even  $\overline{CE} = V_{IH}$  during Fast Mode.

## Fast Programming

During Fast Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0h) and data write cycles (PA/PD). Refer to “Embedded Program Algorithm for Fast Mode” in “■ FLOW CHART”.

## Query (CFI:Common Flash Memory Interface)

The CFI (Common Flash Memory Interface) specification outlines device and host system software interrogation handshake which allows specific vendor-specified software algorithms to be used for entire families of device. This allows device-independent, JEDEC ID-independent, and forward-and backward-compatible software support for the specified flash device families. Refer to “Common Flash Memory Interface Code Table” in “■ FLEXIBLE SECTOR-ERASE ARCHITECTURE” in detail.

The operation is initiated by writing the query command (98h) into the command register. Following the command write, a read cycle from specific address retrieves device information. Please note that output data of upper byte

(DQ<sub>15</sub> to DQ<sub>8</sub>) is “0”. Refer to “Common Flash Memory Interface Code Table” in “■ FLEXIBLE SECTOR-ERASE ARCHITECTURE”. To terminate operation, write the Read/Reset command sequence into the register.

### **HiddenROM Entry Command**

The device has a HiddenROM area with One Time Protect function. This area is to enter the security code and to enable the change of the code once set. Program/erase is possible in this area until it is protected. However once it is protected, it is impossible to unprotect. Therefore extreme caution is required.

HiddenROM area is 256 byte. This area is normally the “outermost” 8K words boot block area. Therefore, write the HiddenROM entry command sequence to enter the HiddenROM area. It is called HiddenROM mode when the HiddenROM area appears.

The following commands are permitted after issuing the HiddenROM Entry command:

1. Autoselect
2. Password Program
3. Password Verify
4. Password Unlock
5. Read/Reset
6. Program
7. Chip and Sector Erase
8. HiddenROM Protection Bit Program
9. PPB Program
10. All PPB Erase
11. PPB Lock Bit Set
12. DPB Write
13. DPB/PPB/PPB Lock Bit Verify
14. HiddenROM Exit

The following commands are unavailable when the HiddenROM is enabled. Issuing the following commands while the HiddenROM is enabled results in the command being ignored.

1. CFI
2. Set to Fast Mode
3. Fast Program
4. Reset from Fast Mode
5. Program and Sector Erase Suspend
6. Program and Sector Erase Resume

The HiddenROM Entry command is allowed when the device is in either program or erase suspend modes. If the HiddenROM is enabled, the program or erase suspend command is ignored. This prevents resuming either programming or erase on the HiddenROM if the overlayed sector is undergoing programming or erase. It is the responsibility of the software to resume the program or erase of a suspended program or erase after exiting the HiddenROM.

Executing any of the PPB program/erase commands, or Password Unlock command results in the Bank A returning the status of these operations while they are in progress, thus making the HiddenROM unavailable for reading. If the HiddenROM is enabled while the DPB command is issued, the DPB for the overlayed sector is NOT updated. Reading the DPB status using the PPB Lock Bit/DPB verify command when the HiddenROM is enabled returns invalid data. Note that any other commands should not be issued other than the HiddenROM program/protection/reset commands during the HiddenROM mode. When you issue the other commands including the suspend resume, send the HiddenROM reset command first to exit the HiddenROM mode and then issue each command.

### **HiddenROM™ Program Command**

To program the data to the HiddenROM area, write the HiddenROM program command sequence during HiddenROM mode. This command is the same as the program command in usual except to write the command during HiddenROM mode. Therefore the detection of completion method is the same as using the DQ<sub>7</sub> data

polling, and DQ<sub>6</sub> toggle bit. Need to pay attention to the address to be programmed. If the address other than the HiddenROM area is selected to program, data of the address are changed.

During the write into the HiddenROM region, the program suspend command issuance is prohibited.

## HiddenROM™ Protect Command

The method to protect the HiddenROM is to apply high voltage (V<sub>ID</sub>) to A<sub>9</sub> and  $\overline{OE}$ , set the sector address in the HiddenROM area and (A<sub>6</sub>, A<sub>5</sub>, A<sub>4</sub>, A<sub>3</sub>, A<sub>2</sub>, A<sub>1</sub>, A<sub>0</sub>) = (0, 0, 1, 1, X, 1, 0), and apply the write pulse during the HiddenROM mode. To verify the protect circuit, apply high voltage (V<sub>ID</sub>) to A<sub>9</sub>, specify (A<sub>6</sub>, A<sub>5</sub>, A<sub>4</sub>, A<sub>3</sub>, A<sub>2</sub>, A<sub>1</sub>, A<sub>0</sub>) = (0, 0, 1, 1, X, 1, 0) and the sector address in the HiddenROM area, and read. When “1” appears on DQ<sub>0</sub>, the protect setting is completed. “0” appears on DQ<sub>0</sub> if it is not protected. Please apply write pulse again. The same command sequence could be used for the above method because other than the HiddenROM mode, it is the same as the sector protect in the past.

And the device has also HiddenROM protect command without V<sub>ID</sub>. See “MBM29QM96DF Command Definitions Table” in “■ DEVICE BUS OPERATION”.

Other sector will be effected if the address other than those for HiddenROM area is selected for the sector address, so please be careful. Once it is protected, protection can not be cancelled, so please pay the closest attention.

## Password Program Command

The Password Program Command permits programming the password that is used as part of the hardware protection scheme. The actual password is 64-bits long. 4 Password Program commands are required to program the password. The user must enter the unlock cycle, password program command (38h) and the program address/data for each portion of the password when programming. There are no provisions for entering the 2-cycle unlock cycle, the password program command, and all the password data. There is no special addressing order required for programming the password. Also, when the password is undergoing programming, Simultaneous Operation is disabled. Read operations to any memory location will return the programming status. Once programming is complete, the user must issue a Read/Reset command to return the device to normal operation. Once the Password is written and verified, the Password Mode Locking Bit must be set in order to prevent verification. The Password Program Command is only capable of programming “0”s. Programming a “1” after a cell is programmed as a “0” results in a time-out by the Embedded Program Algorithm with the cell remaining as a “0”. The password is all F’s when shipped from the factory. All 64-bit password combinations are valid as a password. Writing the HiddenROM Exit command returns the device back to normal operation.

## Password Verify Command

The Password Verify Command is used to verify the Password. The Password is verifiable only when the Password Mode Locking Bit is not programmed. If the Password Mode Locking Bit is programmed and the user attempts to verify the Password, the device will always drive all F’s onto the DQ data bus.

The Password Verify command is permitted if the HiddenROM is enabled. Also, the device will not operate in Simultaneous Operation when the Password Verify command is executed. Only the password is returned regardless of the bank address. The lower two address bits (A<sub>1</sub>:A<sub>0</sub>) are valid during the Password Verify. Writing the HiddenROM Exit command returns the device back to normal operation.

## Password Protection Mode Locking Bit Program Command

The Password Protection Mode Locking Bit Program Command programs the Password Protection Mode Locking Bit, which prevents further verifies or updates to the Password. Once programmed, the Password Protection Mode Locking Bit cannot be erase. Once the Password Protection Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit program circuitry is disabled, thereby forcing the device to remain in the Password Protection mode. After issuing “PL/68h” at 4th bus cycle, the device requires approximately 150μs time out period for programming the Password Protection Mode Locking Bit. Then by writing “PL/48h” at 5th bus cycle, the device outputs verify data at DQ<sub>0</sub>. If DQ<sub>0</sub> = 1 then Password Protection Mode Locking Bit is programmed. If not, then the user needs to repeat this program sequence from the 4th cycle of “PL/68h”. Exiting the Mode Locking Bit Program command is accomplished by writing the HiddenROM Exit command.

**Persistent Sector Protection Mode Locking Bit Program Command**

The Persistent Sector Protection Mode Locking Bit Program Command programs the Persistent Sector Protection Mode Locking Bit, which prevents the Password Mode Locking Bit from ever being programmed. By disabling the program circuitry of the Password Mode Locking Bit, the device is forced to remain in the Persistent Sector Protection mode of operation, once this bit is set. After issuing "SPML/68h" at 4th bus cycle, the device requires approximately 150µs time out period for programming the Persistent Protection Mode Locking Bit. Then by writing "SPML/48h" at 5th bus cycle, the device outputs verify data at DQ<sub>0</sub>. If DQ<sub>0</sub> = 1 then Persistent Protection Mode Locking Bit is programmed. If not, then the user needs to repeat this program sequence from the 4th cycle of "SPML/68h". Exiting the Persistent Protection Mode Locking Bit Program command is accomplished by writing the HiddenROM Exit command.

**PPB Lock Bit Set Command**

The PPB Lock Bit Set command is used to set the PPB Lock bit if it is cleared either at reset or if the Password Unlock command was successfully executed. There is no PPB Lock Bit Clear command. Once the PPB Lock Bit is set, it cannot be cleared unless the device is taken through a power-on clear or the Password Unlock command is executed. If the Password Mode Locking Bit is set, the PPB Lock Bit status is reflected as set, even after a power-on reset cycle. Exiting the PPB Lock Bit Set command is accomplished by writing the HiddenROM Exit command.

**DPB Write(Erase) Command**

The DPB Write command is used to set or clear a DPB for a given sector. The high order address bits (A<sub>22</sub> to A<sub>12</sub>) are issued at the same time as the code 01h or 00h on DQ<sub>7</sub> to DQ<sub>0</sub>. All other DQ data bus pins are ignored during the data write cycle. The DPBs are modifiable at any time, regardless of the state of the PPB or PPB Lock Bit. The DPBs are cleared at power-up or hardware reset. Exiting the DPB Write command is accomplished by writing the HiddenROM Exit command.

**DPB Verify command**

DPB verify command is used to verify the status of a DPB for given sector.

Scanning the sector addresses (SA) will produce a logical "1" at the device output DQ<sub>0</sub> for a protected sector. Otherwise the device will produce "0" at DQ<sub>0</sub> for the sector which is not protected. Writing the HiddenROM Exit Command returns the device back to normal operation.

**PPB Lock Bit Verify command**

PPB Lock Bit verify command is used to verify the status of a PPB Lock Bit.

A logical "1" at the device output DQ<sub>1</sub> indicates that the PPB Lock Bit is set.

If PPB Lock Bit is not set, DQ<sub>1</sub> will output "0". Writing the HiddenROM Exit Command returns the device back to normal operation.

**Password Unlock Command**

The Password Unlock command is used to clear the PPB Lock Bit so that the PPBs can be unlocked for modification, thereby allowing the PPBs to become accessible for modification. The exact password must be entered in order for the unlocking function to occur. This command cannot be issued any faster than 2 µs at a time to prevent a hacker from running through the all 64-bit combinations in an attempt to correctly match a password. If the command is issued before the 2 µs execution window for each portion of the unlock, the command will be ignored.

The Password Unlock function is accomplished by writing Password Unlock command and data to the device to perform the clearing of the PPB Lock Bit. A<sub>0</sub> and A<sub>1</sub> are used to determine the 16 bit data quantity is used to match separated 16 bits. Writing the Password Unlock command is address order specific. In other words, the lowers address A<sub>1</sub>:A<sub>0</sub> = 00, the next cycle command is to A<sub>1</sub>:A<sub>0</sub> = 01, then to A<sub>1</sub>:A<sub>0</sub> = 10, and finally to A<sub>1</sub>:A<sub>0</sub> = 11. Writing out of sequence results in the Password Unlock not returning a match with the password and the PPB Lock Bit remains set.



Once the Password Unlock command is entered, the  $\overline{\text{RY/BY}}$  pin goes LOW indicating that the device is busy. Also, reading the Bank A results in the  $\text{DQ}_6$  pin toggling, indicating that the Password Unlock function is in progress. Reading the other bank returns actual array data. Approximately  $2\mu\text{s}$  is required for each portion of the unlock. Once the first portion of the password unlock completes ( $\overline{\text{RY/BY}}$  is not driven and  $\text{DQ}_6$  does not toggle when read), the next cycle is issued, only this time with the next part of the password. Seven cycles Password Unlock commands are required to successfully clear the PPB Lock Bit. As with the first Password Unlock command, the  $\overline{\text{RY/BY}}$  signal goes LOW and reading the device results in the  $\text{DQ}_6$  pin toggling on successive read operations until complete. It is the responsibility of the microprocessor to keep track of the number of Password Unlock cycles, the order, and when to read the PPB Lock bit to confirm successful password unlock. Writing the HiddenROM Exit Command returns the device back to normal operation.

## PPB Program Command

The PPB Program command is used to program, or set, a given PPB. Each PPB is individually programmed (but is bulk erased with the other PPBs). The specific sector address ( $\text{A}_{22}$  to  $\text{A}_{12}$ ) are written at the same time as the program command  $60\text{h}$ . If the PPB Lock Bit is set and the corresponding PPB is set for the sector, the PPB Program command will not execute and the command will time-out without programming the PPB. After issuing " $\text{SGA} + \text{WP}/68\text{h}$ " at 4th bus cycle, the device requires approximately  $150\mu\text{s}$  time out period for programming the PPB. Then by writing " $\text{SGA} + \text{WP}/48\text{h}$ " at 5th bus cycle, the device outputs verify data at  $\text{DQ}_0$ . If  $\text{DQ}_0 = 1$  then PPB is programmed. If not, then the user needs to repeat this program sequence from the 4th cycle of " $\text{SGA} + \text{WP}/68\text{h}$ ".

The PPB Program command does not follow the Embedded Program algorithm. Writing the HiddenROM Exit Command returns the device back to normal operation.

## All PPB Erase Command

The All PPB Erase command is used to erase all PPBs in bulk. There is no means for individually erasing a specific PPB. Unlike the PPB program, no specific sector address is required. However, when the PPB erase command is written ( $60\text{h}$ ), all Sector PPBs are erased in parallel. If the PPB Lock Bit is set the ALL PPB Erase command will not execute and the command will time-out without erasing the PPBs. After issuing " $\text{WP}/60\text{h}$ " at 4th bus cycle, the device requires approximately  $1.5\text{ms}$  time out period for programming the PPB. Then by writing " $\text{SGA} + \text{WP}/40\text{h}$ " at 5th bus cycle, the device outputs verify data at  $\text{DQ}_0$ . If  $\text{DQ}_0 = 0$  then PPB is successfully erased. If not, then the user needs to repeat this program sequence from the 4th cycle of " $\text{WP}/60\text{h}$ ".

It is the responsibility of the user to preprogram all PPBs prior to issuing the All PPB Erase command. If the user attempts to erase a cleared PPB, over-erasure may occur making it difficult to program the PPB at a later time. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed. Writing the HiddenROM Exit Command returns the device back to normal operation.

## Write Operation Status

Detailed in "Hardware Sequence Flags Table" in "■ COMMAND DEFINITIONS" are all the status flags which can determine the status of the bank for the current mode operation. The read operation from the bank which doesn't operate Embedded Algorithm returns data of memory cells. These bits offer a method for determining whether an Embedded Algorithm is properly completed. The information on  $\text{DQ}_2$  is address-sensitive. This means that if an address from an erasing sector is consecutively read, the  $\text{DQ}_2$  bit will toggle. However,  $\text{DQ}_2$  will not toggle if an address from a non-erasing sector is consecutively read. This allows users to determine which sectors are in erase and which are not.

The status flag is not output from banks (non-busy banks) which do not execute Embedded Algorithms. For example, a bank (busy bank) is executing an Embedded Algorithm. When the read sequence is  $[1] < \text{busy bank} >$ ,  $[2] < \text{non-busy bank} >$ ,  $[3] < \text{busy bank} >$ , the  $\text{DQ}_6$  toggles in the case of  $[1]$  and  $[3]$ . In case of  $[2]$ , the data of memory cells are output. In the erase-suspend read mode with the same read sequence,  $\text{DQ}_6$  will not be toggled in  $[1]$  and  $[3]$ .

Hardware Sequence Flafs Table

Status			DQ <sub>7</sub>	DQ <sub>6</sub>	DQ <sub>5</sub>	DQ <sub>3</sub>	DQ <sub>2</sub>
In Progress	Embedded Program Algorithm		$\overline{\text{DQ}}_7$	Toggle	0	0	1
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle* <sup>1</sup>
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{\text{DQ}}_7$	Toggle	0	0	1* <sup>2</sup>
Exceeded Time Limits	Embedded Program Algorithm		$\overline{\text{DQ}}_7$	Toggle	1	0	1
	Embedded Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{\text{DQ}}_7$	Toggle	1	0	N/A

\*1 : Successive reads from the erasing or erase-suspend sector will cause DQ<sub>2</sub> to toggle.

\*2 : Reading from non-erase suspend sector address will indicate logic “1” at the DQ<sub>2</sub> bit.

Notes: • DQ<sub>0</sub> and DQ<sub>1</sub> are reserve pins for future use.  
• DQ<sub>4</sub> is limited to Fujitsu internal use.

#### DQ<sub>7</sub>

##### Data Polling

The device features  $\overline{\text{Data}}$  Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm, an attempt to read the device will produce a complement of data last written to DQ<sub>7</sub>. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce true data last written to DQ<sub>7</sub>. During the Embedded Erase Algorithm, an attempt to read the device will produce a “0” at the DQ<sub>7</sub> output. Upon completion of the Embedded Erase Algorithm, an attempt to read device will produce a “1” on DQ<sub>7</sub>. The flowchart for  $\overline{\text{Data}}$  Polling (DQ<sub>7</sub>) is shown in “Data Polling Algorithm” in “■ FLOW CHART”.

For programming, the  $\overline{\text{Data}}$  Polling is valid after the rising edge of the fourth write pulse in the four write pulse sequences.

For chip erase and sector erase, the  $\overline{\text{Data}}$  Polling is valid after the rising edge of the sixth write pulse in the six write pulse sequences.  $\overline{\text{Data}}$  Polling must be performed at sector addresses of sectors being erased, not protected sectors. Otherwise the status may become invalid.

If a program address falls within a protected sector,  $\overline{\text{Data}}$  Polling on DQ<sub>7</sub> is active for approximately 1 μs, then that bank returns to the read mode. After an erase command sequence is written, if all sectors selected for erasing are protected,  $\overline{\text{Data}}$  Polling on DQ<sub>7</sub> is active for approximately 400 μs, then the bank returns to read mode.

Once the Embedded Algorithm operation is close to being completed, the device data pins (DQ<sub>7</sub>) may change asynchronously while the output enable ( $\overline{\text{OE}}$ ) is asserted low. This means that device is driving status information on DQ<sub>7</sub> at one instant, and then that byte’s valid data at the next instant. Depending on when the system samples the DQ<sub>7</sub> output, it may read the status or valid data. Even if device has completed the Embedded Algorithm operation and DQ<sub>7</sub> has a valid data, data outputs on DQ<sub>0</sub> to DQ<sub>6</sub> may still be invalid. The valid data on DQ<sub>0</sub> to DQ<sub>7</sub> will be read on successive read attempts.

The  $\overline{\text{Data}}$  Polling feature is active only during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out. (See “Toggle Bit Status Table” in “■ COMMAND DEFINITIONS”.)

See “Data Polling during Embedded Algorithm Operation Timing Diagram” in “■ TIMING DIAGRAM” for the  $\overline{\text{Data}}$  Polling timing specifications and diagrams.

## DQ<sub>6</sub>

### Toggle Bit I

The device also features the “Toggle Bit I” as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During Embedded Program or Erase Algorithm cycle, successive attempts to read ( $\overline{OE}$  toggling) data from the busy bank will result in DQ<sub>6</sub> toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ<sub>6</sub> will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth write pulse in the four write pulse sequences. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth write pulse in the six write pulse sequences. The Toggle Bit I is active during the sector time out.

In programming, if the sector being written is protected, the toggle bit will toggle for about 1  $\mu$ s and then stop toggling with data unchanged. In erase, the device will erase all selected sectors except for protected ones. If all selected sectors are protected, the chip will toggle the toggle bit for about 400  $\mu$ s and then drop back into read mode, having data kept remained.

Either  $\overline{CE}$  or  $\overline{OE}$  toggling will cause DQ<sub>6</sub> to toggle. In addition, an Erase Suspend/Resume command will cause DQ<sub>6</sub> to toggle.

The system can use DQ<sub>6</sub> to determine whether a sector is actively erased or is erase-suspended. When a bank is actively erased (that is, the Embedded Erase Algorithm is in progress), DQ<sub>6</sub> toggles. When a bank enters the Erase Suspend mode, DQ<sub>6</sub> stops toggling. Successive read cycles during erase-suspend-program cause DQ<sub>6</sub> to toggle.

To operate toggle bit function properly,  $\overline{CE}$  or  $\overline{OE}$  must be high when bank address is changed.

See “AC Waveforms for Toggle Bit I during Embedded Algorithm Operations Timing Diagram” in “■ TIMING DIAGRAM” for the Toggle Bit I timing specifications and diagrams.

## DQ<sub>5</sub>

### Exceeded Timing Limits

DQ<sub>5</sub> will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ<sub>5</sub> will produce “1”. This is a failure condition indicating that the program or erase cycle was not successfully completed. Data Polling is only operating function of the device under this condition. The  $\overline{CE}$  circuit will partially power down device under these conditions (to approximately 2 mA). The  $\overline{OE}$  and  $\overline{WE}$  pins will control the output disable functions as described in “MBM29QM96DF User Bus Operation Table” in “■ DEVICE BUS OPERATION”.

The DQ<sub>5</sub> failure condition may also appear if a user tries to program a non-blank location without pre-erase. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads valid data on DQ<sub>7</sub> bit and DQ<sub>6</sub> never stop toggling. Once the device has exceeded timing limits, the DQ<sub>5</sub> bit will indicate a “1.” Please note that this is not a device failure condition since the device was incorrectly used. If this occurs, reset device with the command sequence.

## DQ<sub>3</sub>

### Sector Erase Timer

After completion of the initial sector erase command sequence, sector erase time-out begins. DQ<sub>3</sub> will remain low until the time-out is completed. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit I indicates that a valid erase command has been written, DQ<sub>3</sub> may be used to determine whether the sector erase timer window is still open. If DQ<sub>3</sub> is high (“1”) the internally controlled erase cycle has begun. If DQ<sub>3</sub> is low (“0”), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ<sub>3</sub> prior to and following each subsequent Sector Erase command. If DQ<sub>3</sub> were high on the second status check, the command may not have been accepted.

See “Hardware Sequence Flags Table” in “■ COMMAND DEFINITIONS”: Hardware Sequence Flags.



## DQ<sub>2</sub>

### Toggle Bit II

This toggle bit II, along with DQ<sub>6</sub>, can be used to determine whether the device is in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ<sub>2</sub> to toggle during the Embedded Erase Algorithm. If the device is in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ<sub>2</sub> to toggle. When the device is in the erase-suspended-program mode, successive reads from the non-erase suspended sector will indicate a logic “1” at the DQ<sub>2</sub> bit.

DQ<sub>6</sub> is different from DQ<sub>2</sub> in that DQ<sub>6</sub> toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ<sub>7</sub>, is summarized as follows :

For example, DQ<sub>2</sub> and DQ<sub>6</sub> can be used together to determine if the erase-suspend-read mode is in progress. (DQ<sub>2</sub> toggles while DQ<sub>6</sub> does not.) See also “Toggle Bit Status Table” in “■ COMMAND DEFINITIONS” and “DQ<sub>2</sub> vs. DQ<sub>6</sub>” in “■ TIMING DIAGRAM”.

Furthermore DQ<sub>2</sub> can also be used to determine which sector is being erased. At the erase mode, DQ<sub>2</sub> toggles if this bit is read from an erasing sector.

To operate toggle bit function properly,  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  must be high when bank address is changed.

### Reading Toggle Bits DQ<sub>6</sub>/DQ<sub>2</sub>

Whenever the system initially begins reading toggle bit status, it must read DQ<sub>7</sub> to DQ<sub>0</sub> at least twice in a row to determine whether a toggle bit is toggling. Typically a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ<sub>7</sub> to DQ<sub>0</sub> on the following read cycle.

However, if, after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ<sub>5</sub> is high (see the section on DQ<sub>5</sub>) . If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ<sub>5</sub> went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ<sub>5</sub> has not gone high. The system may continue to monitor the toggle bit and DQ<sub>5</sub> through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation. (Refer to “Toggle Bit Algorithm” in “■ FLOW CHART”.)

**Toggle Bit Status Table**

Mode	DQ <sub>7</sub>	DQ <sub>6</sub>	DQ <sub>2</sub>
Program	DQ <sub>7</sub>	Toggle	1
Erase	0	Toggle	Toggle*
Erase-Suspend Read (Erase-Suspended Sector)	1	1	Toggle
Erase-Suspend Program	$\overline{\text{DQ}}_7$	Toggle	1*

\* : Successive reads from the erasing or erase-suspend sector will cause DQ<sub>2</sub> to toggle. Reading from non-erase suspend sector address will indicate logic “1” at the DQ<sub>2</sub> bit.

## **RY/ $\overline{\text{BY}}$ (Ready/Busy Pin)**

The device provides a RY/ $\overline{\text{BY}}$  open-drain output pin as a way to indicate to the host system that Embedded Algorithms are either in progress or have been completed. If output is low, the device is busy with either a program or erase operation. If output is high, the device is ready to accept any read/program or erase operation. If the device is placed in an Erase Suspend mode, RY/ $\overline{\text{BY}}$  output will be high.

During programming, the RY/ $\overline{\text{BY}}$  pin is driven low after the rising edge of the fourth write pulse. During an erase operation, the RY/ $\overline{\text{BY}}$  pin is driven low after the rising edge of the sixth write pulse. The RY/ $\overline{\text{BY}}$  pin will indicate a busy condition during  $\overline{\text{RESET}}$  pulse. Refer to “RY/ $\overline{\text{BY}}$  Timing Diagram during Program/Erase Operation Timing Diagram” and “ $\overline{\text{RESET}}$ , RY/ $\overline{\text{BY}}$  Timing Diagram” in “■ TIMING DIAGRAM” for a detailed timing diagram. The RY/ $\overline{\text{BY}}$  pin is pulled high in standby mode.

Since this is an open-drain output, RY/ $\overline{\text{BY}}$  pins can be tied together in parallel with a pull-up resistor to  $V_{CC}$ .

## **Data Protection**

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up device automatically resets internal state machine to Read mode. Also, with its control register architecture, alteration of memory contents only occurs after successful completion of specific multi-bus cycle command sequence.

Device also incorporates several features to prevent inadvertent write cycles resulting from  $V_{CC}$  power-up and power-down transitions or system noise.

## **Low $V_{CC}$ Write Inhibit**

To avoid initiation of a write cycle during  $V_{CC}$  power-up and power-down, a write cycle is locked out for  $V_{CC}$  less than  $V_{LKO}$  (Min). If  $V_{CC} < V_{LKO}$ , the command register is disabled and all internal program/erase circuits are disabled. Under this condition, the device will reset to the read mode. Subsequent writes will be ignored until the  $V_{CC}$  level is greater than  $V_{LKO}$ . It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when  $V_{CC}$  is above  $V_{LKO}$  (Min).

If the Embedded Erase Algorithm is interrupted, there is possibility that the erasing sector(s) can not be used.

## **Write Pulse “Glitch” Protection**

Noise pulses of less than 5 ns (typical) on  $\overline{\text{OE}}$ ,  $\overline{\text{CE}}$ , or  $\overline{\text{WE}}$  will not initiate a write cycle.

## **Logical Inhibit**

Writing is inhibited by holding any one of  $\overline{\text{OE}} = V_{IL}$ ,  $\overline{\text{CE}} = V_{IH}$ , or  $\overline{\text{WE}} = V_{IH}$ . To initiate a write cycle,  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  must be a logical zero while  $\overline{\text{OE}}$  is a logical one.

## **Power-up Write Inhibit**

Power-up of the device with  $\overline{\text{WE}} = \overline{\text{CE}} = V_{IL}$  and  $\overline{\text{OE}} = V_{IH}$  will not accept commands on the rising edge of  $\overline{\text{WE}}$ . The internal state machine is automatically reset to read mode on power-up.

## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value		Unit
		Min	Max	
Storage Temperature	T <sub>stg</sub>	−55	+ 125	°C
Ambient Temperature with Power Applied	T <sub>A</sub>	−40	+ 85	°C
Voltage with Respect to Ground. All pins except A <sub>9</sub> , $\overline{\text{OE}}$ , and $\overline{\text{RESET}}$ *1, *2	V <sub>IN</sub> , V <sub>OUT</sub>	−0.5	V <sub>CC</sub> + 0.5	V
Power Supply Voltage *1, *2	V <sub>CC</sub> , V <sub>CCQ</sub>	−0.5	+ 4.0	V
A <sub>9</sub> , $\overline{\text{OE}}$ , and $\overline{\text{RESET}}$ *1, *3	V <sub>IN</sub>	−0.5	+ 13.0	V
$\overline{\text{WP/ACC}}$ *1, *4	V <sub>ACC</sub>	−0.5	+ 10.5	V

\*1 : Voltage is defined on the basis of V<sub>SS</sub> = GND = 0V.

\*2 : Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, inputs or I/O pins may undershoot V<sub>SS</sub> to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V<sub>CC</sub> + 0.5 V. During voltage transitions, inputs may overshoot to V<sub>CC</sub> + 2.0 V for periods of up to 20 ns.

\*3 : Minimum DC input voltage on A<sub>9</sub>,  $\overline{\text{OE}}$ , and  $\overline{\text{RESET}}$  pins is −0.5 V. During voltage transitions, A<sub>9</sub>,  $\overline{\text{OE}}$ , and  $\overline{\text{RESET}}$  pins may undershoot V<sub>SS</sub> to −2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V<sub>IN</sub> − V<sub>CC</sub>) does not exceed + 9.0 V. Maximum DC input voltage on A<sub>9</sub>,  $\overline{\text{OE}}$  and  $\overline{\text{RESET}}$  pins is + 13.0 V which may overshoot to + 14.0 V for periods of up to 20 ns.

\*4 : Minimum DC input voltage on  $\overline{\text{WP/ACC}}$  pins is −0.5 V. During voltage transitions,  $\overline{\text{WP/ACC}}$  pin may undershoot V<sub>SS</sub> to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on  $\overline{\text{WP/ACC}}$  pin is + 10.5 V which may overshoot to + 12.0 V for periods of up to 20 ns when V<sub>CC</sub> is applied.

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING RANGES

Parameter	Symbol	Part No.	Value		Unit
			Min	Max	
Ambient Temperature	T <sub>A</sub>	MBM29QM96DF-65/80	−40	+ 85	°C
Power Supply Voltage *	V <sub>CC</sub>	MBM29QM96DF-65/80	+ 2.7	+ 3.1	V
V <sub>CCQ</sub> Supply Voltage *	V <sub>CCQ</sub>	MBM29QM96DF-65	+ 2.7	V <sub>CC</sub>	V
		MBM29QM96DF-80	+ 1.65	V <sub>CC</sub>	V

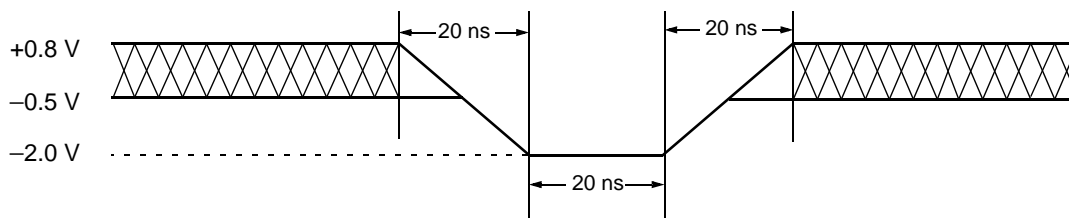
\* : Voltage is defined on the basis of V<sub>SS</sub> = GND = 0 V.

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

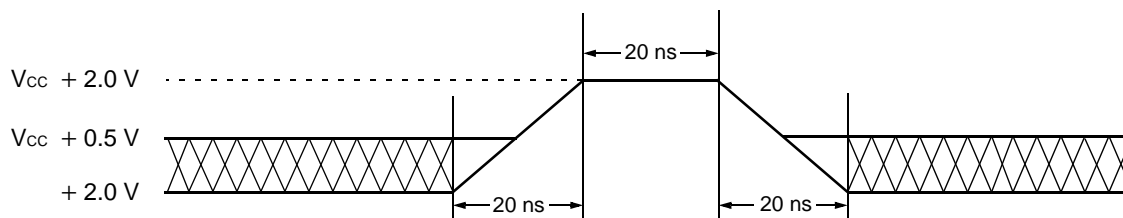
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

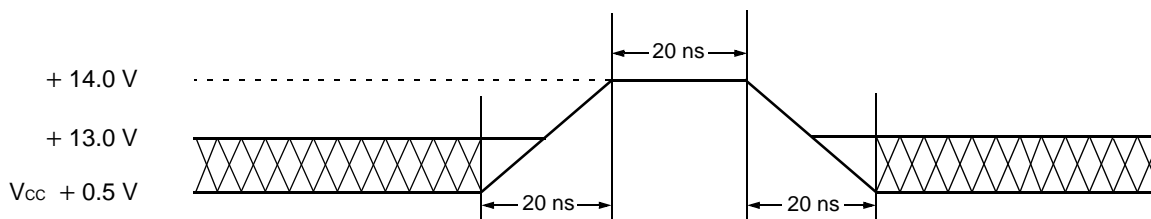
## ■ MAXIMUM OVERSHOOT / MAXIMUM UNDERSHOOT



**Figure 1** Maximum Undershoot Waveform



**Figure 2** Maximum Overshoot Waveform 1



**Note:** This waveform is applied for  $A_9$ ,  $\overline{OE}$ , and  $\overline{RESET}$ .

**Figure 3** Maximum Overshoot Waveform 2

## ■ DC CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Input Leakage Current	$I_{LI}$	$V_{IN} = V_{SSQ}$ to $V_{CCQ}$ , $V_{CC} = V_{CC} \text{ Max}$	-1.0	—	+ 1.0	$\mu\text{A}$
Output Leakage Current	$I_{LO}$	$V_{OUT} = V_{SSQ}$ to $V_{CCQ}$ , $V_{CC} = V_{CC} \text{ Max}$	-1.0	—	+ 1.0	$\mu\text{A}$
$A_9$ , $\overline{OE}$ , $\overline{RESET}$ Inputs Leakage Current	$I_{LIT}$	$V_{CC} = V_{CC} \text{ Max}$ , $A_9$ , $\overline{OE}$ , $\overline{RESET} = 12.5 \text{ V}$	—	—	35	$\mu\text{A}$
$\overline{WP}/\text{ACC}$ Accelerated Program Current	$I_{LIA}$	$V_{CC} = V_{CC} \text{ Max}$ , $\overline{WP}/\text{ACC} = V_{ACC} \text{ Max}$	—	—	20	mA
$V_{CC}$ Active Current *1 (Initial/Random Read)	$I_{CC1}$	$\overline{CE} = V_{IL}$ , $\overline{OE} = V_{IH}$ , $f = 10 \text{ MHz}$	—	—	45	mA
		$\overline{CE} = V_{IL}$ , $\overline{OE} = V_{IH}$ , $f = 5 \text{ MHz}$	—	—	20	mA
$V_{CC}$ Active Current *2	$I_{CC2}$	$\overline{CE} = V_{IL}$ , $\overline{OE} = V_{IH}$	—	—	25	mA
$V_{CC}$ Current (Standby)	$I_{CC3}$	$V_{CC} = V_{CC} \text{ Max}$ , $\overline{CE} = V_{CCQ} \pm 0.3 \text{ V}$ , $\overline{RESET} = V_{CCQ} \pm 0.3 \text{ V}$ , $\overline{WP}/\text{ACC} = V_{CCQ} \pm 0.3 \text{ V}$	—	1	5	$\mu\text{A}$
$V_{CC}$ Current (Standby, Reset)	$I_{CC4}$	$V_{CC} = V_{CC} \text{ Max}$ , $\overline{RESET} = V_{SSQ} \pm 0.3 \text{ V}$	—	1	5	$\mu\text{A}$
$V_{CC}$ Current (Page Mode) *3	$I_{CC5}$	$\overline{CE} = V_{IL}$ , $\overline{OE} = V_{IH}$ , $f = 40 \text{ MHz}$	—	—	5	mA
$V_{CC}$ Current (Automatic Sleep Mode) *4	$I_{CC6}$	$V_{CC} = V_{CC} \text{ Max}$ , $\overline{CE} = V_{SS} \pm 0.3 \text{ V}$ , $V_{IN} = V_{CCQ} \pm 0.3 \text{ V}$ or $V_{SSQ} \pm 0.3 \text{ V}$	—	1	5	$\mu\text{A}$
$V_{CC}$ Active Current*5 (Read-While-Program)	$I_{CC7}$	$\overline{CE} = V_{IL}$ , $\overline{OE} = V_{IH}$	—	—	45	mA
$V_{CC}$ Active Current*5 (Read-While-Erase)	$I_{CC8}$	$\overline{CE} = V_{IL}$ , $\overline{OE} = V_{IH}$	—	—	45	mA
$V_{CC}$ Active Current*5 (Erase-Suspend-Program)	$I_{CC9}$	$\overline{CE} = V_{IL}$ , $\overline{OE} = V_{IH}$	—	—	25	mA
Input Low Voltage	$V_{IL}$	—	-0.5	—	0.6	V
Input High Voltage	$V_{IH}$	—	$V_{CCQ} - 0.2$	—	$V_{CCQ} + 0.3$	V
Voltage for Auteselect and Sector Protection( $A_9$ , $\overline{OE}$ , $\overline{RESET}$ )*6	$V_{ID}$	—	11.5	12.0	12.5	V
Voltage for $\overline{WP}/\text{ACC}$ Sector Protection/Unprotection and Program Acceleration	$V_{ACC}$	—	8.5	9.0	9.5	V
Output Low Voltage	$V_{OL1}$	$I_{OL} = 4.0 \text{ mA}$ , $V_{CC} = V_{CC} \text{ Min}$	—	—	0.3	V
	$V_{OL2}$	$I_{OL} = 100 \mu\text{A}$ , $V_{CC} = V_{CC} \text{ Min}$	—	—	0.1	V
Output High Voltage	$V_{OH1}$	$I_{OH} = -2.0 \text{ mA}$ , $V_{CC} = V_{CC} \text{ Min}$	$V_{CCQ} - 0.3$	—	—	V
	$V_{OH2}$	$I_{OH} = -100 \mu\text{A}$ , $V_{CC} = V_{CC} \text{ Min}$	$V_{CCQ} - 0.2$	—	—	V
Low $V_{CC}$ Lock-Out Voltage	$V_{LKO}$	—	2.3	2.4	2.5	V

\*1 :  $I_{CC}$  current listed includes both the DC operating current and the frequency dependent component.

\*2 :  $I_{CC}$  active while Embedded Algorithm (Program or Erase) is in progress.

\*3 : Addresses except  $A_2$ ,  $A_1$ ,  $A_0$  are fixed.

\*4 : Automatic sleep mode enables the low power mode when address remain stable for 150 ns.

\*5 : Embedded Algorithm (Program or Erase) is in progress.(@5 MHz)

\*6 :  $V_{ID}$  is only for Sector Group Protection operation and Autoselect mode.

## ■ AC CHARACTERISTICS

- Read Only Operations Characteristics

Parameter	Symbol		Condition	Value *				Unit
				65		80		
	JEDEC	Standard		Min	Max	Min	Max	
Read Cycle Time	t <sub>AVAV</sub>	t <sub>RC</sub>	—	65	—	80	—	ns
Address to Output Delay	t <sub>AVQV</sub>	t <sub>ACC</sub>	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	—	65	—	80	ns
Page Read Cycle Time	—	t <sub>PRC</sub>	—	25	—	30	—	ns
Page Address to Output Delay	—	t <sub>PACC</sub>	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	—	25	—	30	ns
Chip Enable to Output Delay	t <sub>ELQV</sub>	t <sub>CE</sub>	$\overline{OE} = V_{IL}$	—	65	—	80	ns
Output Enable to Output Delay	t <sub>GLQV</sub>	t <sub>OE</sub>	—	—	25	—	30	ns
Chip Enable to Output High-Z	t <sub>EHQZ</sub>	t <sub>DF</sub>	—	—	25	—	30	ns
Output Enable to Output High-Z	t <sub>GHQZ</sub>	t <sub>DF</sub>	—	—	25	—	30	ns
Output Hold Time From Address, $\overline{CE}$ or $\overline{OE}$ , Whichever Occurs First	t <sub>AXQX</sub>	t <sub>OH</sub>	—	4	—	4	—	ns
$\overline{RESET}$ Pin Low to Read Mode	—	t <sub>READY</sub>	—	—	20	—	20	ns

Note : \*Test Conditions:

Output Load:  $V_{CCQ} = 1.65\text{ V to }2.7\text{ V} : 30\text{pF}$

$V_{CCQ} = 2.7\text{ V to }3.1\text{ V} : 1\text{ TTL gate and }30\text{pF (MBM29QM96DF-65)}$

1 TTL gate and 100pF (MBM29QM96DF-80)

Input rise and fall times: 5 ns

Input pulse levels: 0.0 V or  $V_{CCQ}$

Timing measurement reference level

Input:  $0.5 \times V_{CCQ}$

Output:  $0.5 \times V_{CCQ}$

• Write (Erase/Program) Operations

Parameter		Symbol		Value						Unit
				65			80			
		JEDEC	Standard	Min	Typ	Max	Min	Typ	Max	
Write Cycle Time		t <sub>AVAV</sub>	t <sub>WC</sub>	65	—	—	80	—	—	ns
Address Setup Time		t <sub>AVWL</sub>	t <sub>AS</sub>	0	—	—	0	—	—	ns
Address Setup Time to $\overline{\text{OE}}$ Low During Toggle Bit Polling		—	t <sub>ASO</sub>	12	—	—	12	—	—	ns
Address Hold Time		t <sub>WLAX</sub>	t <sub>AH</sub>	45	—	—	45	—	—	ns
Address Hold Time from $\overline{\text{CE}}$ or $\overline{\text{OE}}$ High During Toggle Bit Polling		—	t <sub>AHT</sub>	0	—	—	0	—	—	ns
Data Setup Time		t <sub>DVWH</sub>	t <sub>DS</sub>	35	—	—	35	—	—	ns
Data Hold Time		t <sub>WHDX</sub>	t <sub>DH</sub>	0	—	—	0	—	—	ns
Output Enable Hold Time	Read	—	t <sub>OEh</sub>	0	—	—	0	—	—	ns
	Toggle and $\overline{\text{Data}}$ Polling			10	—	—	10	—	—	ns
$\overline{\text{CE}}$ High During Toggle Bit Polling		—	t <sub>CEPH</sub>	20	—	—	20	—	—	ns
$\overline{\text{OE}}$ High During Toggle Bit Polling		—	t <sub>OEPh</sub>	20	—	—	20	—	—	ns
Read Recover Time Before Write		t <sub>GHWL</sub>	t <sub>GHWL</sub>	0	—	—	0	—	—	ns
Read Recover Time Before Write		t <sub>GHEL</sub>	t <sub>GHEL</sub>	0	—	—	0	—	—	ns
$\overline{\text{CE}}$ Setup Time		t <sub>ELWL</sub>	t <sub>CS</sub>	0	—	—	0	—	—	ns
$\overline{\text{WE}}$ Setup Time		t <sub>WLEL</sub>	t <sub>WS</sub>	0	—	—	0	—	—	ns
$\overline{\text{CE}}$ Hold Time		t <sub>WHEH</sub>	t <sub>CH</sub>	0	—	—	0	—	—	ns
$\overline{\text{WE}}$ Hold Time		t <sub>EHWH</sub>	t <sub>WH</sub>	0	—	—	0	—	—	ns
Write Pulse Width		t <sub>WLWH</sub>	t <sub>WP</sub>	35	—	—	35	—	—	ns
$\overline{\text{CE}}$ Pulse Width		t <sub>ELEH</sub>	t <sub>CP</sub>	35	—	—	35	—	—	ns
Write Pulse Width High		t <sub>WHWL</sub>	t <sub>WPH</sub>	30	—	—	30	—	—	ns
$\overline{\text{CE}}$ Pulse Width High		t <sub>EHEL</sub>	t <sub>CPH</sub>	30	—	—	30	—	—	ns
Word Programming Operation		t <sub>WHWH1</sub>	t <sub>WHWH1</sub>	—	6	—	—	6	—	μs
Sector Erase Operation* <sup>1</sup>		t <sub>WHWH2</sub>	t <sub>WHWH2</sub>	—	0.5	—	—	0.5	—	s
V <sub>CC</sub> Setup Time		—	t <sub>VCS</sub>	50	—	—	50	—	—	μs
Rise Time to V <sub>ID</sub> * <sup>2</sup>		—	t <sub>VIDR</sub>	500	—	—	500	—	—	ns
Rise Time to V <sub>ACC</sub> * <sup>3</sup>		—	t <sub>VACCR</sub>	500	—	—	500	—	—	ns
Voltage Transition Time * <sup>2</sup>		—	t <sub>VLHT</sub>	4	—	—	4	—	—	μs
Write Pulse Width* <sup>2</sup>		—	t <sub>WPP</sub>	100	—	—	100	—	—	μs
$\overline{\text{OE}}$ Setup Time to $\overline{\text{WE}}$ Active* <sup>2</sup>		—	t <sub>OESP</sub>	4	—	—	4	—	—	μs
$\overline{\text{CE}}$ Setup Time to $\overline{\text{WE}}$ Active* <sup>2</sup>		—	t <sub>CSP</sub>	4	—	—	4	—	—	μs

(Continued)

(Continued)

Parameter	Symbol		Value						Unit
			65			80			
	JEDEC	Standard	Min	Typ	Max	Min	Typ	Max	
Recover Time from RY/ $\overline{\text{BY}}$	—	t <sub>RB</sub>	0	—	—	0	—	—	ns
$\overline{\text{RESET}}$ Pulse Width	—	t <sub>RP</sub>	500	—	—	500	—	—	ns
$\overline{\text{RESET}}$ High Level Period Before Read	—	t <sub>RH</sub>	200	—	—	200	—	—	ns
Program/Erase Valid to RY/ $\overline{\text{BY}}$ Delay	—	t <sub>BUSY</sub>	—	—	90	—	—	90	ns
Delay Time from Embedded Output Enable	—	t <sub>EOE</sub>	—	—	65	—	—	80	ns
Erase Time-out Time	—	t <sub>TOW</sub>	50	—	—	50	—	—	μs
Erase Suspend Transition Time	—	t <sub>SPD</sub>	—	—	20	—	—	20	μs

\*1 : This does not include the preprogramming time.

\*2 : This timing is for Sector Group Protection operation.

\*3 : This timing is limited for Accelerated Program operation only.



## ■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Value			Unit	Comments
	Min	Typ	Max		
Sector Erase Time	—	0.5	2.0	s	Excludes programming time prior to erase
Word Programming Time	—	6	100	μs	Excludes system-level overhead
Chip Programming Time	—	37.7	150	s	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycle	—

Note : Typical Erase Conditions:  $T_A = +25\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 2.9\text{ V}$   
 Typical Program Conditions:  $T_A = +25\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 2.9\text{ V}$ , Data = Checker





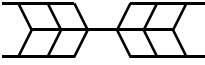
## ■ FBGA PIN CAPACITANCE

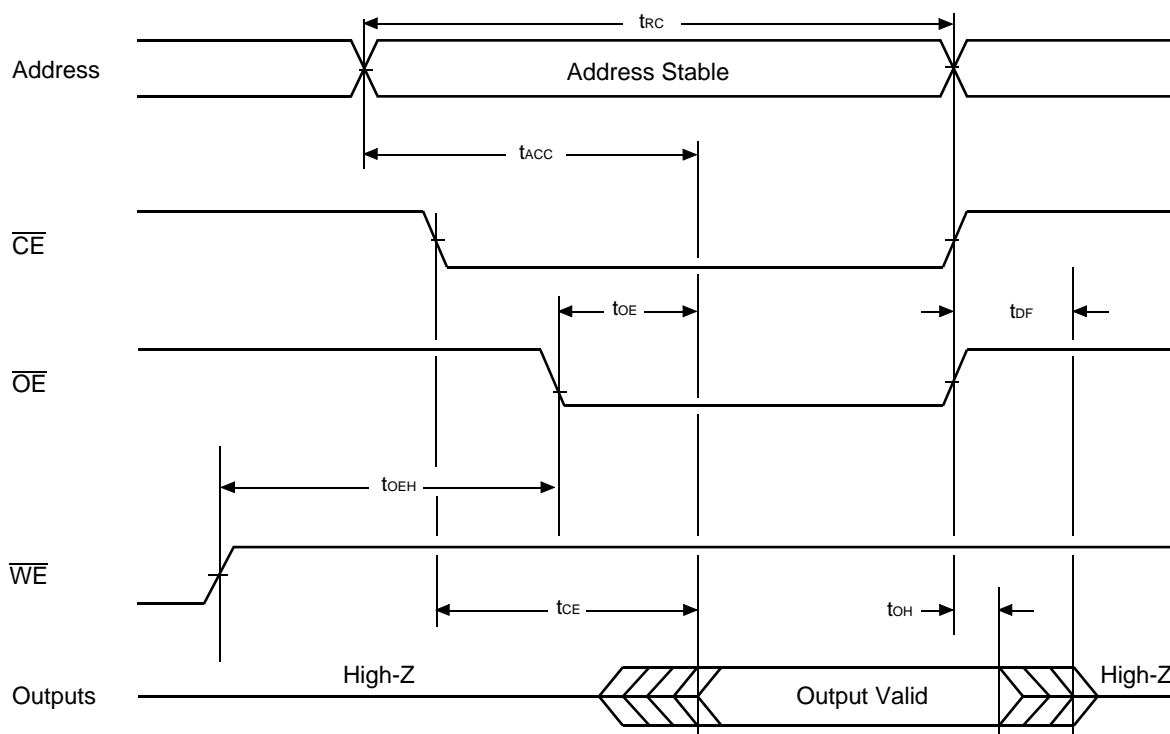
Parameter	Symbol	Test Setup	Typ	Max	Unit
Input Capacitance	$C_{IN}$	$V_{IN} = 0$	7.0	10.0	pF
Output Capacitance	$C_{OUT}$	$V_{OUT} = 0$	6.0	12.0	pF
Control Pin Capacitance	$C_{IN2}$	$V_{IN} = 0$	7.5	11.0	pF
$\overline{WP}/ACC$ Pin Capacitance	$C_{IN3}$	$V_{IN} = 0$	10.0	12.0	pF

Note : Test Conditions:  $T_A = +25\text{ }^{\circ}\text{C}$ ,  $f = 1.0\text{ MHz}$

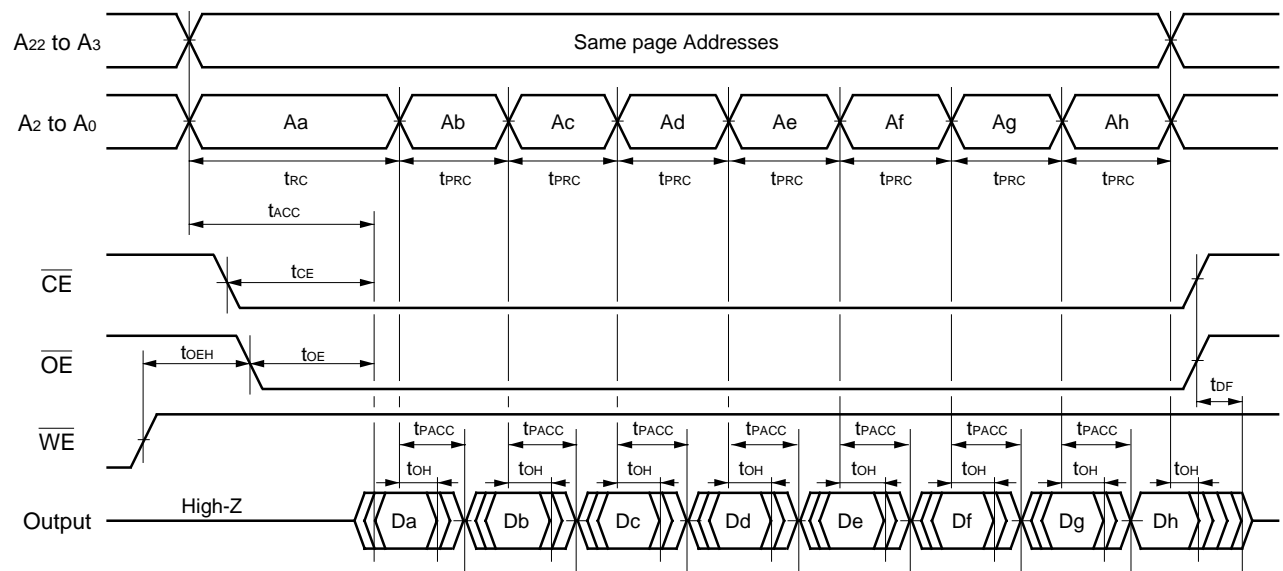
## SWITCHING WAVEFORMS

- Key to Switching Waveforms

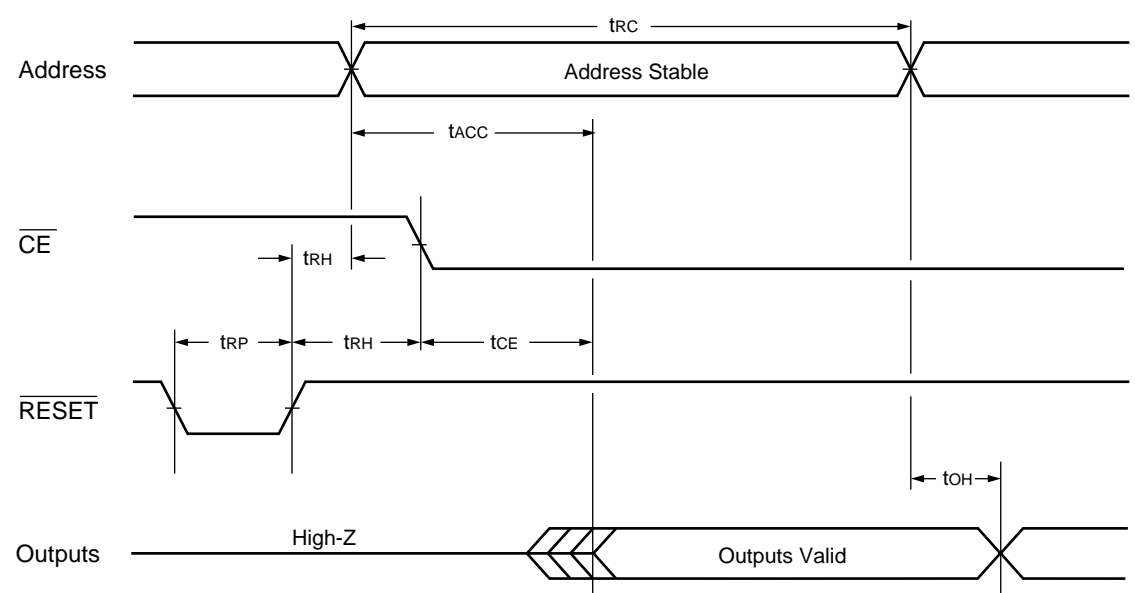
WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Change from H to L
	May Change from L to H	Will Be Change from L to H
	"H" or "L": Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State



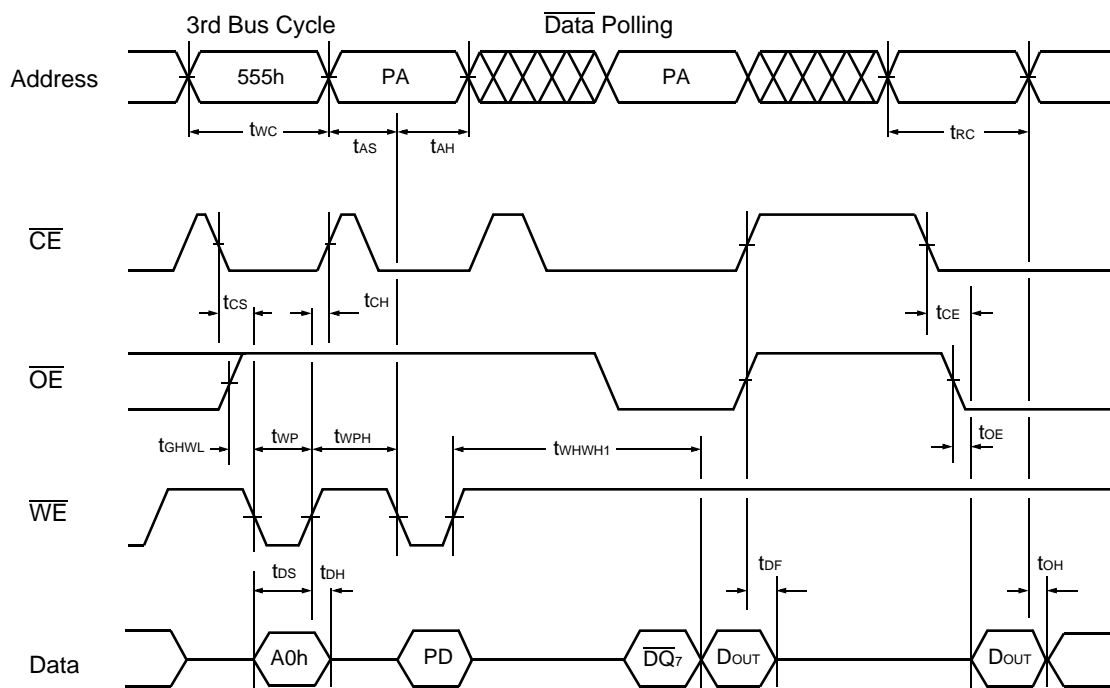
Read Operation Timing Diagram



Page Read Operation Timing Diagram

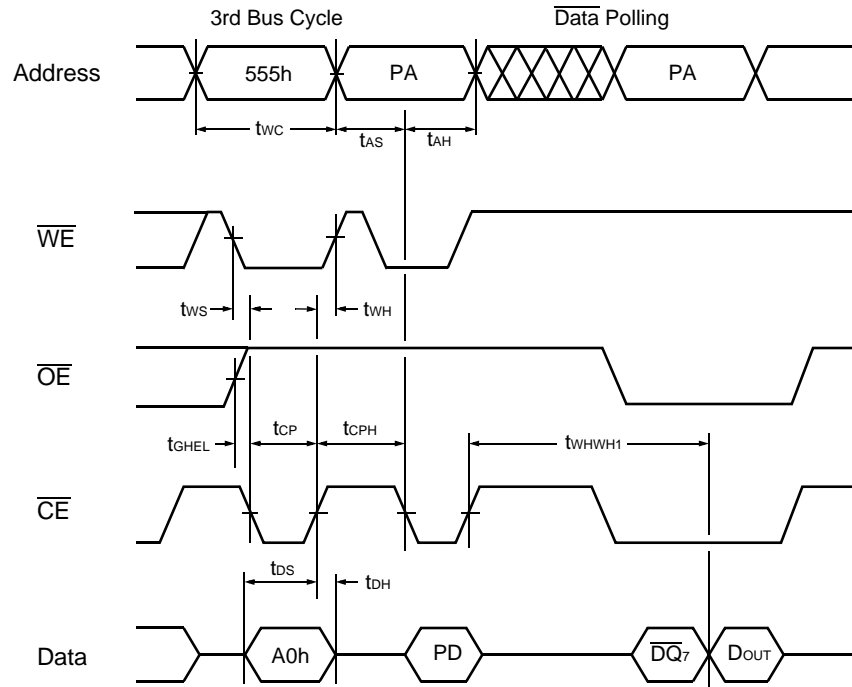


Hardware Reset/Read Operation Timing Diagram



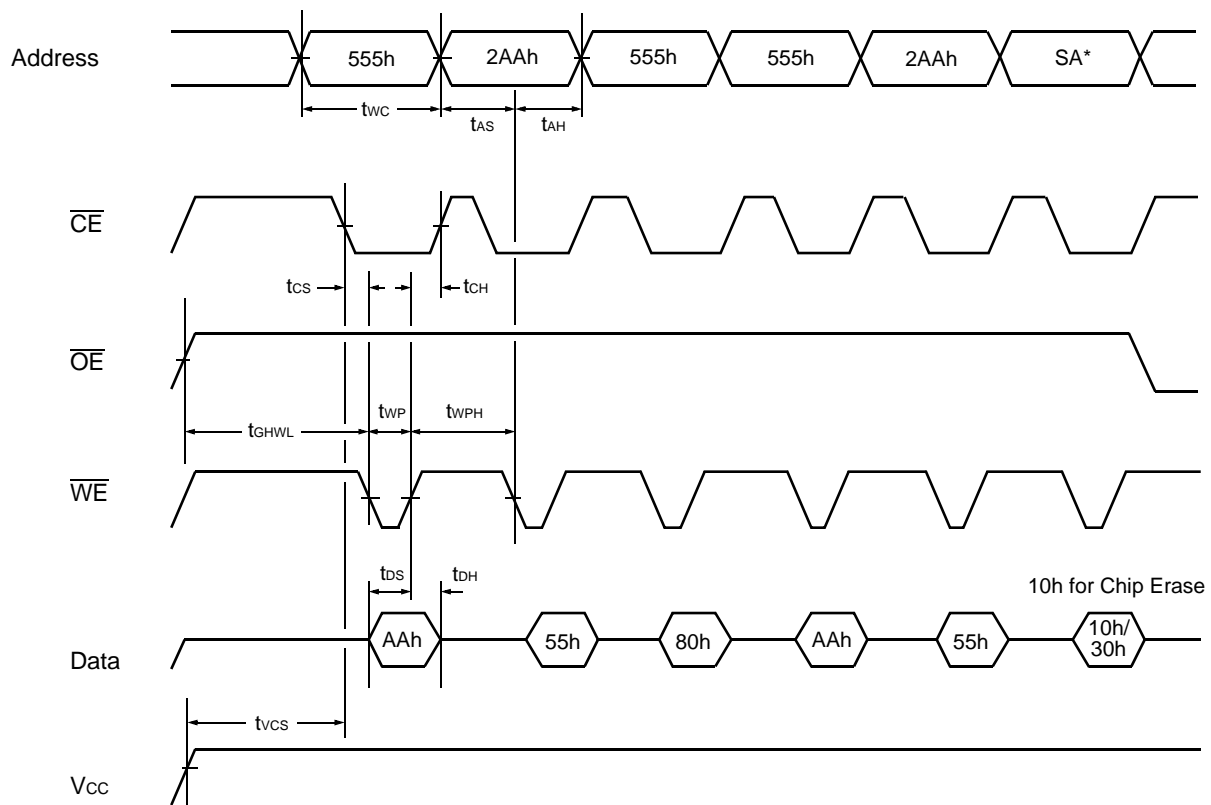
- Notes :
- PA is address of the memory location to be programmed.
  - PD is data to be programmed at word address.
  - $\overline{DQ_7}$  is the output of the complement of the data written to the device.
  - DOUT is the output of the data written to the device.
  - Figure indicates last two bus cycles out of four bus cycle sequence.

Alternate  $\overline{WE}$  Controlled Program Operation Timing Diagram



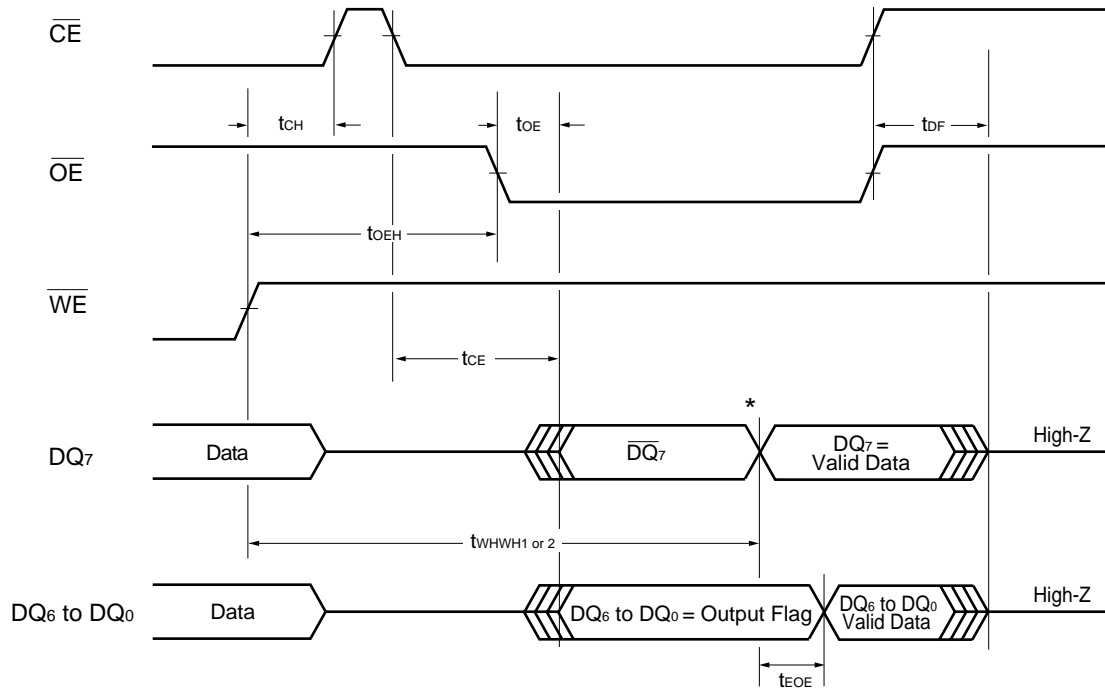
- Notes :
- PA is address of the memory location to be programmed.
  - PD is data to be programmed at word address.
  - $\overline{DQ_7}$  is the output of the complement of the data written to the device.
  - DOUT is the output of the data written to the device.
  - Figure indicates last two bus cycles out of four bus cycle sequence.

Alternate  $\overline{CE}$  Controlled Program Operation Timing Diagram



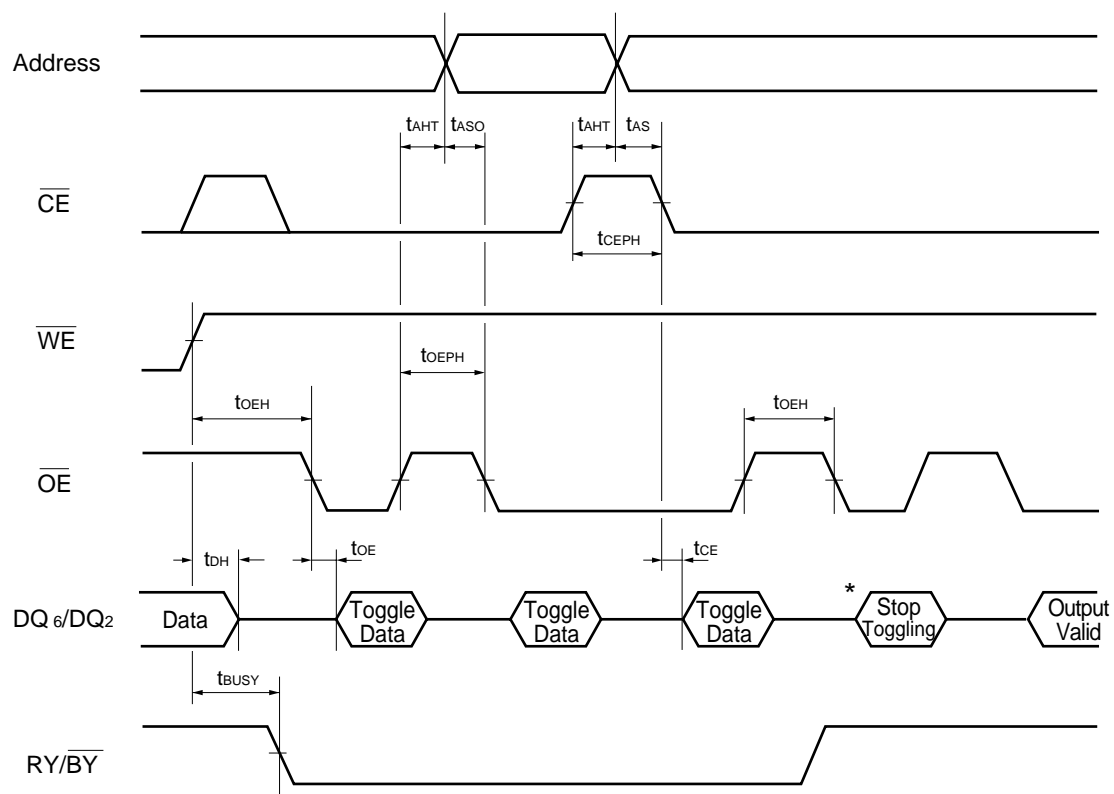
\* : SA is the sector address for Sector Erase. Address = 555h for Chip Erase.

Chip/Sector Erase Operation Timing Diagram



\* : DQ<sub>7</sub> = Valid Data (The device has completed the Embedded operation.)

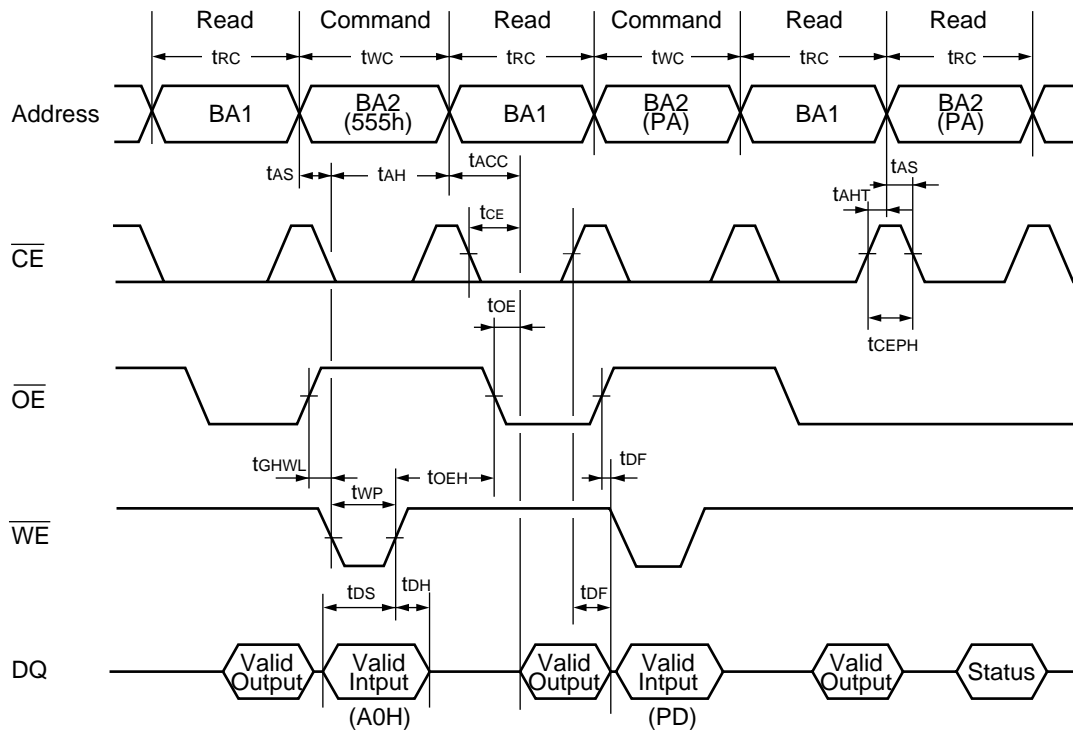
Data Polling during Embedded Algorithm Operation Timing Diagram



\* : DQ<sub>6</sub> stops toggling (The device has completed the Embedded operation.)

AC Waveforms for Toggle Bit I during Embedded Algorithm Operations



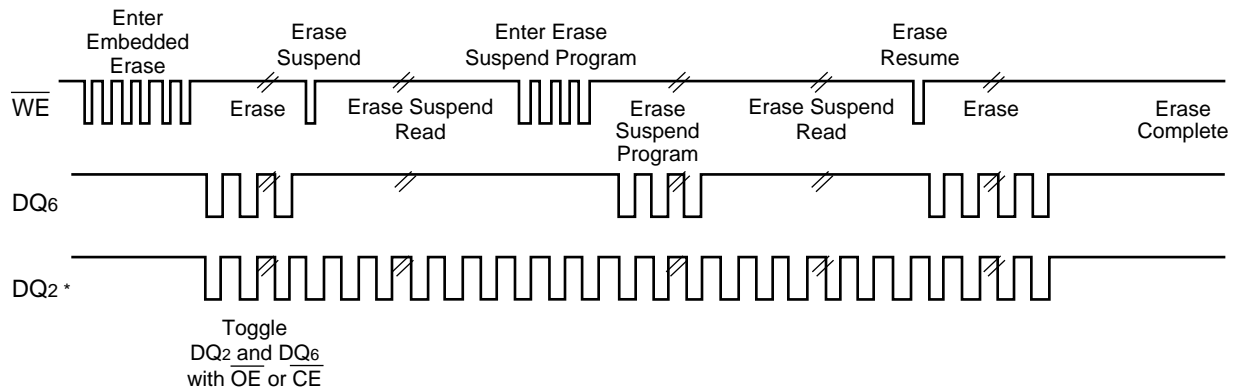


Note : This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.

BA1 : Address corresponding to Bank 1

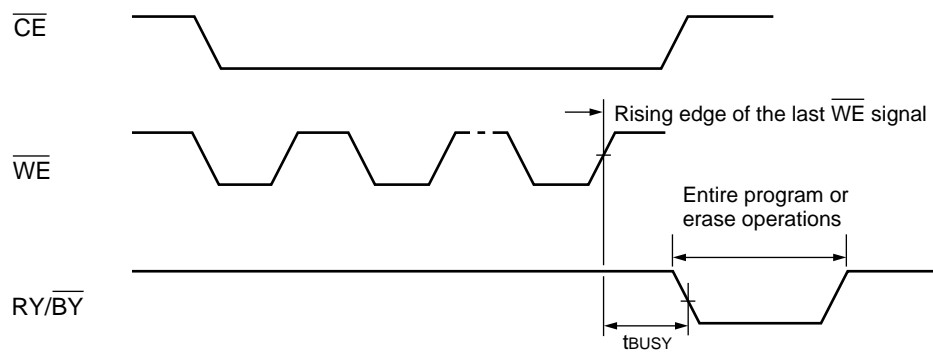
BA2 : Address corresponding to Bank 2

Bank-to-Bank Read / Write(Program and Erase) Timing Diagram

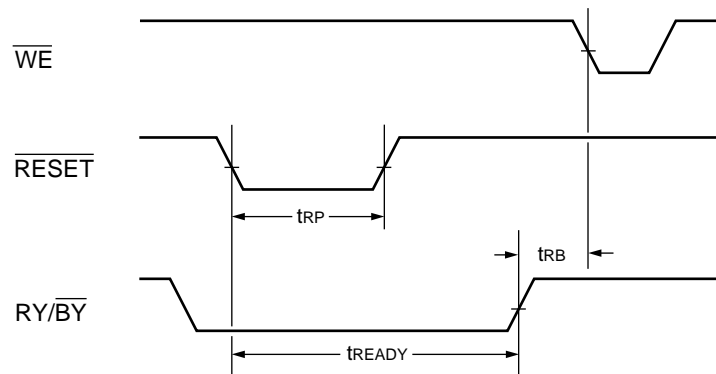


\* : DQ2 is read from the erase-suspended sector.

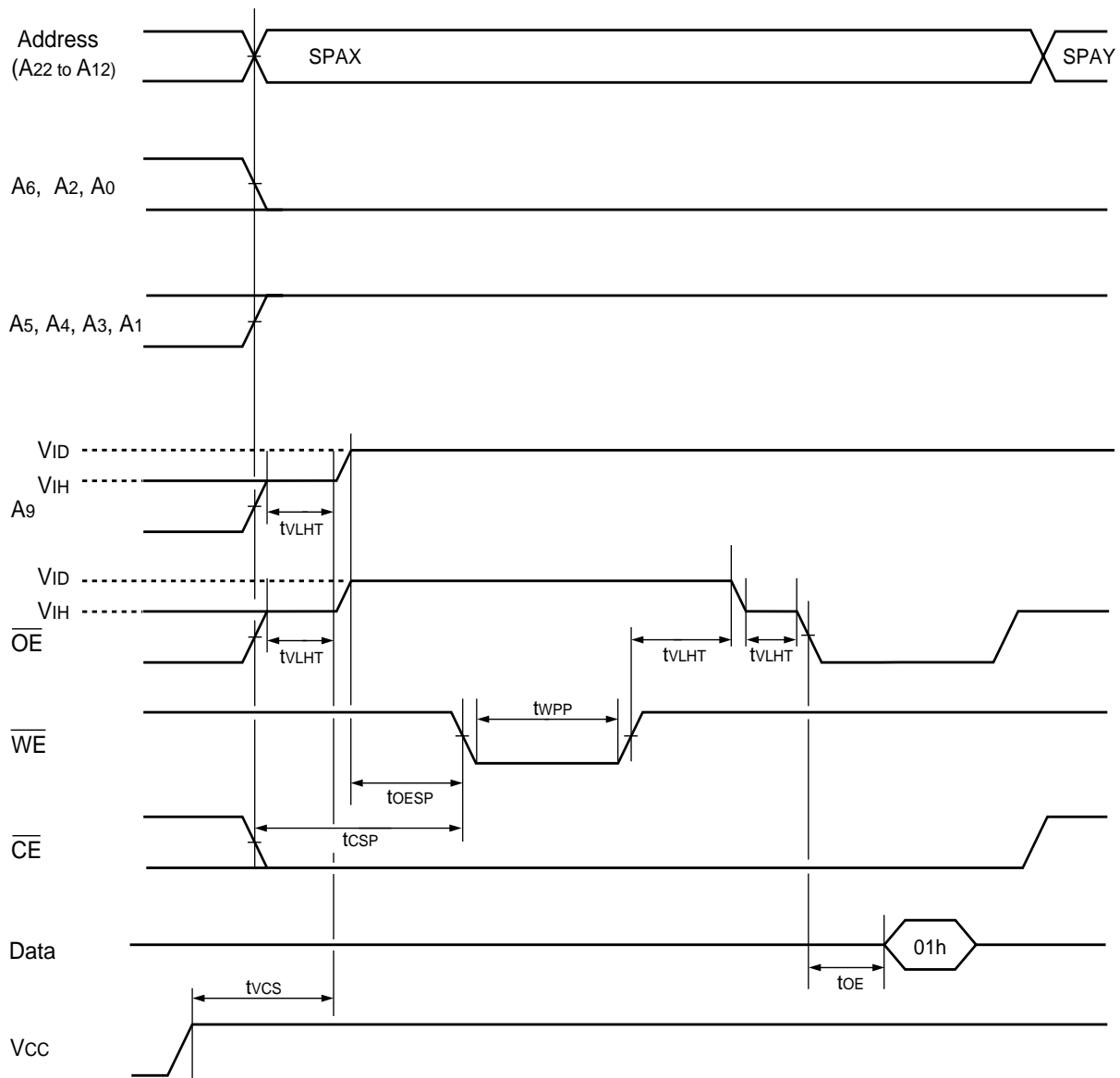
DQ2 vs. DQ6



$\overline{RY/BY}$  Timing Diagram during Program/Erase Operation Timing Diagram

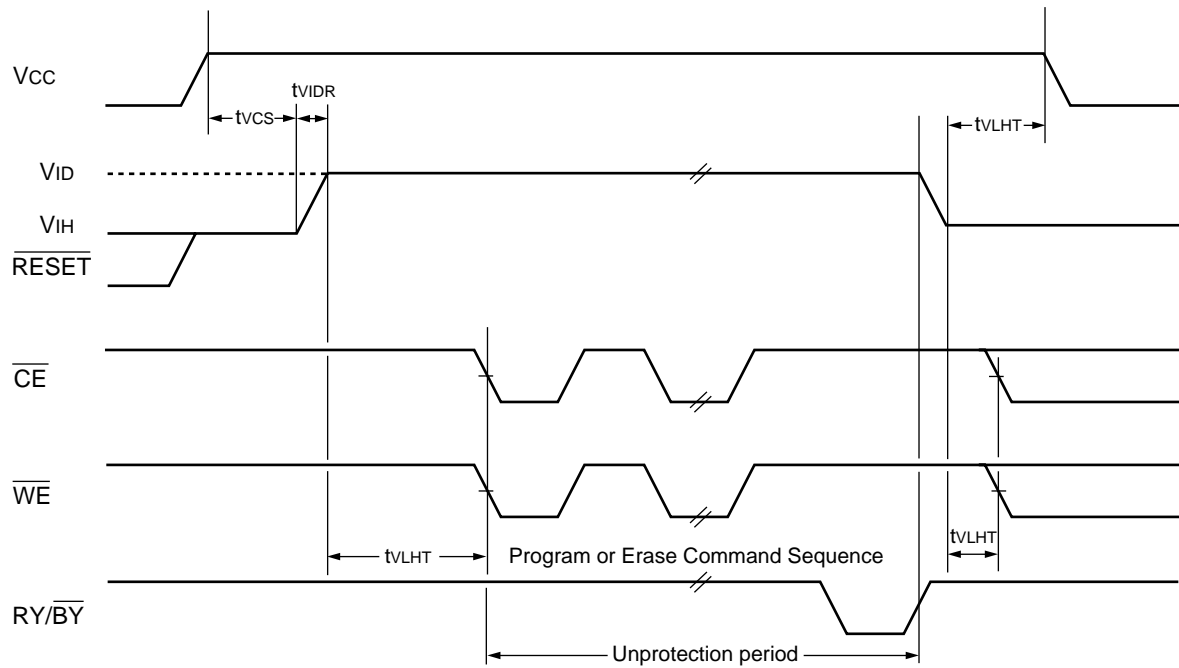


$\overline{RESET}$ ,  $\overline{RY/BY}$  Timing Diagram

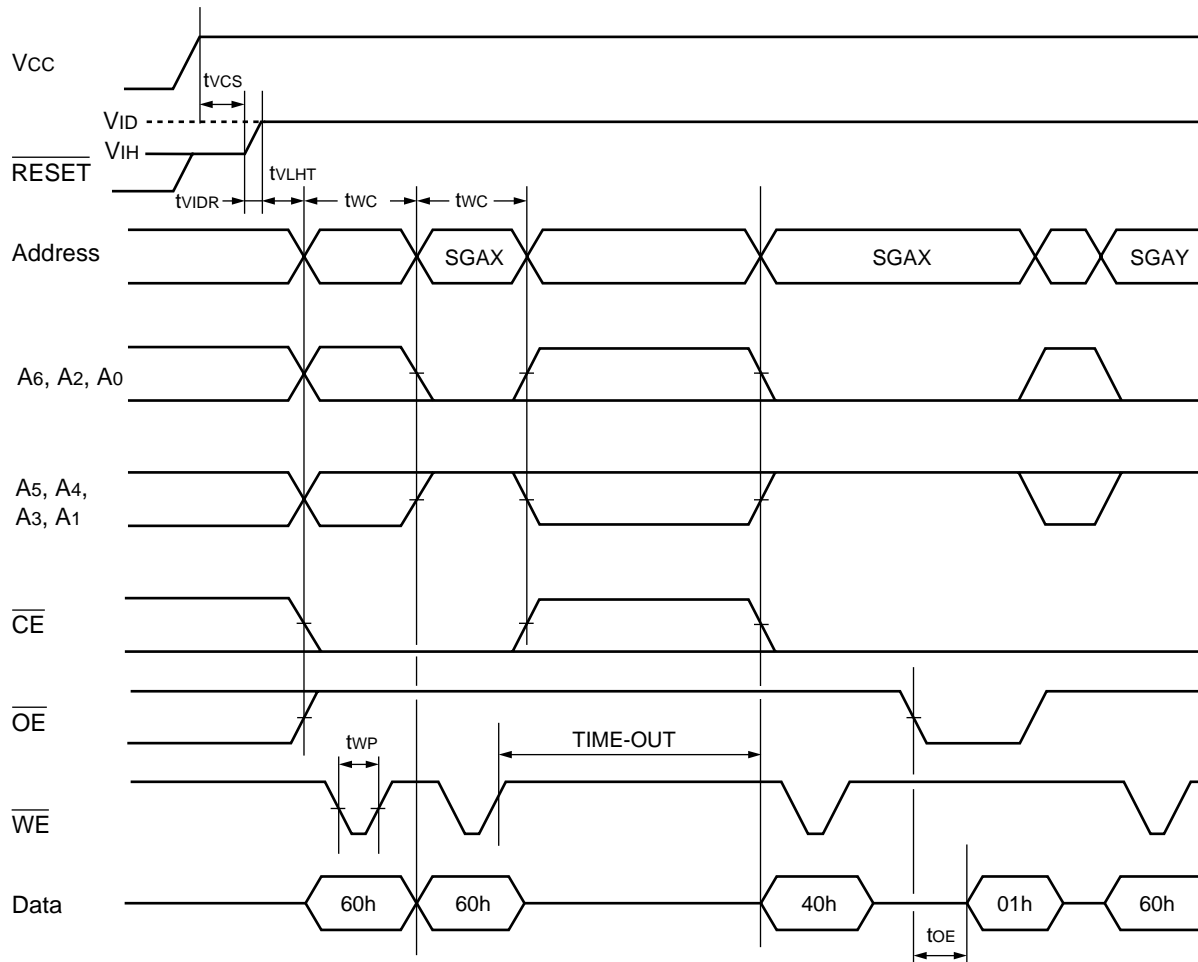


SPAX : Sector Group Address to be protected  
 SPAY : Next Sector Group Address to be protected

Sector Group Protection Timing Diagram

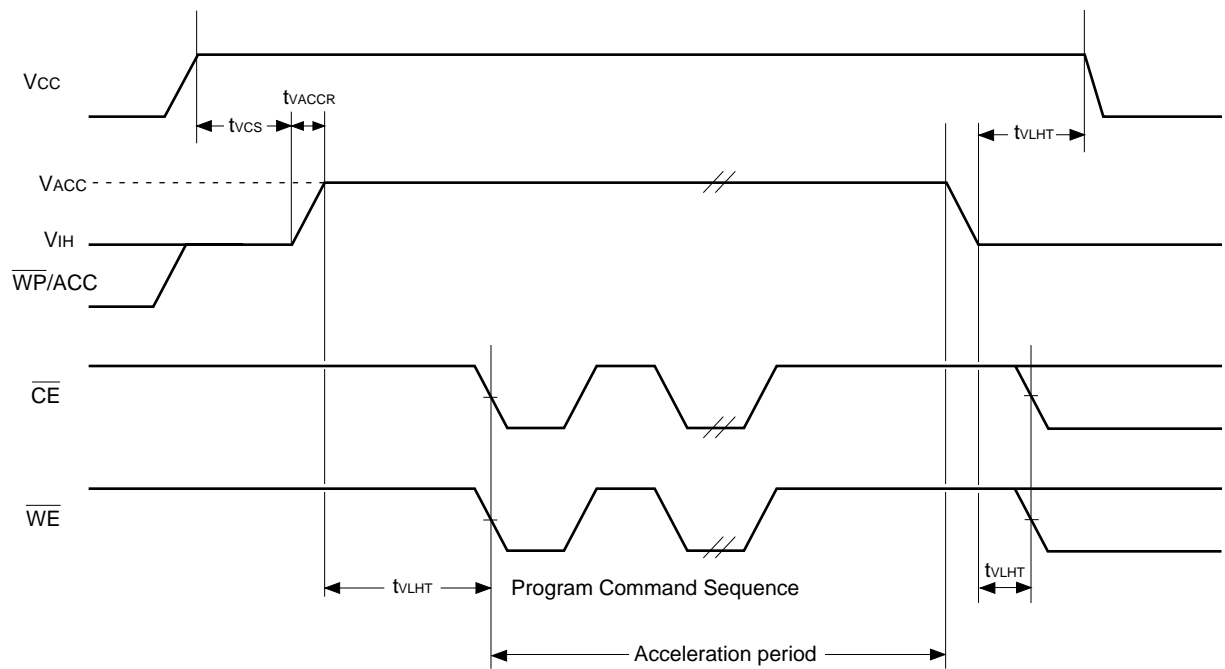


Temporary Sector Group Unprotection Timing Diagram



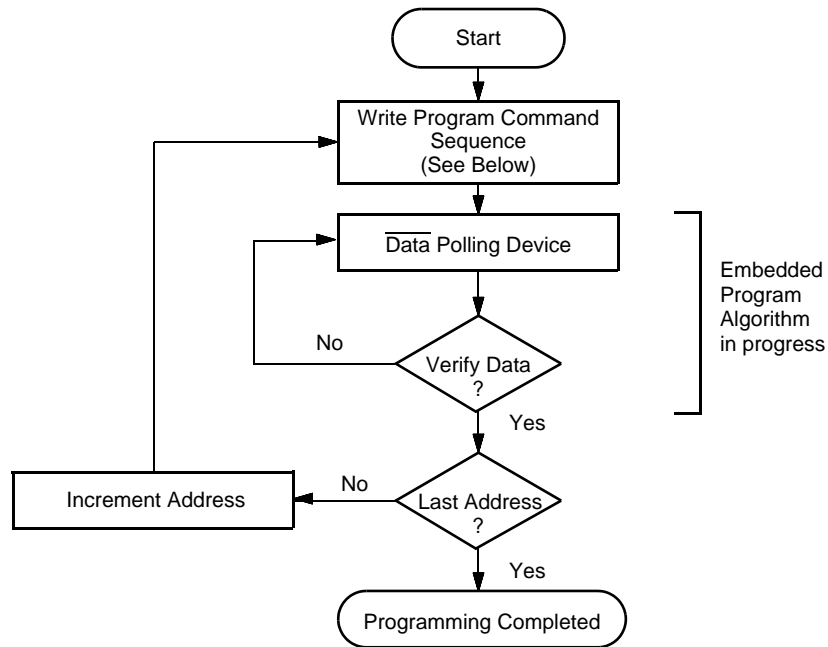
SGAX : Sector Group Address to be protected  
 SGAY : Next Sector Group Address to be protected  
 TIME-OUT : Time-Out window = 250  $\mu$ s (Min)

Extended Sector Group Protection Timing Diagram

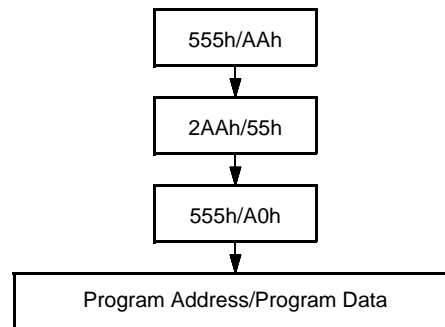


Accelerated Program Timing Diagram

## EMBEDDED ALGORITHM

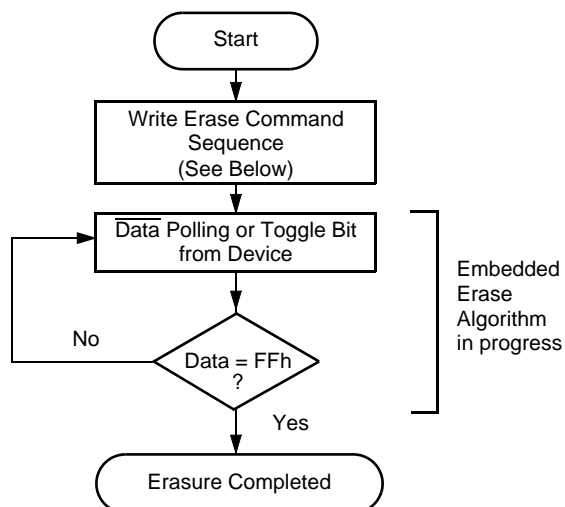


### Program Command Sequence (Address/Command):

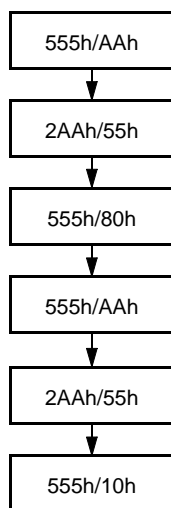


Embedded Program™ Algorithm

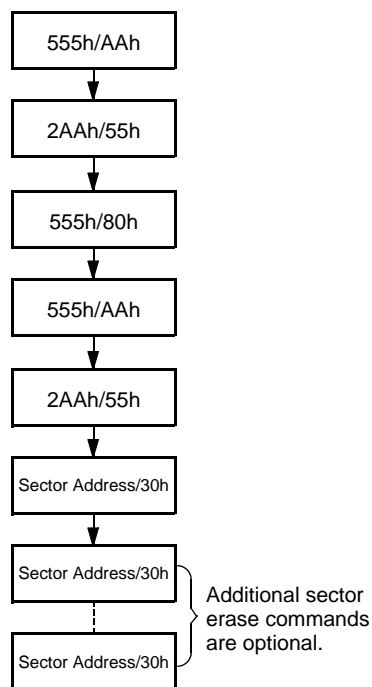
## EMBEDDED ALGORITHM



### Chip Erase Command Sequence (Address/Command):

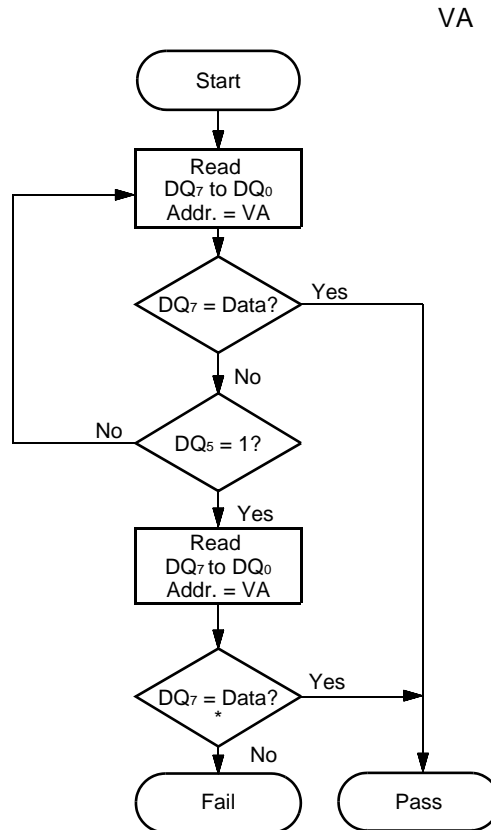


### Individual Sector/Multiple Sector Erase Command Sequence (Address/Command):



Embedded Erase™ Algorithm

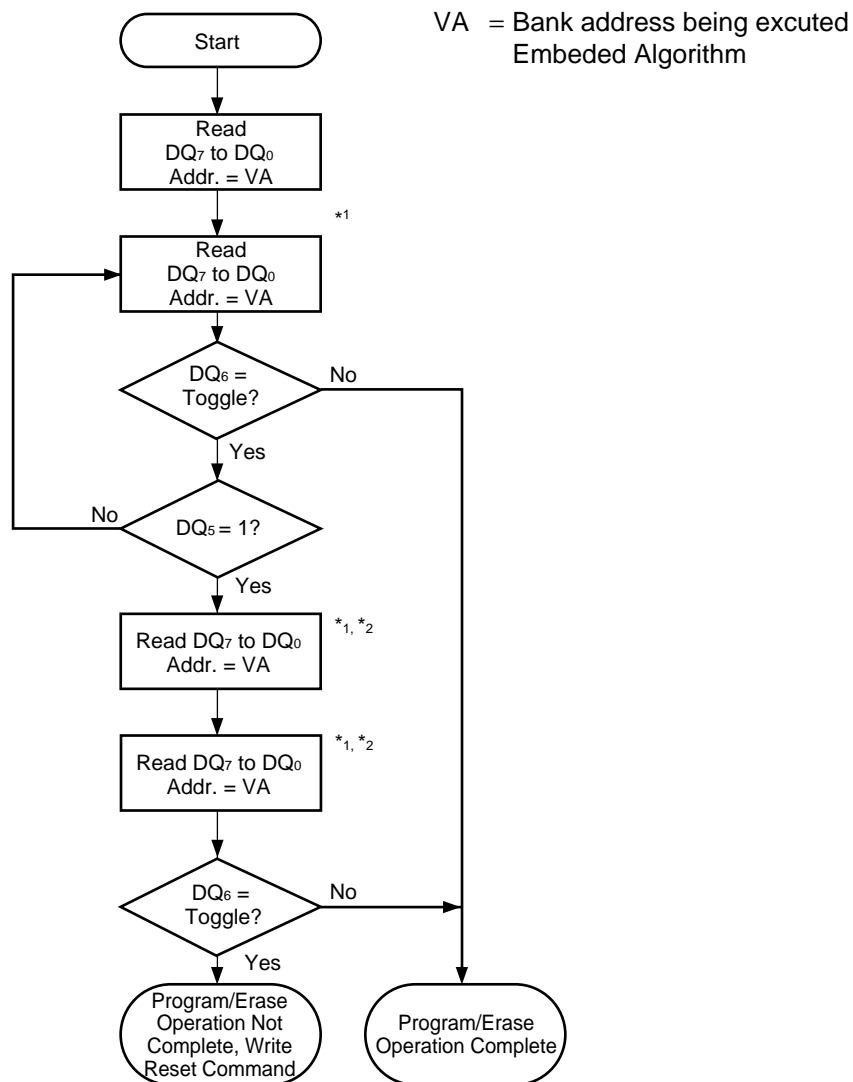




VA = Address for programming  
 = Any of the sector addresses within the sector being erased during sector erase or multiple sector erase operation.  
 = Any of the sector addresses within the sector not being protected during chip erase operation.

\* : DQ<sub>7</sub> is rechecked even if DQ<sub>5</sub> = "1" because DQ<sub>7</sub> may change simultaneously with DQ<sub>5</sub>.

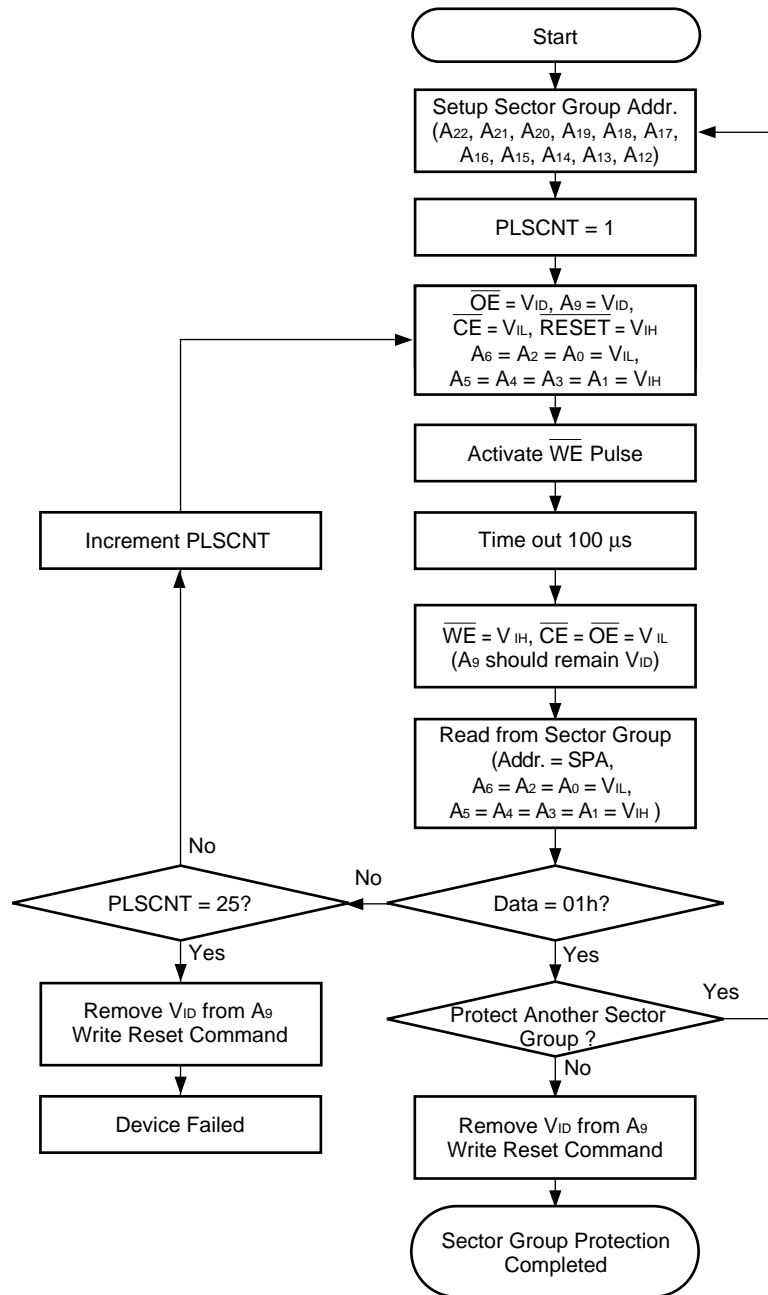
Data Polling Algorithm



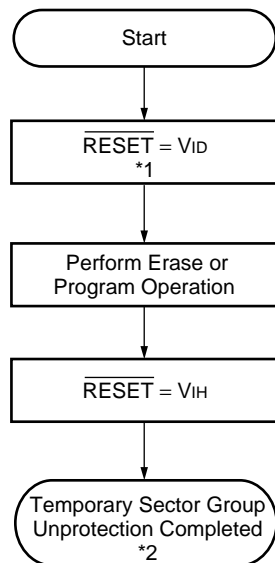
\*1 : Read toggle bit twice to determine whether it is toggling.

\*2 : Recheck toggle bit because it may stop toggling as DQ<sub>5</sub> changes to "1".

Toggle Bit Algorithm



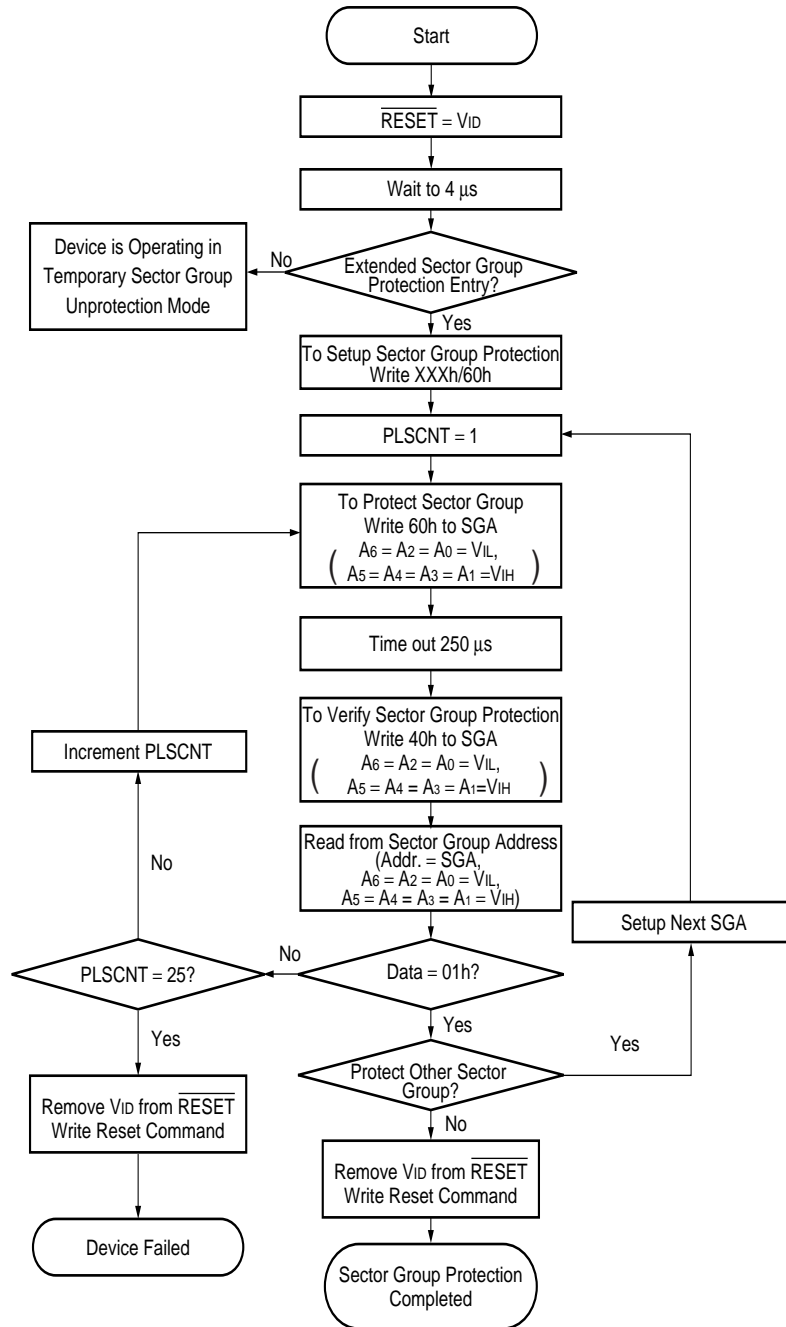
Sector Group Protection Algorithm



\*1 : All protected sector groups are unprotected.

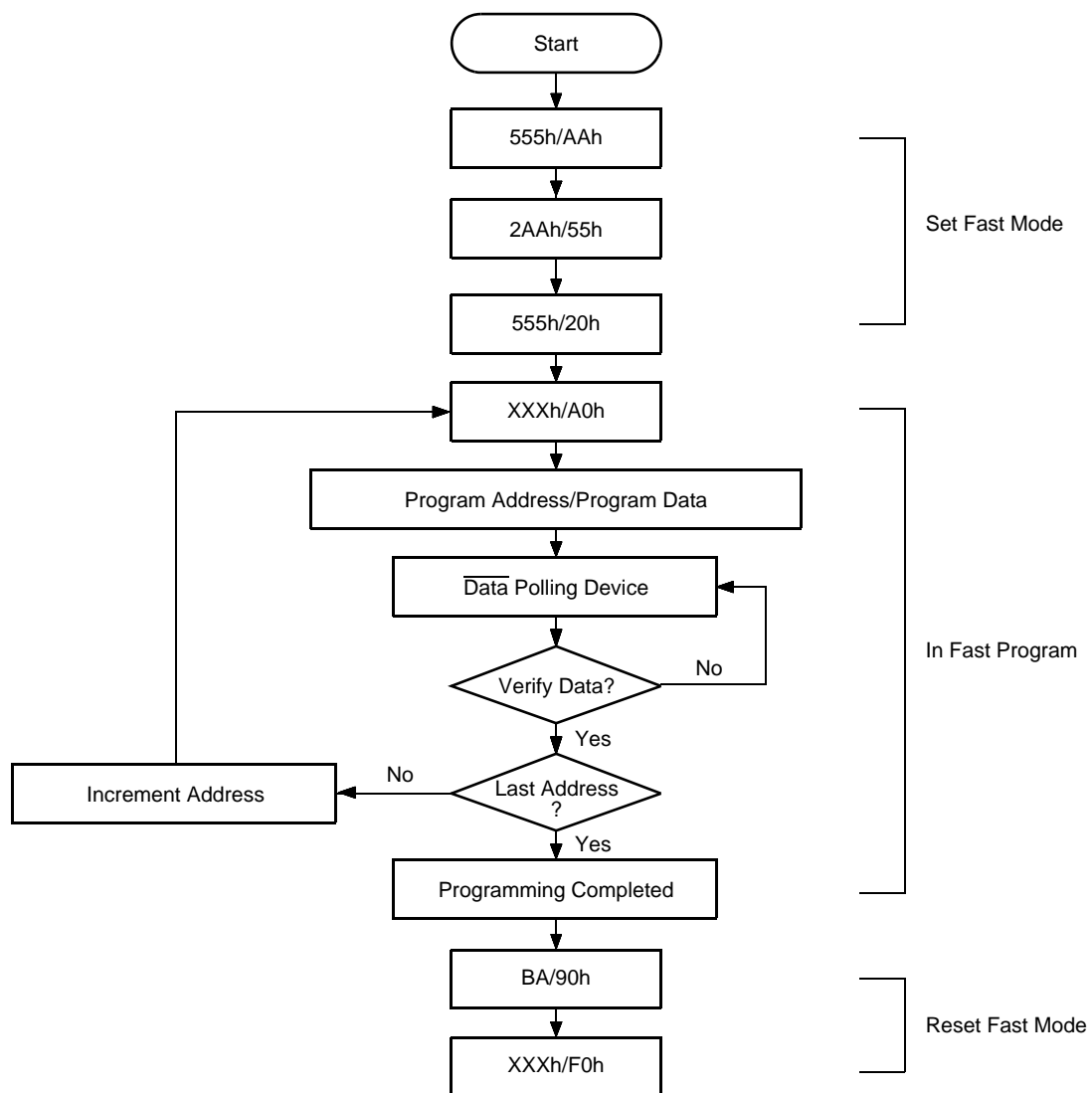
\*2 : All previously protected sector groups are reprotected once again.

Temporary Sector Group Unprotection Algorithm

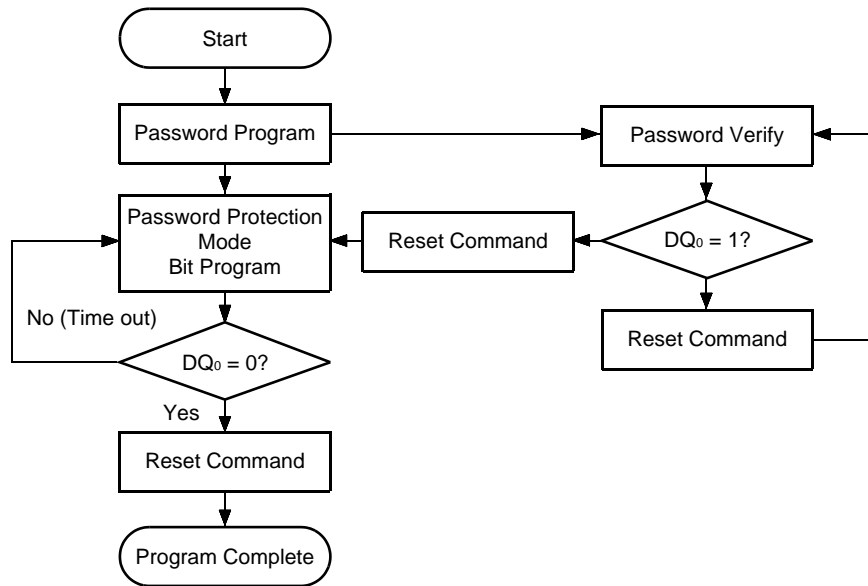


Extended Sector Group Protection Algorithm

## FAST MODE ALGORITHM

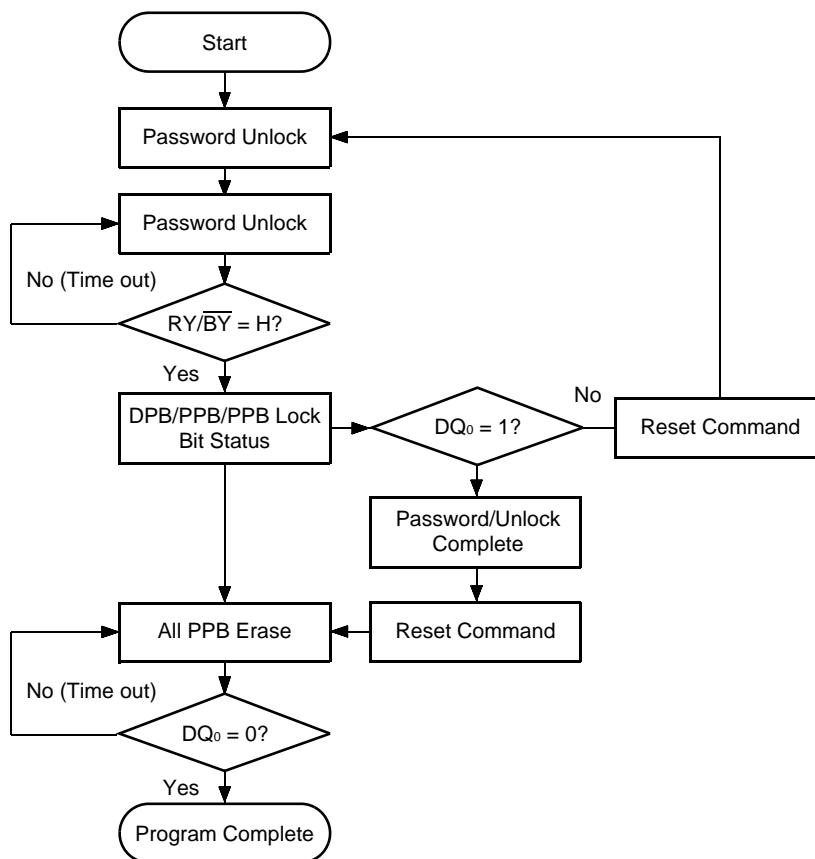


Embedded Program Algorithm for Fast Mode

**Password Mode Choice Method**

Password Sector Protect Algorithm

## PPB Lock Clear in Password Mode



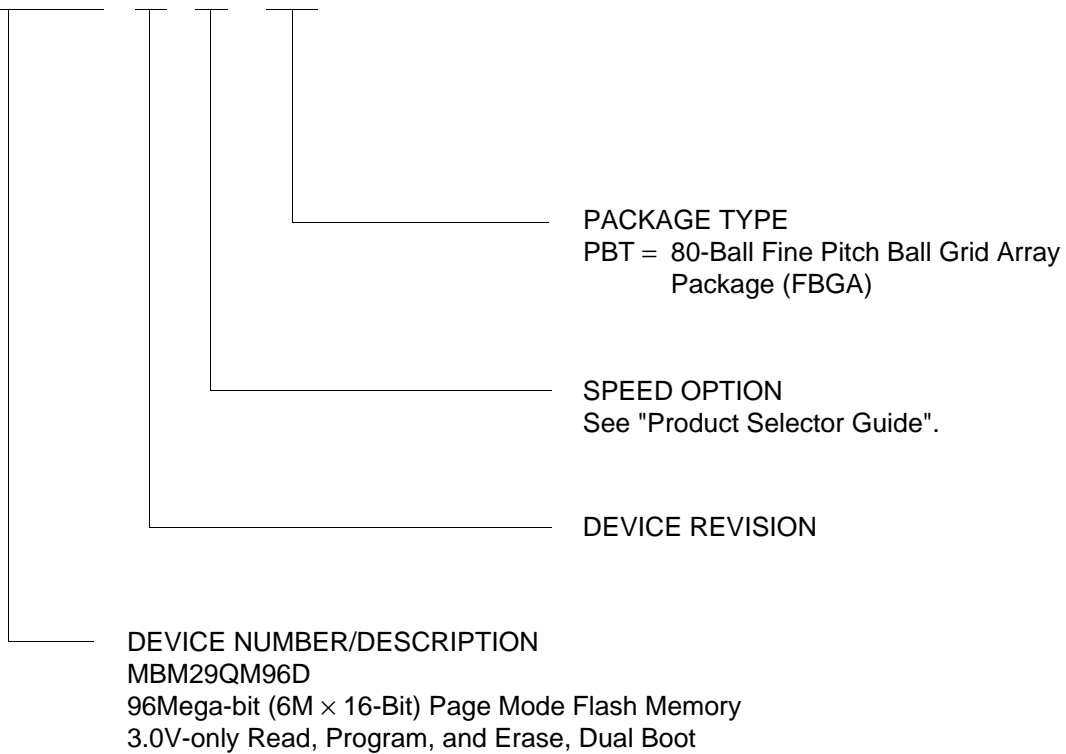
PPB Lock Bit Clear in Password Mode



## ■ ORDERING INFORMATION

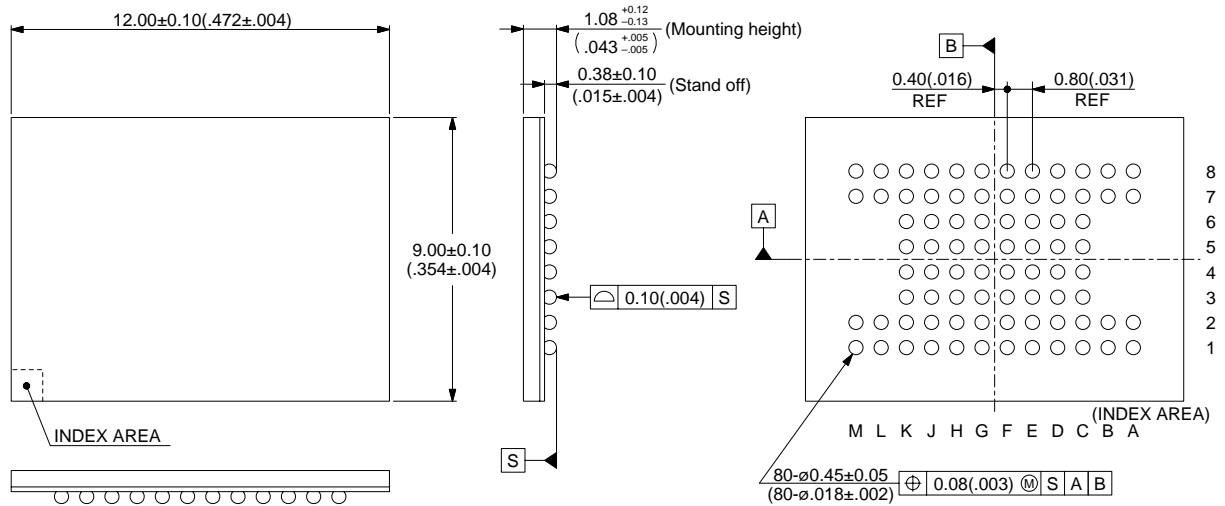
Part Number	Package	Access Time (ns)	Remarks
MBM29QM96DF65PBT	80-ball plastic FBGA (BGA-80P-M03)	65	
MBM29QM96DF80PBT		80	

MBM29QM96D   F   65   PBT



## ■ PACKAGE DIMENSIONS

80-ball plastic FBGA  
(BGA-80P-M03)



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Dimensions in mm (inches) .

Note : The values in parentheses are reference values.

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