

Features :

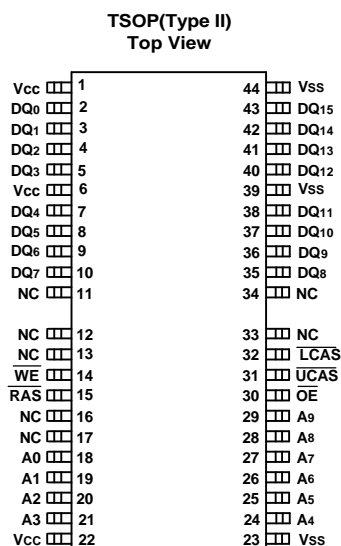
- * 1,048,576 words by 16 bits organization.
- * Fast access time and cycle time.
- * Dual CAS Input.
- * Low power dissipation.
- * Read-Modify-Write, RAS-Only Refresh, CAS-Before-RAS Refresh, Hidden Refresh and Test Mode Capability.
- * 1024 refresh cycles per 16ms.
- * Available in 400 mil TSOPII Packages.
- * Single 2.5V±0.2V Power Supply.
- * All inputs and Outputs are LVTTTL compatible.
- * Extended Data-Out(EDO) Page Mode operation.
- * Self – refresh capability. (S-Version).
- * Extended Temperature Available (-25°C ~ 85°C)

Description :

The GLT4160M16 is a 1,048,576 x 16 bit high-performance CMOS dynamic random access memory. The GLT4160M16 offers Fast Page mode with Extended Data Output, and has both BYTE WRITE and WORD WRITE access cycles via two CAS pins. The GLT4160M16 has symmetric address and accepts 1024-cycle refresh in 16ms interval.

All inputs are TTL compatible. EDO Page Mode operation allows random access up to 1024 x 16 bits within a page, with cycle times as short as 25ns.

HIGH PERFORMANCE	60	70	80
Max. RAS Access Time, (t_{RAC})	60 ns	70 ns	80 ns
Max. Column Address Access Time, (t_{CAA})	30 ns	35 ns	40 ns
Min. Extended Data Out Page Mode Cycle Time, (t_{PC})	25 ns	30 ns	35 ns
Min. Read/Write Cycle Time, (t_{RC})	104 ns	124 ns	144 ns
Max. CAS Access Time (t_{CAC})	15 ns	20 ns	20 ns

Pin Configuration :

Pin Descriptions:

Name	Function
A ₀ - A ₉	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{UCAS}}$	Column Address Strobe/Upper Byte Control
$\overline{\text{LCAS}}$	Column Address Strobe/Lower Byte Control
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
DQ ₀ - DQ ₁₅	Data Inputs / Outputs
V _{CC}	+2.5V Power Supply
V _{SS}	Ground
NC	No Connection

Absolute Maximum Ratings*

Operating Temperature, T_A (ambient)
0°C to +70°C
(extended)..-25°C to +85°C
 Storage Temperature(plastic).....-55°C to +150°C
 Voltage Relative to V_{SS}-1.0V to + 3.5V
 Short Circuit Output Current.....50mA
 Power Dissipation.....1.0W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

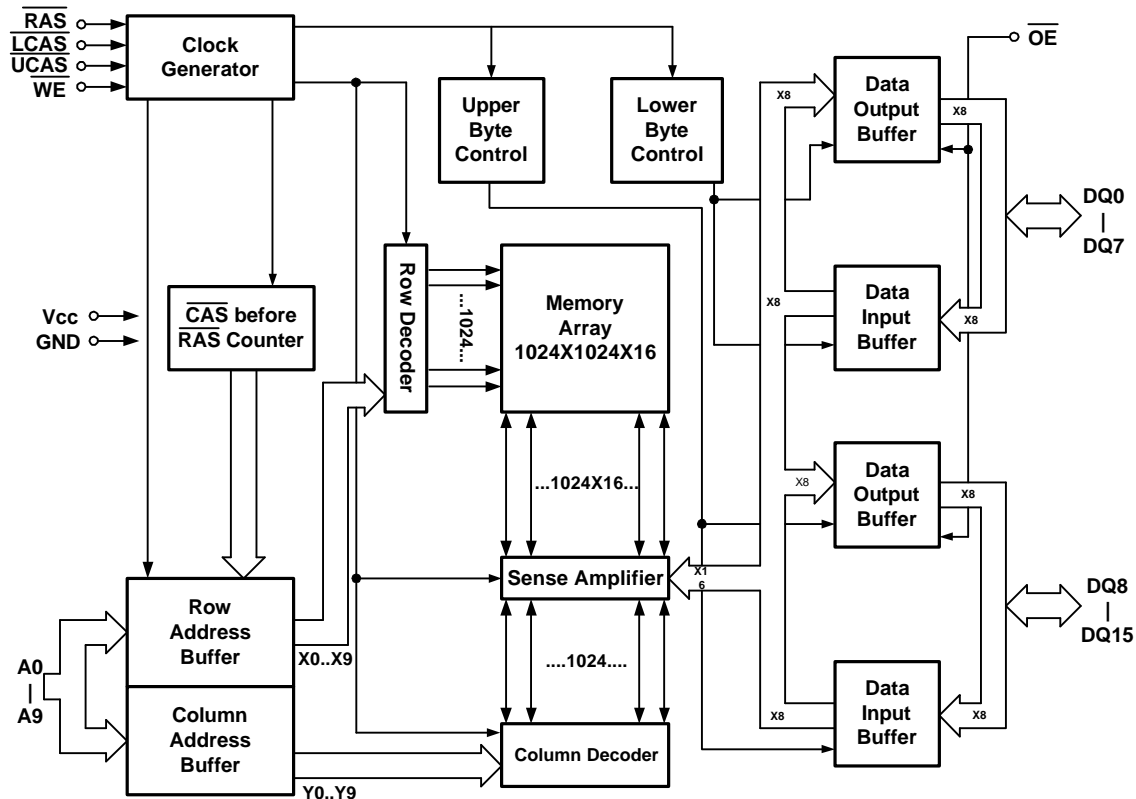
$T_A=25^{\circ}\text{C}$, $V_{CC}=2.5\text{V}\pm 0.2\text{V}$, $V_{SS}=0\text{V}$

Symbol	Parameter	Max.	Unit
C_{IN1}	Address Input	5	pF
C_{IN2}	$\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$	7	pF
C_{OUT}	Data Input/Output	7	pF

*Note: Capacitance is sampled and not 100% tested

Electrical Specifications

- $\overline{\text{CAS}}$ means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
- All voltages are referenced to GND.
- After power up, wait more than 200 μs and then, execute eight $\overline{\text{CAS}}$ -before-RAS or RAS-only refresh cycles as dummy cycles to initialize internal circuit.

Block Diagram :


DC and Operating Characteristics (1-2)

$T_A = 0^{\circ}\text{C}$ to 70°C , -25°C to 85°C (extended temperature) $V_{CC}=2.5\text{V}\pm 0.2\text{V}$, $V_{SS}=0\text{V}$, unless otherwise specified.

Sym.	Parameter	Test Conditions	Access Time	Min.	Typ	Max.	Unit	Notes
I_{LI}	Input Leakage Current (any input pin)	$0\text{V} \leq V_{IN} \leq V_{CC}+0.3\text{V}$ (All other pins not under test=0V)		-5		+5	μA	
I_{LO}	Output Leakage Current (for High-Z State)	$0\text{V} \leq V_{out} \leq V_{CC}$ Output is disabled (Hiz)		-5		+5	μA	
I_{CC1}	Operating Current, Random READ/WRITE	$t_{RC} = t_{RC}(\text{min.})$	$t_{RAC} = 60\text{ns}$ $t_{RAC} = 70\text{ns}$ $t_{RAC} = 80\text{ns}$			140 130 120	mA	1,2
I_{CC2}	Standby Current,(TTL)	$\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}}$ at V_{IH} other inputs $\geq V_{SS}$				1	mA	
I_{CC3}	Refresh Current, RAS-Only	$\overline{\text{RAS}}$ cycling, $\overline{\text{UCAS}}, \overline{\text{LCAS}}$ at V_{IH} $t_{RC} = t_{RC}(\text{min.})$	$t_{RAC} = 60\text{ns}$ $t_{RAC} = 70\text{ns}$ $t_{RAC} = 80\text{ns}$			140 130 120	mA	2
I_{CC4}	Operating Current, EDO Page Mode	$\overline{\text{RAS}}$ at V_{IL} , $\overline{\text{UCAS}}, \overline{\text{LCAS}}$ address cycling: $t_{PC}=t_{PC}(\text{min.})$	$t_{RAC} = 60\text{ns}$ $t_{RAC} = 70\text{ns}$ $t_{RAC} = 80\text{ns}$			140 130 120	mA	1,2
I_{CC5}	Refresh Current, CAS Before RAS	$\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}}$ address cycling: $t_{RC}=t_{RC}(\text{min.})$	$t_{RAC} = 60\text{ns}$ $t_{RAC} = 70\text{ns}$ $t_{RAC} = 80\text{ns}$			140 130 120	mA	1
I_{CC6}	Standby Current, (CMOS)	$\overline{\text{RAS}} \geq V_{CC}-0.2\text{V},$ $\overline{\text{UCAS}} \geq V_{CC}-0.2\text{V},$ $\overline{\text{LCAS}} \geq V_{CC}-0.2\text{V},$ All other inputs V_{SS}				200	μA	1,5
I_{CC7}	Self Refresh Current	$\overline{\text{RAS}} = \overline{\text{UCAS}} = \overline{\text{LCAS}} = V_{IL}$ $\overline{\text{WE}} = \overline{\text{OE}} = A_0 \sim A_9 = V_{CC}-0.2\text{V}$ or 0.2V $DQ_0 \sim DQ_{15} = V_{CC}-0.2\text{V}, 0.2\text{V}$ or Open				200	μA	
V_{IL}	Input Low Voltage			-0.3		+0.8	V	3
V_{IH}	Input High Voltage			2.0		$V_{CC}+0.3$	V	3
V_{OL}	Output Low Voltage	$I_{OL} = 2\text{mA}$				0.4	V	
V_{OH}	Output High Voltage	$I_{OH} = -2\text{mA}$		2			V	

Notes:

1. I_{CC} is dependent on output loading when the device output is selected. Specified $I_{CC}(\text{max.})$ is measured with the output open.
2. I_{CC} is dependent upon the number of address transitions specified $I_{CC}(\text{max.})$ is measured with a maximum of one transition per address cycle in random Read/Write and EDO Fast Page Mode.
3. Specified $V_{IL}(\text{min.})$ is steady state operation. During transitions $V_{IL}(\text{min.})$ may undershoot to -1.0V for a period not to exceed 15ns. All AC parameters are measured with $V_{IL}(\text{min.}) \geq V_{SS}$ and $V_{IH}(\text{max.}) \leq V_{CC}$.
4. Specified $V_{IH}(\text{max.})$ is steady state operation. During transitions $V_{IH}(\text{max.})$ may undershoot to $+1.0\text{V}$ for a period not to exceed 15ns. All AC parameters are measured with $V_{IL}(\text{min.}) \geq V_{SS}$ and $V_{IH}(\text{max.}) \leq V_{CC}$.
5. S-Version.

AC Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , -25°C to 85°C (extended temperature), $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$, $V_{IH} / V_{IL} = 2.0/0\text{V}$, $V_{OH}/V_{OL} = 2.0/0.8\text{V}$

An initial pause of 100 μs and 8 CAS-before-RAS or RAS-only refresh cycles are required after power-up.

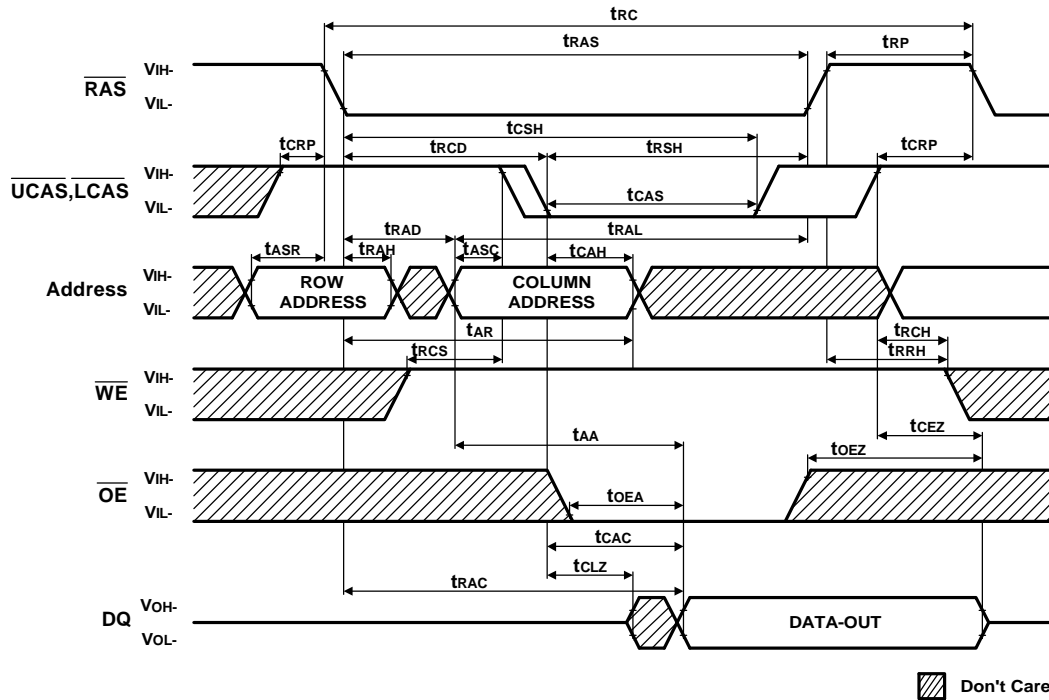
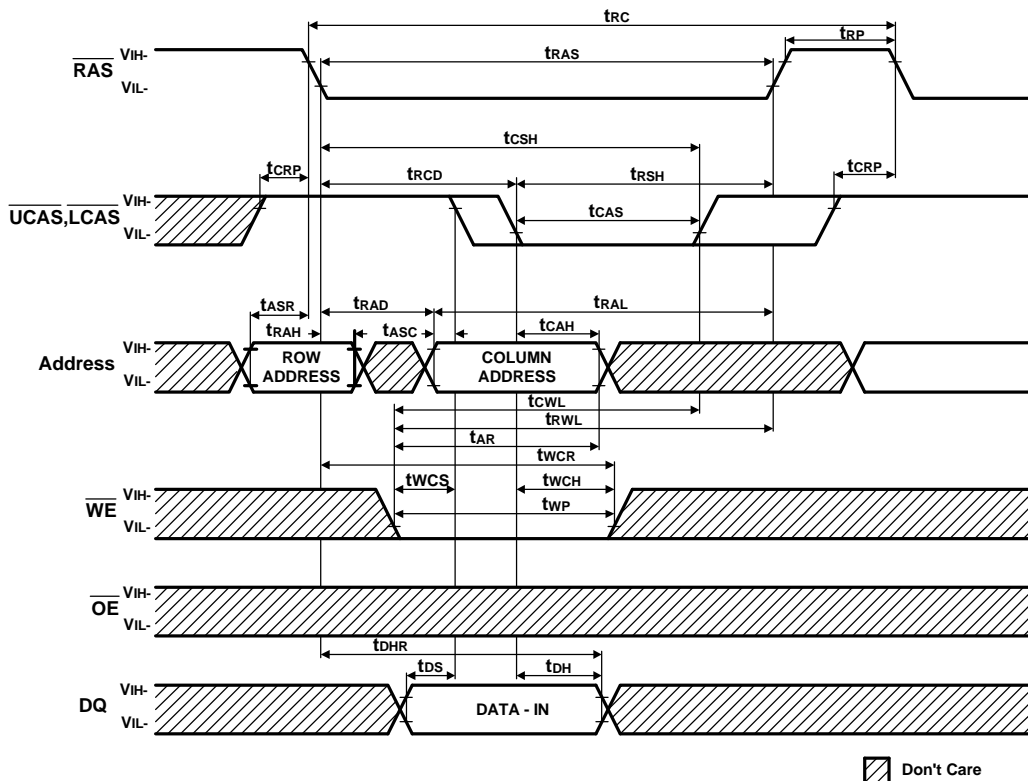
Parameter	Symbol	60		70		80		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read or Write Cycle Time	t_{RC}	104		124		144		ns	
Read Modify Write Cycle Time	t_{RWC}	140		170		190		ns	
RAS Precharge Time	t_{RP}	40		50		60		ns	
RAS Pulse Width	t_{RAS}	60	10k	70	10k	80	10k	ns	
Access Time from RAS	t_{RAC}		60		70		80	ns	1,2,3
Access Time from CAS	t_{CAC}		15		20		20	ns	1,5,10
Access Time from Column Address	t_{AA}		30		35		40	ns	1,5,6
CAS to Output Low-Z	t_{CLZ}	3		3		3		ns	
CAS to Output High-Z	t_{CEZ}	3	15	3	20	3	20	ns	
RAS Hold Time	t_{RSH}	15		20		20		ns	
RAS Hold Time Referenced to OE	t_{ROH}	10		10				ns	
CAS Hold Time	t_{CSH}	45		50		70		ns	
CAS Pulse Width	t_{CAS}	10	10k	15	10k	20	80k	ns	
RAS to CAS Delay Time	t_{RCD}	20	45	20	50	20	60	ns	
RAS to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	ns	7
CAS to RAS Precharge Time	t_{CRP}	5		5		5		ns	
Row Address Set-Up Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		10		ns	
Column Address Set-Up Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	10		15		15		ns	
Column Address to RAS Lead Time	t_{RAL}	30		35		40		ns	
Column Address Hold Time Referenced to RAS	t_{AR}	45		50		60		ns	
Read Command Set-Up Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to CAS	t_{RCH}	0		0		0		ns	4
Read Command Hold Time Referenced to RAS	t_{RRH}	0		0		0		ns	4
Write Command Set-Up Time	t_{WCS}	0		0		0		ns	8,9
Write Command Hold Time	t_{WCH}	10		15		15		ns	
Write Command Pulse Width	t_{WP}	10		15		15		ns	
Write Command to RAS Lead Time	t_{RWL}	15		30		20		ns	
Write Command to CAS Lead Time	t_{CWL}	13		15		20		ns	

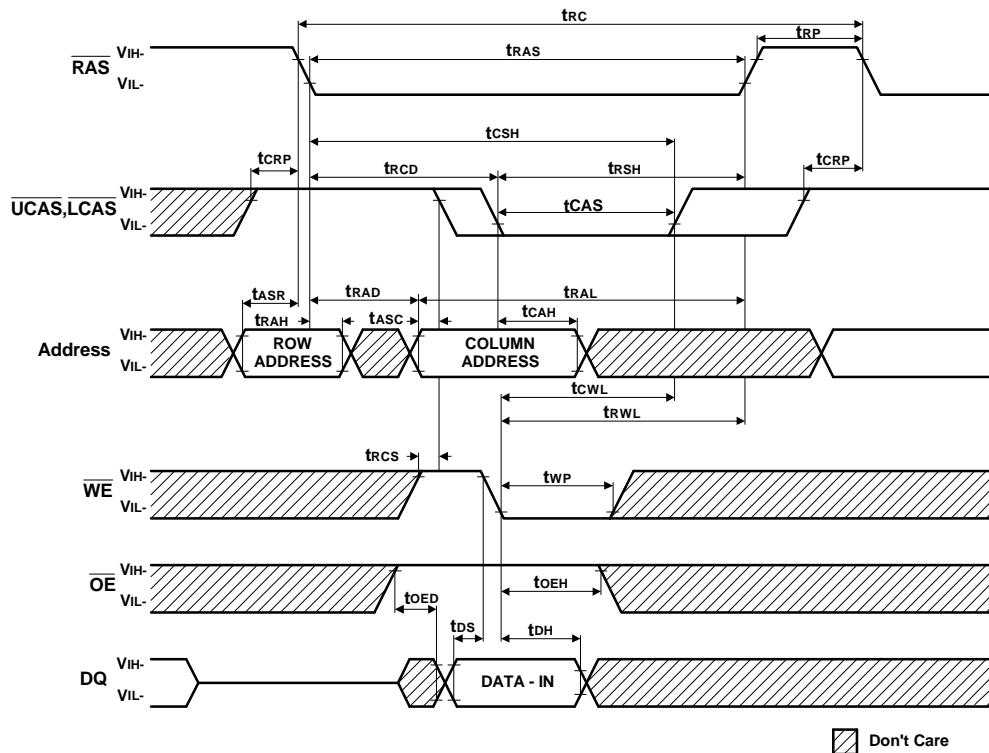
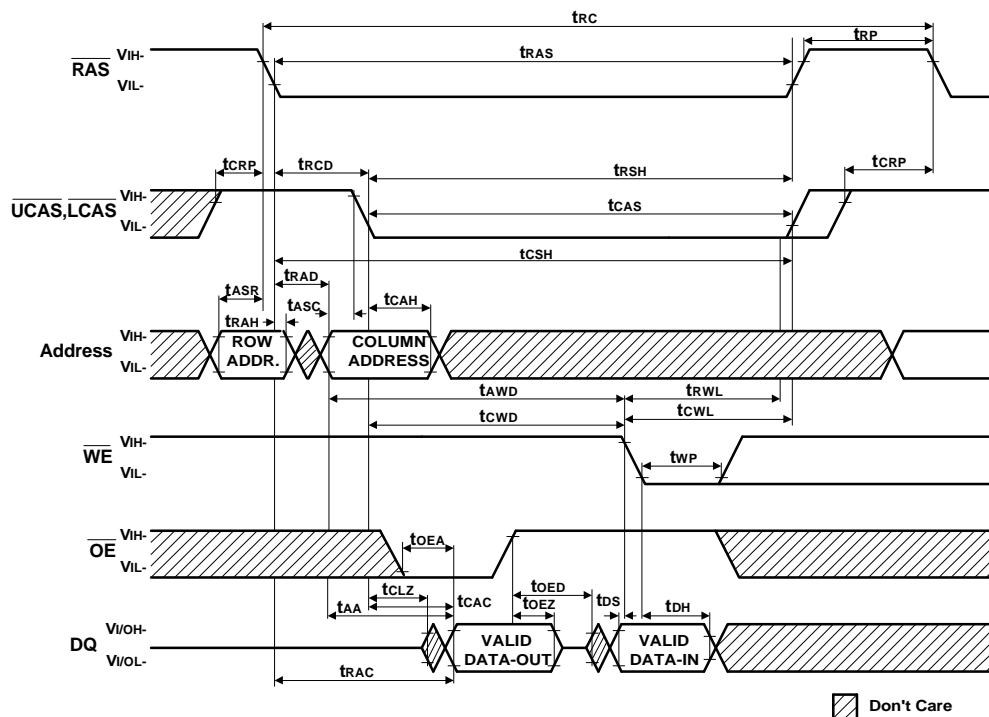
AC Characteristics

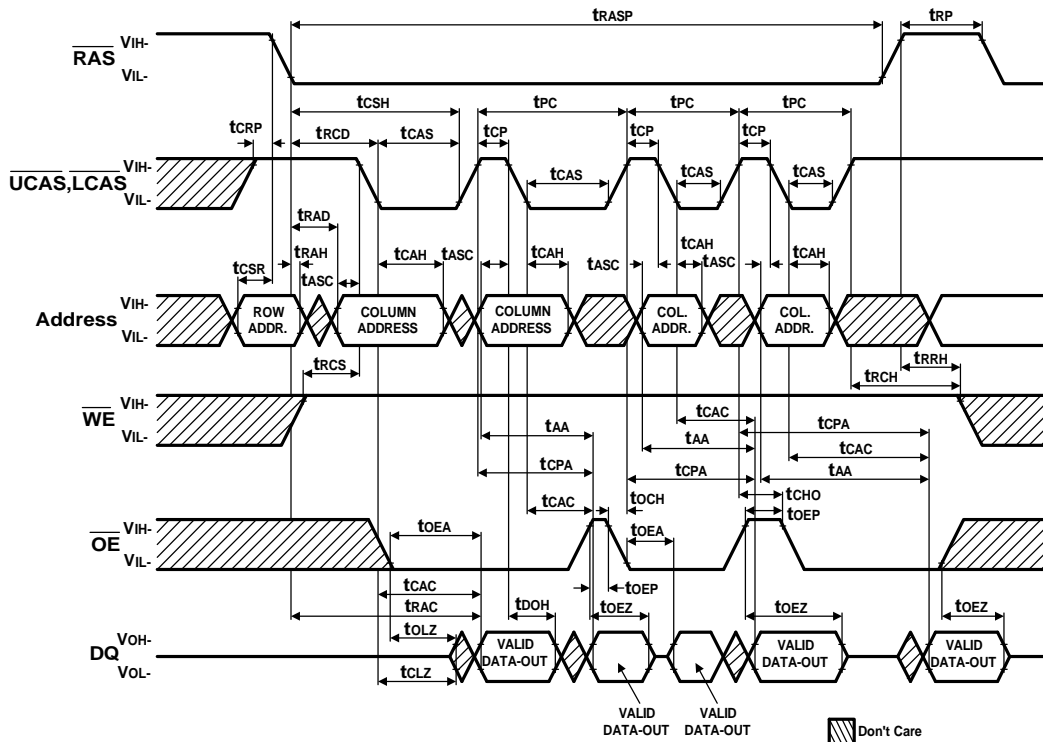
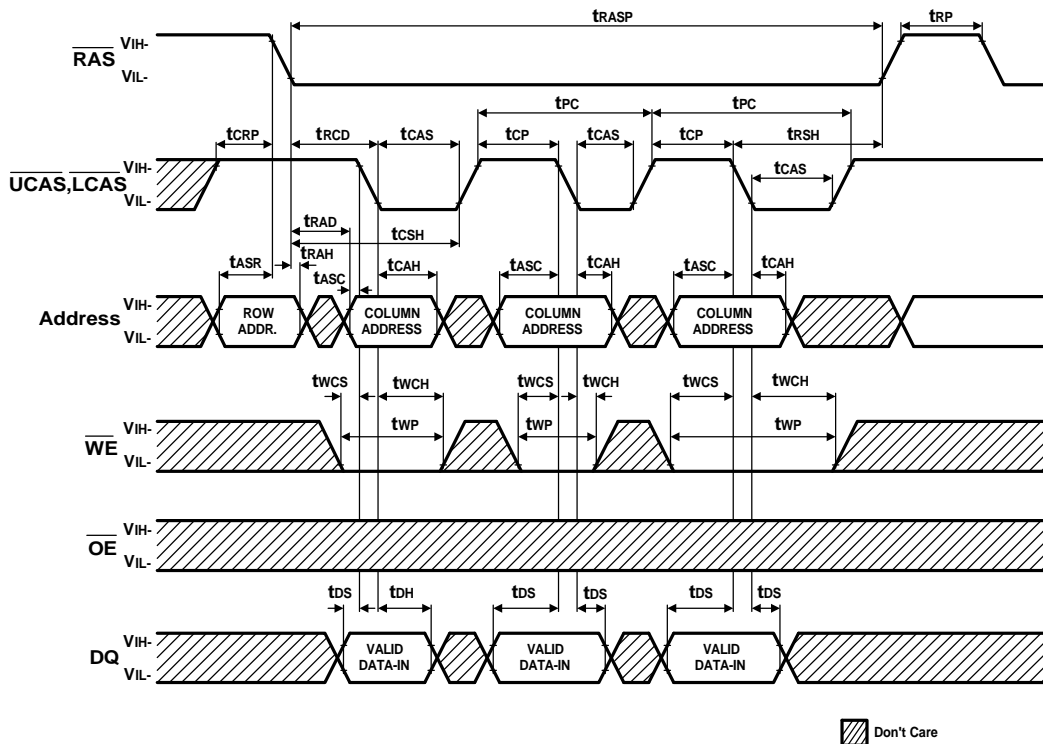
Parameter	Symbol	60		70		80		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Data Set-Up Time	t_{DS}	0		0		0		ns	
Data Hold Time	t_{DH}	10		15		15		ns	
Data Hold Time Referenced to \overline{RAS}	t_{DHR}	45		50		60		ns	
\overline{RAS} to \overline{WE} Delay Time	t_{RWD}	79		94		99		ns	
\overline{CAS} to \overline{WE} Delay Time	t_{CWD}	34		44		44		ns	
Column Address to \overline{WE} Delay Time	t_{AWD}	49		59		64		ns	
\overline{RAS} to \overline{CAS} Precharge Time	t_{RPC}	0		0		5		ns	
Access Time from \overline{CAS} Precharge	t_{CPA}		35		40		45	ns	
EDO Page Mode Cycle Time	t_{PC}	25		30		35		ns	
EDO Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	56		71		81		ns	
\overline{CAS} Precharge Time (EDO Page Mode)	t_{CP}	10		10		10		ns	
\overline{RAS} Pulse Width (EDO Page Mode Only)	t_{RASP}	60	100k	70	100k	80	100k	ns	
Access Time from \overline{OE}	t_{OEA}		15		20		20	ns	
\overline{OE} to Data Delay Time	t_{OED}	15		20		20		ns	
\overline{OE} to Output High-Z	t_{OEZ}	3	20	3	20	3	20	ns	
\overline{OE} Command Hold Time	t_{OEH}	15		20		20		ns	
Data Output Hold after \overline{CAS} low	t_{DOH}	5		5		5		ns	
\overline{RAS} to Output High-Z	t_{REZ}	3	15	3	20	3	20	ns	
\overline{WE} to Output High-Z	t_{WEZ}	3	15	3	20	3	20	ns	
\overline{OE} to \overline{CAS} Hold Time	t_{OCH}	5		5		5		ns	
\overline{CAS} Hold Time to \overline{OE}	t_{CHO}	5		5		5		ns	
\overline{OE} Precharge Time	t_{OEP}	5		5		5		ns	
\overline{CAS} Set-Up Time for \overline{CAS} -before- \overline{RAS} Cycle	t_{CSR}	5		5		5		ns	
\overline{CAS} Hold Time for \overline{CAS} -before- \overline{RAS} Cycle	t_{CHR}	10		15		15		ns	
Transition Time	t_T	2	50	2	50	2	50	ns	
Refresh Period	t_{REF}		16		16		16	ms	
\overline{RAS} pulse width (\overline{CAS} -before- \overline{RAS} Self refresh)	t_{RASS}	100		100		128		μs	
\overline{RAS} precharge time (\overline{CAS} -before- \overline{RAS} Self refresh)	t_{RPS}	110		130		150		ns	
\overline{CAS} precharge time (\overline{CAS} -before- \overline{RAS} Self refresh)	t_{CHS}	50		50		50		ns	

Notes:

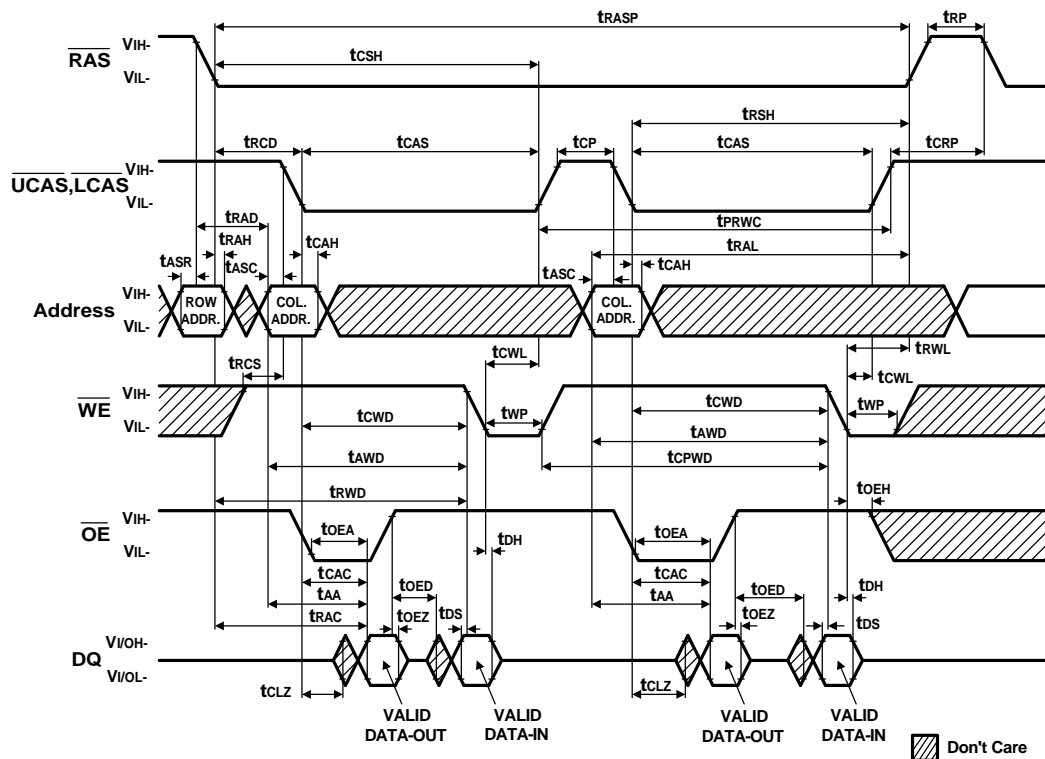
1. Measure with a load equivalent to one TTL inputs and 50 pF.
2. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max.})$. If t_{RCD} is greater than $t_{\text{RCD}}(\text{max.})$, access time will be t_{AA} dominant.
3. Assumes that $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max.})$. If t_{RAD} is greater than $t_{\text{RCD}}(\text{max.})$, access time will be controlled by t_{CAC} .
4. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle.
5. Access time is determined by the longest of t_{CAA} , t_{CAC} and t_{CPA} .
6. Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max.})$.
7. Operation within the $t_{\text{RAD}}(\text{max.})$ limit ensures that $t_{\text{RAC}}(\text{max.})$ can be met. $t_{\text{RAD}}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max.})$ limit, the access time is controlled by t_{CAA} and t_{CAC} .
8. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters.
9. $t_{\text{WCS}}(\text{min.})$ must be satisfied in an Early Write Cycle.
10. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{\text{CAS}}$ of $\overline{\text{WE}}$.
11. t_{T} is measured between $V_{\text{IH}}(\text{min.})$ and $V_{\text{IL}}(\text{max.})$. AC-measurements assume $t_{\text{T}} = 1.5 \text{ ns}$.

Read CYCLE Note : $D_{IN} = \text{OPEN}$

Early Write Cycle NOTE : $D_{OUT} = \text{OPEN}$


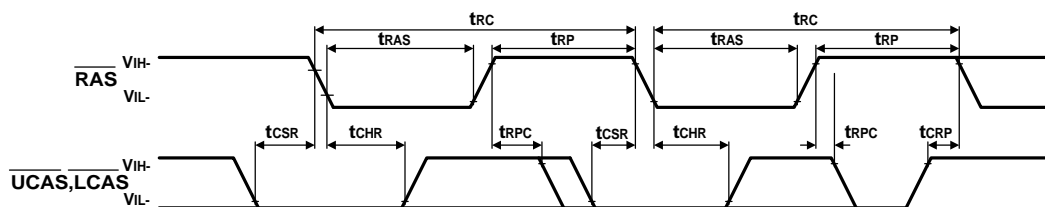
OE Controlled Write Cycle NOTE : $D_{OUT} = OPEN$

Read - Modify - Write Cycle


EDO Page Mode Read Cycle

EDO Page Mode Early Write Cycle NOTE : $D_{OUT} = OPEN$


EDO Page Mode Read - Modify - Write Cycle

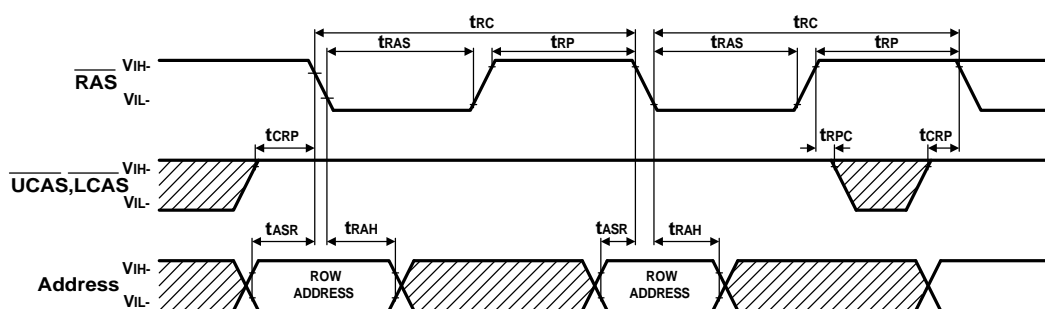


CAS - Before - **RAS** Refresh Cycle



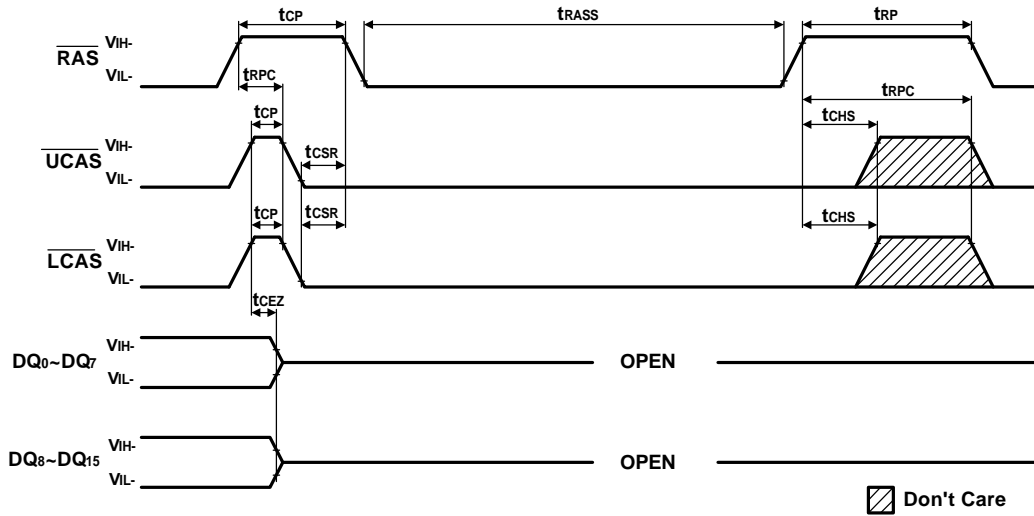
Remark Address, WE, OE : Don't care DQ : Hi-Z

RAS -Only Refresh Cycle

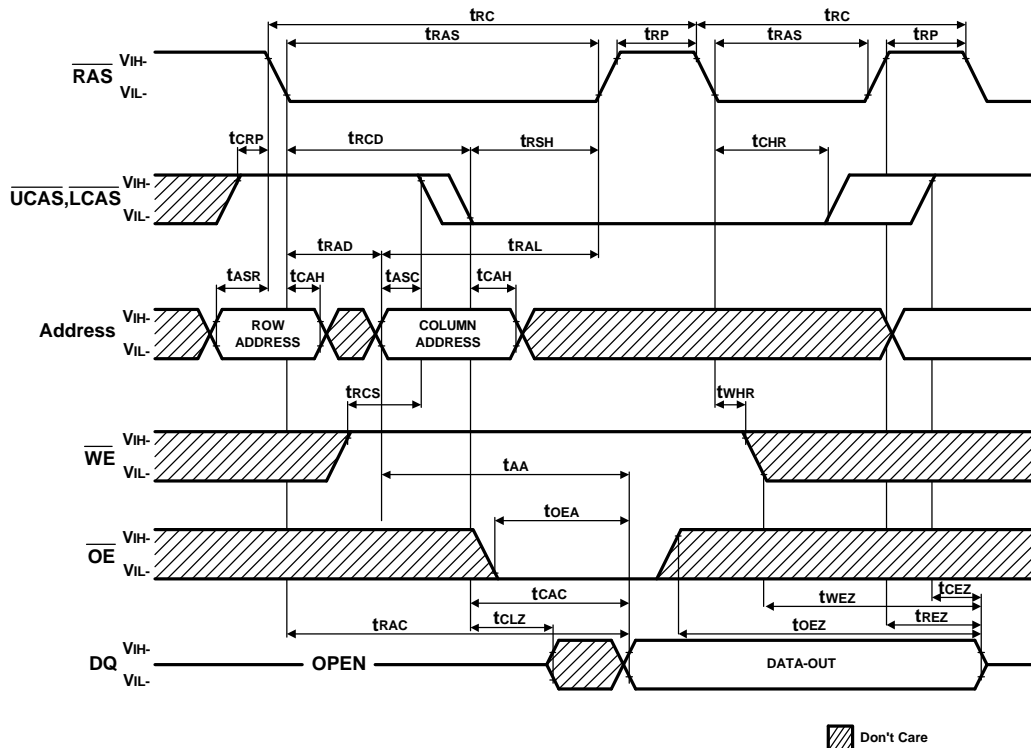


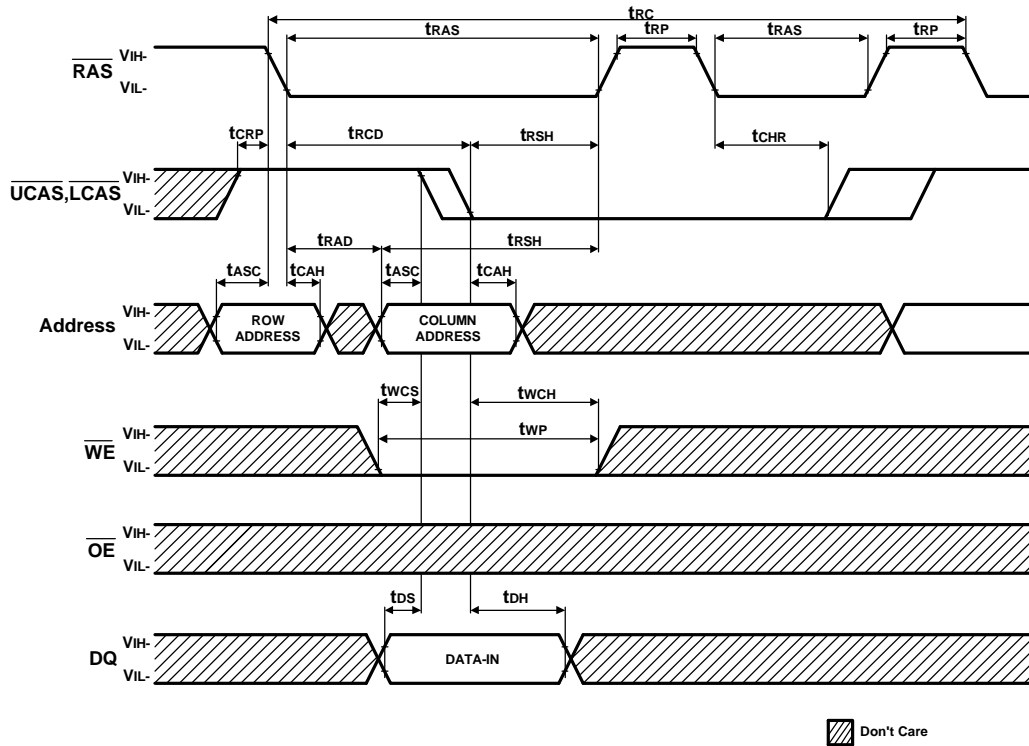
Remark WE, OE : Don't care DQ : Hi-Z

CAS - Before - RAS Self Refresh Cycle

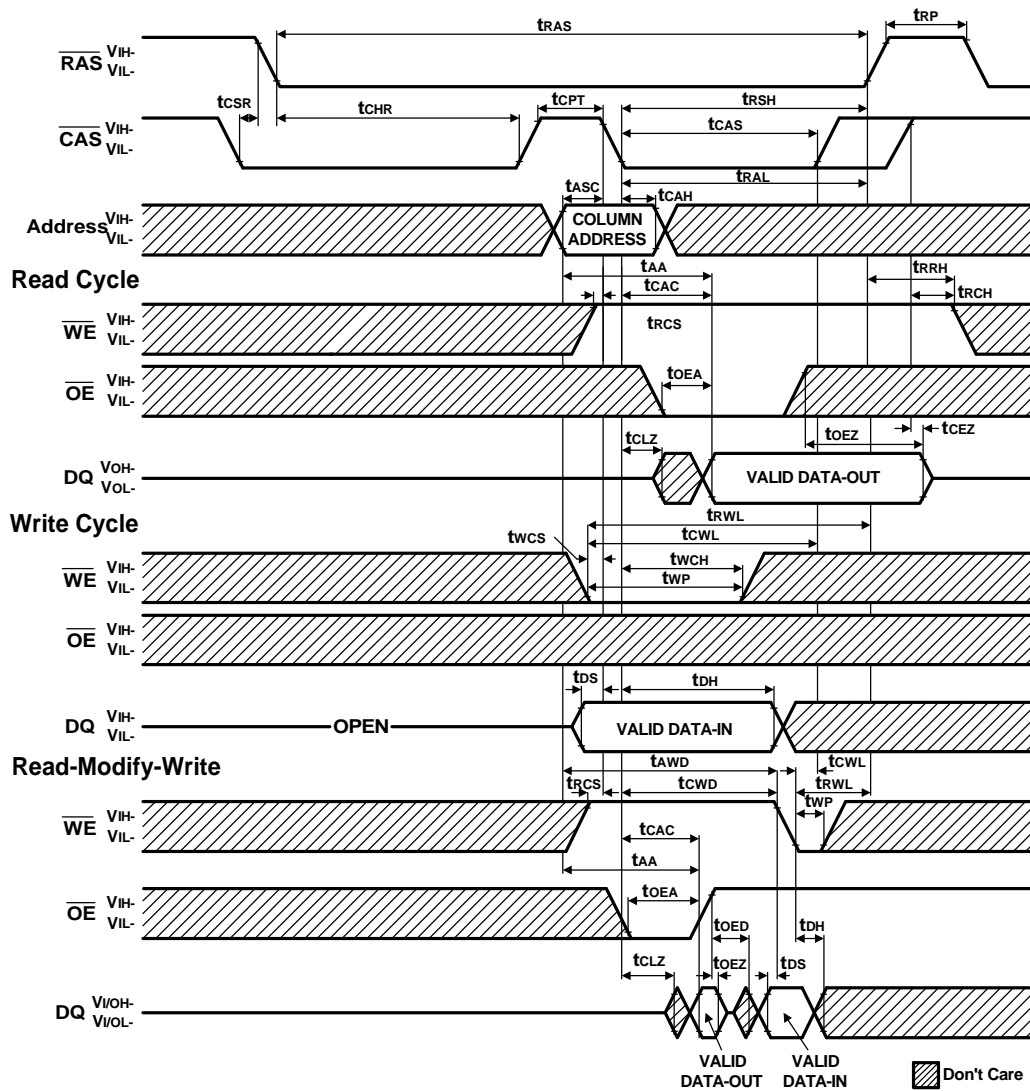


Hidden Refresh Cycle (Read)



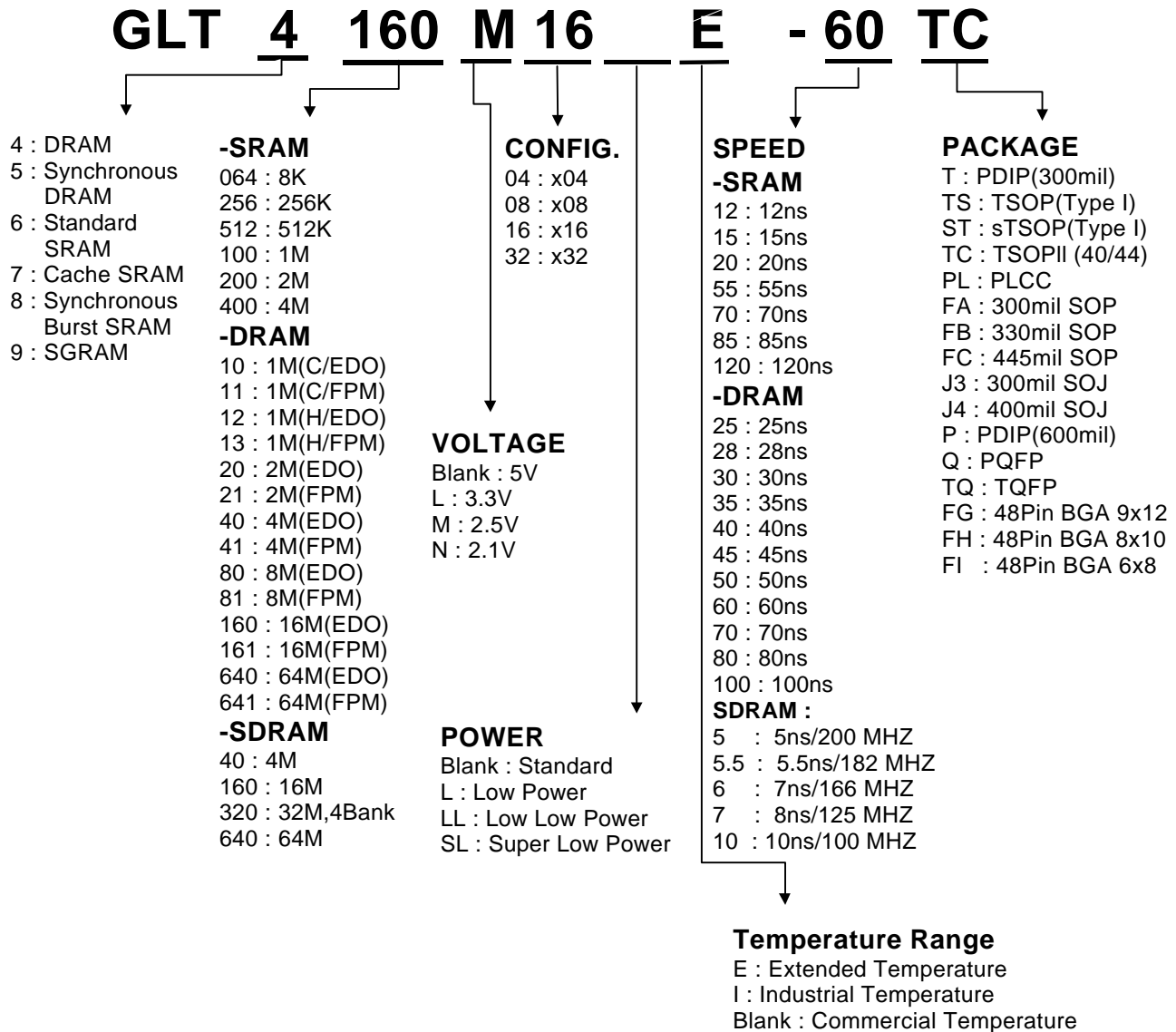
Hidden Refresh Cycle (Write) NOTE : D_{OUT} = OPEN


CAS -Before- RAS Refresh Counter Test Cycle



**GLT4160M16****1M X 16 CMOS DYNAMIC RAM WITH EXTENDED DATA OUTPUT***Dec 2001 (Rev.1.1)***Ordering Information**

Part Number	SPEED	POWER	FEATURE	PACKAGE
GLT4160M16-60TC	60ns	Normal	EDO	44/50L 400mil TSOPII
GLT4160M16-70TC	70ns	Normal	EDO	44/50L 400mil TSOPII
GLT4160M16-80TC	80ns	Normal	EDO	44/50L 400mil TSOPII
GLT4160M16E-60TC	60ns	Normal	EDO	44/50L 400mil TSOPII
GLT4160M16E-70TC	70ns	Normal	EDO	44/50L 400mil TSOPII
GLT4160M16E-80TC	80ns	Normal	EDO	44/50L 400mil TSOPII

Parts Numbers (Top Mark) Definition :


Package Information

44/50L TSOPII 400MIL

