

Features :

- * 1,048,576 words by 4 bits organization.
- * Fast access time and cycle time
- * Low power dissipation.
- * Read-Modify-Write, $\overline{\text{RAS}}$ -Only Refresh, $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh, Hidden Refresh.
- * 1,024 refresh cycles per 16ms.
- * Available in 300 mil 20/26pin SOJ and TSOPII.
- * 3.3V \pm 0.3V Vcc Power Supply voltage.
- * All inputs and Outputs are LVTTTL compatible.
- * Extended Data-Out (EDO) Page access cycle.
- * Self-refresh Capability.
- * Extended Temperature Available (-25°C~85°C)

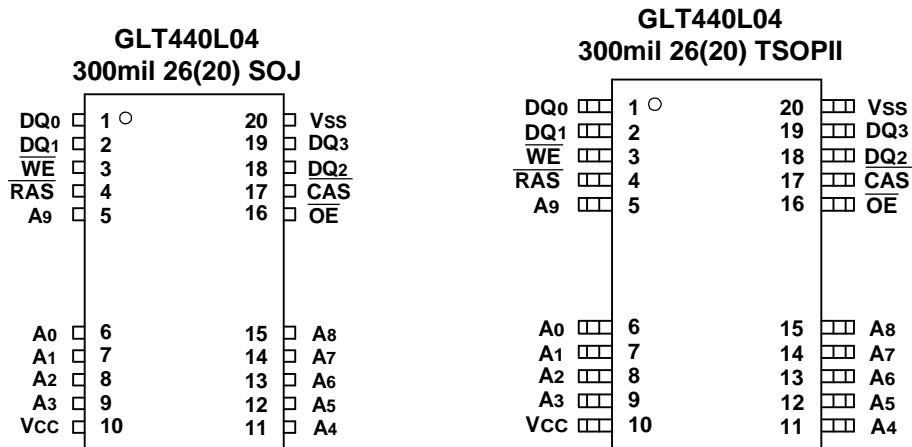
Description :

The GLT440L04 is a high-performance CMOS dynamic random access memory containing 4,194,304 bits organized in a x4 configuration. The GLT440L04 offers page cycle access with Extended Data Output. The GLT440L04 has 10 row- and 10 column-addresses, and accepts 1024-cycle refresh in 16 ms.

The GLT440L04 provides EDO PAGE MODE operation which allows for fast data access within a row-address defined boundary, up to 1024 x 4 bits with cycle times as short as 20ns.

| HIGH PERFORMANCE | 50 | 60 | 70 |
|--|-------|--------|--------|
| Max. $\overline{\text{RAS}}$ Access Time, (t_{RAC}) | 50 ns | 60 ns | 70 ns |
| Max. Column Address Access Time, (t_{AA}) | 25 ns | 30 ns | 35 ns |
| Min. Extended Data Out Page Mode Cycle Time, (t_{PC}) | 20 ns | 25 ns | 30 ns |
| Min. Read/Write Cycle Time, (t_{RC}) | 84 ns | 104 ns | 124 ns |
| Max. $\overline{\text{CAS}}$ Access Time (t_{CAC}) | 13 ns | 15 ns | 20 ns |

Pin Configuration :



Pin Descriptions:

| Name | Function |
|------------------|-----------------------|
| $A_0 - A_9$ | Address Inputs |
| \overline{RAS} | Row Address Strobe |
| \overline{CAS} | Column Address Strobe |
| \overline{WE} | Write Enable |
| \overline{OE} | Output Enable |
| $DQ_0 - DQ_3$ | Data Inputs / Outputs |
| V_{CC} | +3.3V Power Supply |
| V_{SS} | Ground |
| NC | No Connection |

Absolute Maximum Ratings*

| | |
|--|-------------------|
| Operating Temperature, T_A (ambient) |0°C to +70°C |
| (extended)..... | -25°C to + 85°C |
| Storage Temperature(plastic)..... | -55°C to +150°C |
| Voltage Relative to V_{SS} | -0.5V to + 4.6V |
| Short Circuit Output Current..... | 20mA |
| Power Dissipation..... | 1.0W |

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

$T_A=25^\circ\text{C}$, $V_{CC}=3.3\text{V}\pm 0.3\text{V}$, $V_{SS}=0\text{V}$

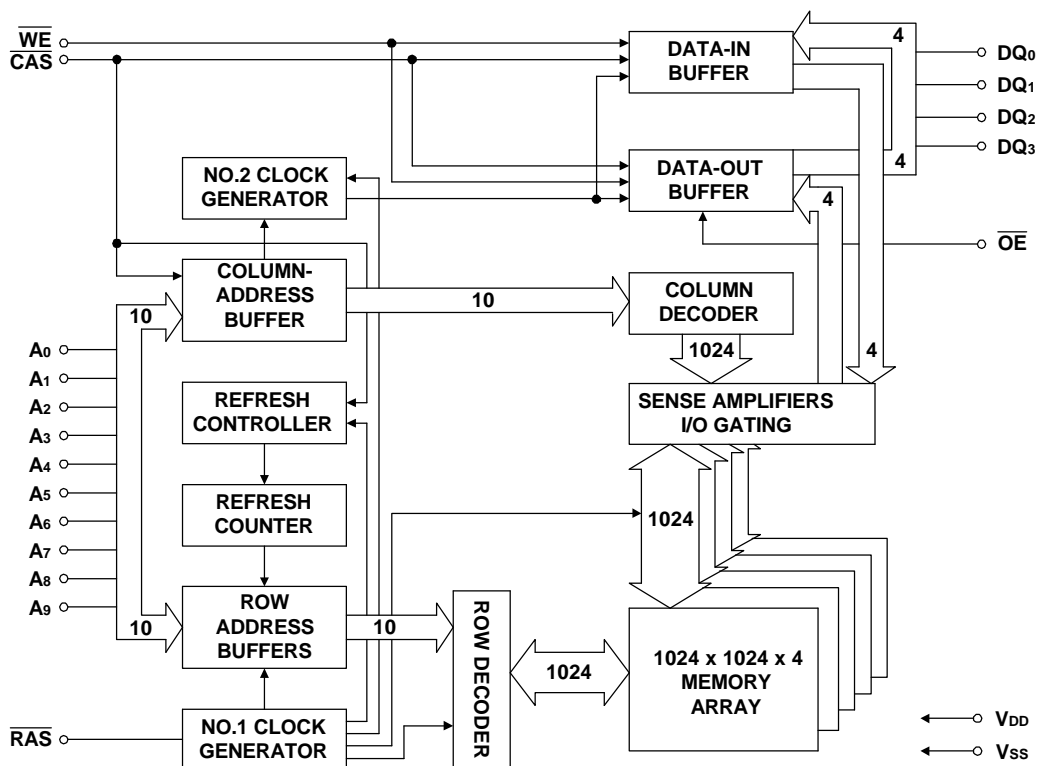
| Symbol | Parameter | Max. | Unit |
|-----------|---|------|------|
| C_{IN1} | Address Input | 5 | pF |
| C_{IN2} | $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ | 7 | pF |
| C_{OUT} | Data Input/Output | 7 | pF |

*Note: Capacitance is sampled and not 100% tested

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 200 μs and then, execute eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ -only refresh cycles as dummy cycles to initialize internal circuit.

Block Diagram :



Truth Table:

| Function | | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | $\overline{\text{OE}}$ | ADDRESS | | DATA-IN/OUT |
|---------------------------------------|-----------|-------------------------|-------------------------|------------------------|------------------------|---------|-------|------------------|
| | | | | | | t_R | t_C | DQ0-DQ3 |
| Standby | | H | H→X | X | X | X | X | High-Z |
| READ | | L | L | H | L | ROW | COL | Data-Out |
| EARLY WRITE | | L | L | L | X | ROW | COL | Data-In |
| READ WRITE | | L | L | H→L | L→H | ROW | COL | Data-Out,Data-In |
| EDO-PAGE-MODE READ | 1st Cycle | L | H→L | H | L | ROW | COL | Data-Out |
| | 2nd cycle | L | H→L | H | L | n/a | COL | Data-Out |
| EDO-PAGE-MODE EARLY-WRITE | 1st Cycle | L | H→L | L | X | ROW | COL | Data-In |
| | 2nd cycle | L | H→L | L | X | n/a | COL | Data-In |
| EDO-PAGE-MODE READ-WRITE | 1st Cycle | L | H→L | H→L | L→H | ROW | COL | Data-Out,Data-In |
| | 2nd cycle | L | H→L | H→L | L→H | n/a | COL | Data-Out,Data-In |
| $\overline{\text{RAS}}$ -ONLY REFRESH | | L | H | X | X | ROW | n/a | High-Z |
| HIDDEN REFRESH | READ | L→H→L | L | H | L | ROW | COL | Data-Out |
| | WRITE | L→H→L | L | L | X | ROW | COL | Data-In |
| CBR REFRESH | | H→L | L | H | X | X | X | High-Z |
| SELF REFRESH | | H→L | L | H | X | X | X | High-Z |

DC and Operating Characteristics (1-2)

$T_A = 0^{\circ}\text{C}$ to 70°C , -25°C to 85°C (extended temperature) $V_{CC}=3.3\text{V}\pm 0.3\text{V}$, $V_{SS}=0\text{V}$, unless otherwise specified.

| Sym. | Parameter | Test Conditions | Access Time | Min. | Typ | Max. | Unit | Notes |
|-----------|--|--|---|------|-----|----------------|---------------|-------|
| I_{LI} | Input Leakage Current (any input pin) | $0\text{V} \leq V_{IN} \leq V_{CC}+0.3\text{V}$ (All other pins not under test=0V) | | -5 | | +5 | μA | |
| I_{LO} | Output Leakage Current (for High-Z State) | $0\text{V} \leq V_{out} \leq V_{CC}$ Output is disabled (Hiz) | | -5 | | +5 | μA | |
| I_{CC1} | Operating Current, Random READ/WRITE | $t_{RC} = t_{RC}(\text{min.})$ | $t_{RAC} = 50\text{ns}$ $t_{RAC} = 60\text{ns}$ $t_{RAC} = 70\text{ns}$ | | | 90 80 70 | mA | 1,2 |
| I_{CC2} | Standby Current | $\overline{\text{RAS}}, \overline{\text{CAS}}$ at V_{IH} other inputs $\geq V_{SS}$ | | | | 1 | mA | |
| I_{CC3} | Refresh Current, $\overline{\text{RAS}}$ -Only | $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ at V_{IH} $t_{RC} = t_{RC}(\text{min.})$ | $t_{RAC} = 50\text{ns}$ $t_{RAC} = 60\text{ns}$ $t_{RAC} = 70\text{ns}$ | | | 90 80 70 | mA | 2 |
| I_{CC4} | Operating Current, EDO Page Mode | $\overline{\text{RAS}}$ at V_{IL} , $\overline{\text{CAS}}$ address cycling: $t_{PC}=t_{PC}(\text{min.})$ | $t_{RAC} = 50\text{ns}$ $t_{RAC} = 60\text{ns}$ $t_{RAC} = 70\text{ns}$ | | | 90 80 70 | mA | 1,2 |
| I_{CC5} | Refresh Current, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ | $\overline{\text{RAS}}, \overline{\text{CAS}}$ address cycling: $t_{RC}=t_{RC}(\text{min.})$ | $t_{RAC} = 50\text{ns}$ $t_{RAC} = 60\text{ns}$ $t_{RAC} = 70\text{ns}$ | | | 90 80 70 | mA | 2 |
| I_{CC6} | Standby Current, (CMOS) | $\overline{\text{RAS}} \geq V_{CC}-0.2\text{V}$, $\overline{\text{CAS}} \geq V_{CC}-0.2\text{V}$, All other inputs V_{SS} | | | | 300 | μA | |
| I_{CC7} | Self refresh Current | $\overline{\text{RAS}} = \overline{\text{CAS}} = 0.2\text{V}$, $\overline{\text{WE}} = \overline{\text{OE}} = A_0 \sim A_9 = V_{CC}-0.2\text{V}$ or 0.2V $DQ_0 \sim DQ_3 = V_{CC}-0.2\text{V}, 0.2\text{V}$ or Open | | | | 300 | μA | |
| V_{IL} | Input Low Voltage | | | -0.3 | | +0.8 | V | 3 |
| V_{IH} | Input High Voltage | | | 2.0 | | $V_{CC}+0.3$ | V | 4 |
| V_{OL} | Output Low Voltage | $I_{OL} = 2\text{mA}$ | | | | 0.4 | V | |
| V_{OH} | Output High Voltage | $I_{OH} = -2\text{mA}$ | | 2.4 | | | V | |

Notes:

- I_{CC} is dependent on output loading when the device output is selected. Specified $I_{CC}(\text{max.})$ is measured with the output open.
- I_{CC} is dependent upon the number of address transitions specified $I_{CC}(\text{max.})$ is measured with a maximum of one transition per address cycle in random Read/Write and EDO Fast Page Mode.
- Specified $V_{IL}(\text{min.})$ is steady state operation. During transitions $V_{IL}(\text{min.})$ may undershoot to -0.9V for a period not to exceed 10ns. All AC parameters are measured with $V_{IL}(\text{min.}) \geq V_{SS}$ and $V_{IH}(\text{max.}) \leq V_{CC}$.
- Specified $V_{IH}(\text{max.})$ is steady state operation. During transitions $V_{IH}(\text{max.})$ may overshoot to $V_{CC}+0.9\text{V}$ for a period not to exceed 10ns. All AC parameters are measured with $V_{IL}(\text{min.}) \geq V_{SS}$ and $V_{IH}(\text{max.}) \leq V_{CC}$.

AC Characteristics

$T_A = -0^{\circ}\text{C}$ to 70°C , -25°C to 85°C (extended temperature), $V_{CC} = 3.3\text{ V} \pm 0.3\text{V}$, $V_{IH}/V_{IL} = 3.0/0\text{V}$, $V_{OH}/V_{OL} = 2/0.8\text{V}$

An initial pause of 200 μs and 8 CAS -before- RAS or RAS -only refresh cycles are required after power-up.

| Parameter | Symbol | 50 | | 60 | | 70 | | Unit | Notes |
|--|-----------|------|------|------|------|------|------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Read or Write Cycle Time | t_{RC} | 84 | | 104 | | 124 | | ns | |
| Read Modify Write Cycle Time | t_{RWC} | 116 | | 140 | | 170 | | ns | |
| RAS Precharge Time | t_{RP} | 30 | | 40 | | 50 | | ns | |
| RAS Pulse Width | t_{RAS} | 50 | 10k | 60 | 10k | 70 | 10k | ns | |
| Access Time from RAS | t_{RAC} | | 50 | | 60 | | 70 | ns | 1,2,3 |
| Access Time from CAS | t_{CAC} | | 13 | | 15 | | 20 | ns | 1,5,7 |
| Access Time from Column Address | t_{AA} | | 25 | | 30 | | 35 | ns | 1,5,6 |
| CAS to Output Low-Z | t_{CLZ} | 3 | | 3 | | 3 | | ns | |
| CAS to Output High-Z | t_{CEZ} | 3 | 13 | 3 | 15 | 3 | 20 | ns | |
| RAS Hold Time | t_{RSH} | 13 | | 15 | | 20 | | ns | |
| CAS Hold Time | t_{CSH} | 38 | | 45 | | 50 | | ns | |
| CAS Pulse Width | t_{CAS} | 8 | 10k | 10 | 10k | 15 | 10k | ns | |
| RAS to CAS Delay Time | t_{RCD} | 20 | 37 | 20 | 45 | 20 | 50 | ns | |
| RAS to Column Address Delay Time | t_{RAD} | 15 | 25 | 15 | 30 | 15 | 35 | ns | |
| CAS to RAS Precharge Time | t_{CRP} | 5 | | 5 | | 5 | | ns | |
| Row Address Set-Up Time | t_{ASR} | 0 | | 0 | | 0 | | ns | |
| Row Address Hold Time | t_{RAH} | 10 | | 10 | | 10 | | ns | |
| Column Address Set-Up Time | t_{ASC} | 0 | | 0 | | 0 | | ns | |
| Column Address Hold Time | t_{CAH} | 8 | | 10 | | 15 | | ns | |
| Column Address to RAS Lead Time | t_{RAL} | 25 | | 30 | | 35 | | ns | |
| Column Address Hold Time Referenced to RAS | t_{AR} | 40 | | 45 | | 50 | | ns | |
| Read Command Set-Up Time | t_{RCS} | 0 | | 0 | | 0 | | ns | |
| Read Command Hold Time Referenced to CAS | t_{RCH} | 0 | | 0 | | 0 | | ns | 4 |
| Read Command Hold Time Referenced to RAS | t_{RRH} | 0 | | 0 | | 0 | | ns | 4 |
| Write Command Set-Up Time | t_{WCS} | 0 | | 0 | | 0 | | ns | 8,9 |
| Write Command Hold Time | t_{WCH} | 10 | | 10 | | 15 | | ns | |
| Write Command Pulse Width | t_{WP} | 10 | | 10 | | 15 | | ns | |
| Write Command to RAS Lead Time | t_{RWL} | 13 | | 15 | | 30 | | ns | |
| Write Command to CAS Lead Time | t_{CWL} | 8 | | 10 | | 15 | | ns | |

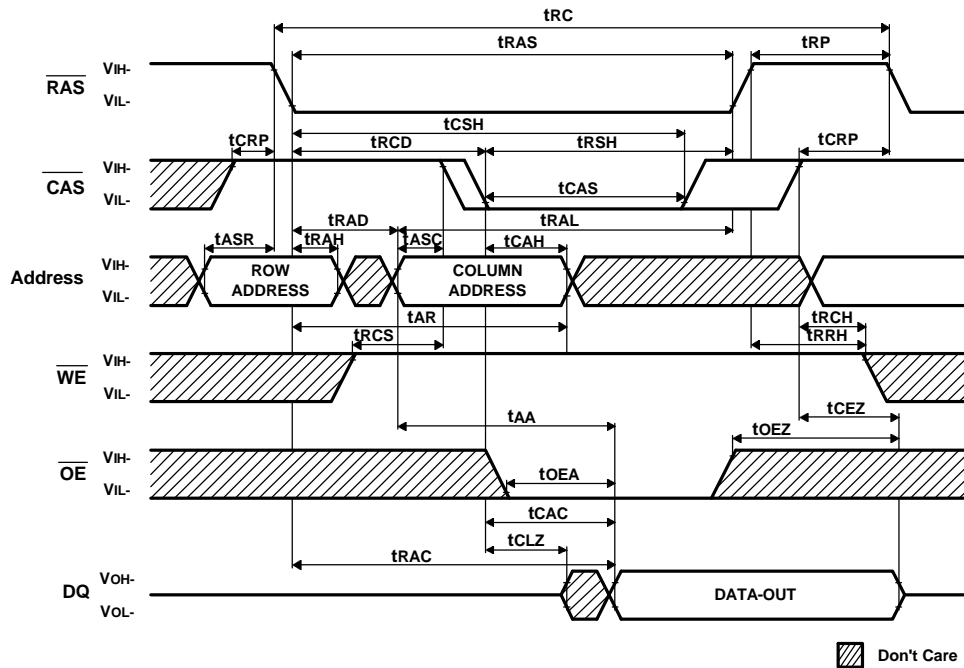
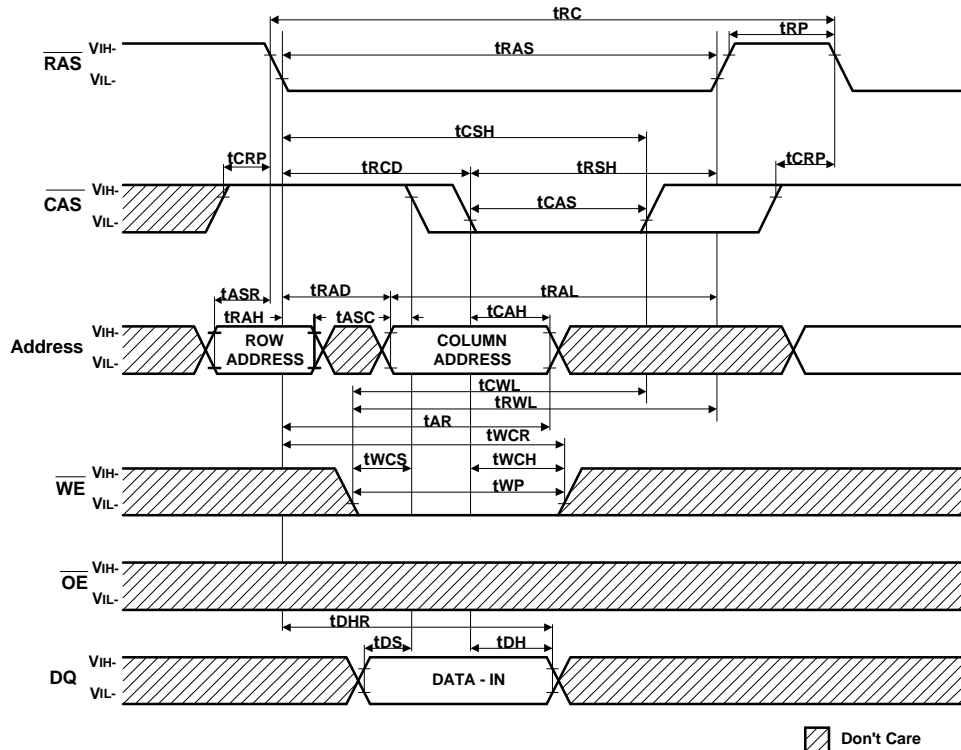
AC Characteristics

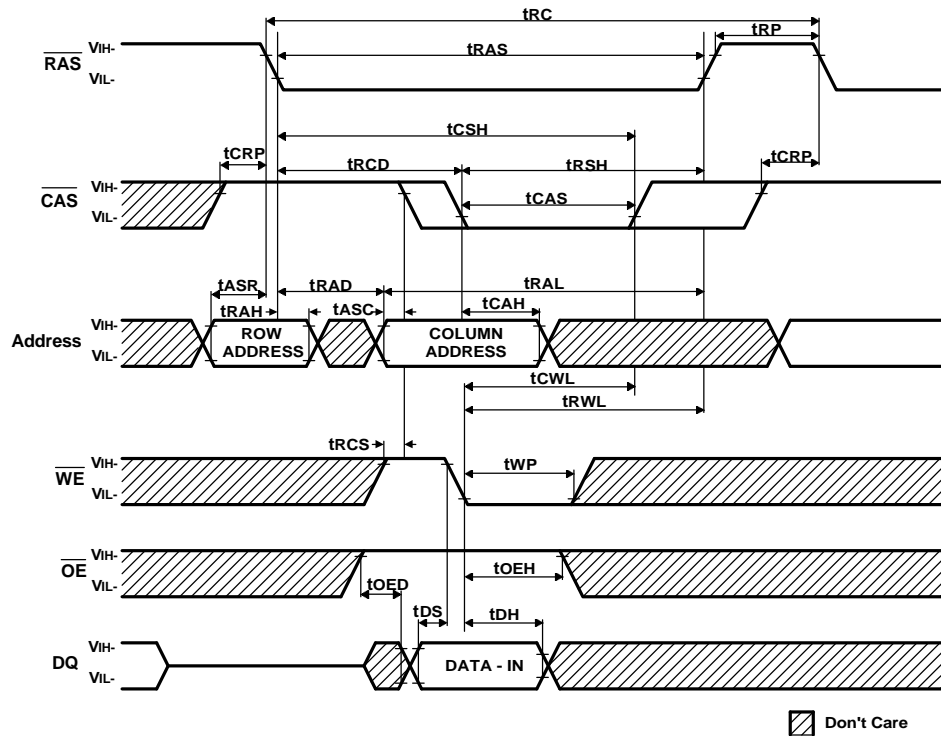
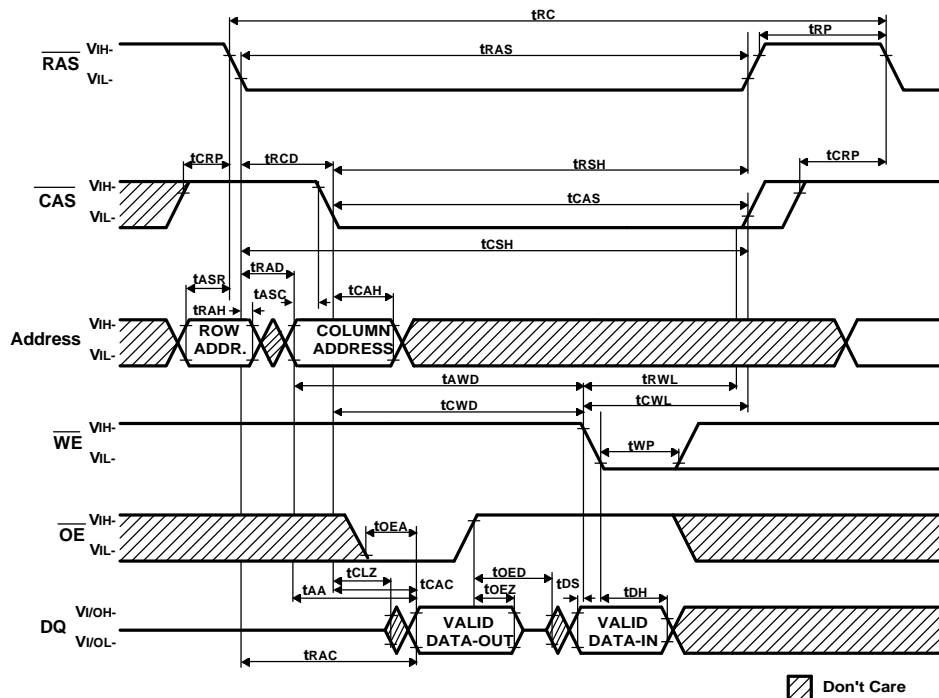
| Parameter | Symbol | 50 | | 60 | | 70 | | Unit | Notes |
|--|------------|------|------|------|------|------|------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Data Set-Up Time | t_{DS} | 0 | | 0 | | 0 | | ns | 10 |
| Data Hold Time | t_{DH} | 8 | | 10 | | 15 | | ns | 10 |
| Data Hold Time Referenced to \overline{RAS} | t_{DHR} | 40 | | 45 | | 50 | | ns | |
| \overline{RAS} to \overline{WE} Delay Time | t_{RWD} | 67 | | 79 | | 94 | | ns | |
| \overline{CAS} to \overline{WE} Delay Time | t_{CWD} | 30 | | 34 | | 44 | | ns | |
| Column Address to \overline{WE} Delay Time | t_{AWD} | 42 | | 49 | | 59 | | ns | |
| \overline{CAS} Precharge to \overline{WE} Delay | t_{CPWD} | 47 | | 54 | | 64 | | ns | |
| \overline{RAS} to \overline{CAS} Precharge Time | t_{RPC} | 5 | | 5 | | 5 | | ns | |
| \overline{CAS} precharge time (\overline{CAS} Before \overline{RAS} counter test cycle) | t_{CPT} | 20 | | 20 | | 25 | | ns | |
| Access Time from \overline{CAS} Precharge | t_{CPA} | | 28 | | 35 | | 40 | ns | |
| EDO Page Mode Cycle Time | t_{PC} | 20 | | 25 | | 30 | | ns | |
| EDO Page Mode Read-Modify-Write Cycle Time | t_{PRWC} | 47 | | 56 | | 71 | | ns | |
| \overline{CAS} Precharge Time (EDO Page Mode) | t_{CP} | 8 | | 10 | | 10 | | ns | |
| \overline{RAS} Pulse Width (EDO Page Mode Only) | t_{RASP} | 50 | 100k | 60 | 100k | 70 | 100k | ns | |
| \overline{RAS} Hold Time from \overline{CAS} precharge | t_{RHCP} | 30 | | 35 | | 40 | | ns | |
| Access Time from \overline{OE} | t_{OEA} | | 13 | | 15 | | 20 | ns | |
| \overline{OE} to Data Delay Time | t_{OED} | 13 | | 15 | | 20 | | ns | |
| \overline{OE} to Output Low-Z | t_{OLZ} | 3 | | 3 | | 3 | | ns | |
| \overline{OE} to Output High-Z | t_{OEZ} | 3 | 13 | 3 | 15 | 3 | 20 | ns | |
| \overline{WE} to Data Delay | t_{WED} | 15 | | 15 | | 20 | | ns | |
| \overline{OE} Command Hold Time | t_{OEH} | 13 | | 15 | | 20 | | ns | |
| Data Output Hold after \overline{CAS} low | t_{DOH} | 5 | | 5 | | 5 | | ns | |
| \overline{RAS} to Output High-Z | t_{REZ} | 3 | 13 | 3 | 15 | 3 | 20 | ns | |
| \overline{WE} to Output High-Z | t_{WEZ} | 3 | 13 | 3 | 15 | 3 | 20 | ns | |
| \overline{OE} to \overline{CAS} Hold Time | t_{OCH} | 5 | | 5 | | 5 | | ns | |
| \overline{CAS} Hold Time to \overline{OE} | t_{CHO} | 5 | | 5 | | 5 | | ns | |
| \overline{OE} Precharge Time | t_{OEP} | 5 | | 5 | | 5 | | ns | |
| \overline{WE} Puts width (EDO mixed read write cycle) | t_{WPE} | 5 | | 5 | | 5 | | ns | |
| \overline{CAS} Set-Up Time for \overline{CAS} -before- \overline{RAS} Cycle | t_{CSR} | 5 | | 5 | | 5 | | ns | |
| \overline{CAS} Hold Time for \overline{CAS} -before- \overline{RAS} Cycle | t_{CHR} | 10 | | 10 | | 15 | | ns | |

| Parameter | Symbol | 50 | | 60 | | 70 | | Unit | Notes |
|---|-------------------|------|------|------|------|------|------|---------------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| WE to RAS precharge time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ refresh) | t_{WRP} | 10 | | 10 | | 10 | | ns | |
| WE to RAS hold time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ refresh) | t_{WRH} | 10 | | 10 | | 10 | | ns | |
| Transition Time | t_{T} | 2 | 50 | 2 | 50 | 2 | 50 | ns | 11 |
| Refresh Period (1,024 cycles) | t_{REF} | | 16 | | 16 | | 16 | ms | |
| Refresh Period (L-Version) | t_{REF} | | 128 | | 128 | | 128 | ms | |
| RAS Pulse Width ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self refresh) | t_{RASS} | 100 | | 100 | | 100 | | μs | |
| RAS precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self refresh) | t_{RPS} | 90 | | 110 | | 130 | | ns | |
| CAS Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self refresh) | t_{CHS} | 50 | | 50 | | 50 | | ns | |

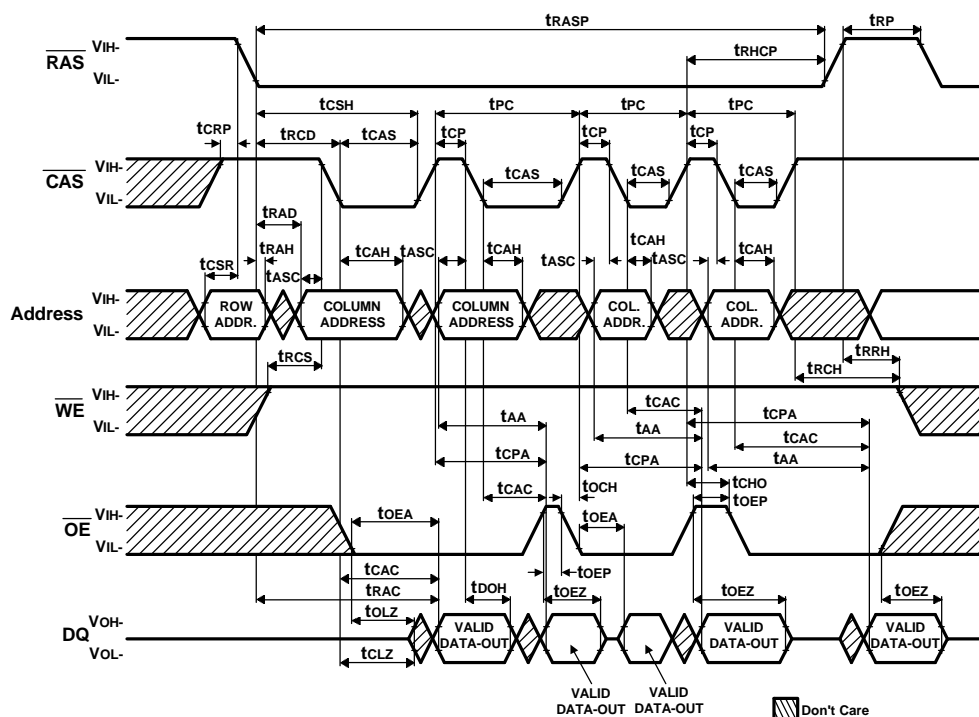
Notes:

1. Measure with a load equivalent to one TTL input and 100 pF.
2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max.})$. If t_{RCD} is greater than $t_{RCD}(\text{max.})$, access time will be t_{AA} dominant.
3. Assumes that $t_{RAD} \leq t_{RAD}(\text{max.})$. If t_{RAD} is greater than $t_{RAD}(\text{max.})$, access time will be controlled by t_{CAC} .
4. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle.
5. Access time is determined by the longest of t_{AA} , t_{CAC} and t_{CPA} .
6. Assumes that $t_{RAD} \geq t_{RAD}(\text{max.})$.
7. Assumes that $t_{RCD} \geq t_{RCD}(\text{max.})$.
8. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters.
9. $t_{WCS}(\text{min.})$ must be satisfied in an Early Write Cycle.
10. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{\text{CAS}}$ or $\overline{\text{WE}}$.
11. t_T is measured between $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$. AC-measurements assume $t_T = 2 \text{ ns}$.

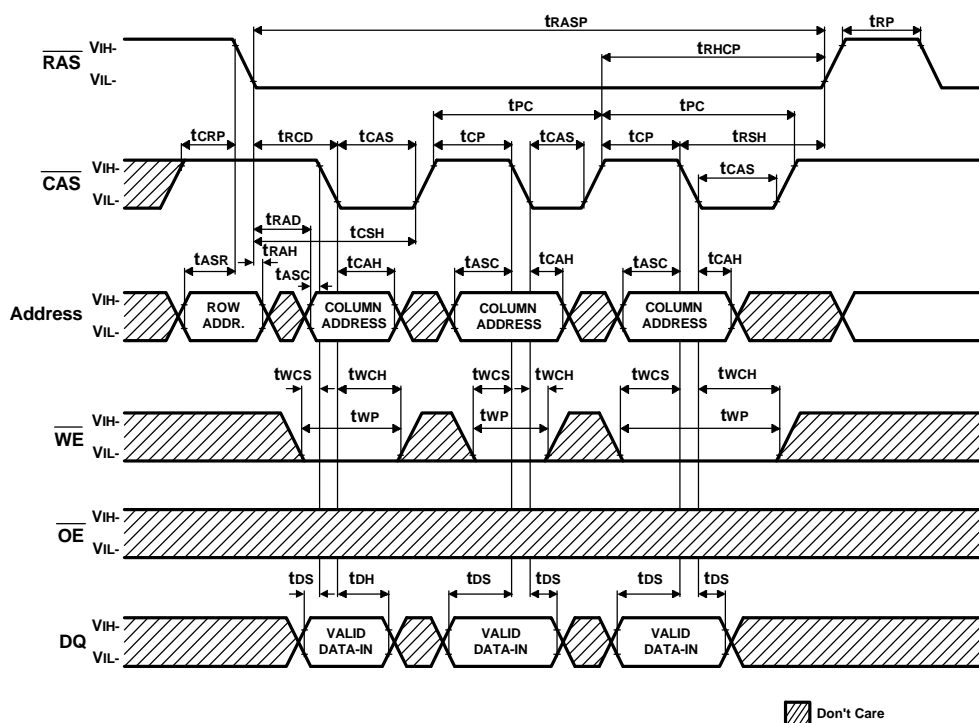
Read Cycle

Early Write Cycle NOTE : D_{OUT} = OPEN


OE Controlled Write Cycle NOTE : D_{OUT} = OPEN

Read - Modify - Write Cycle


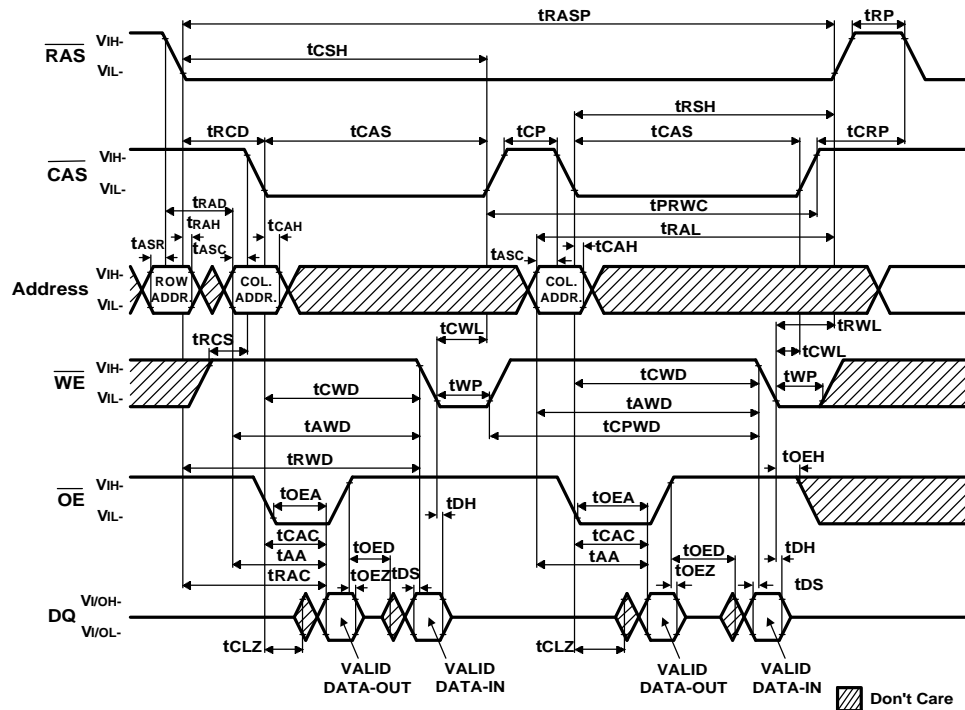
EDO Page Mode Read Cycle



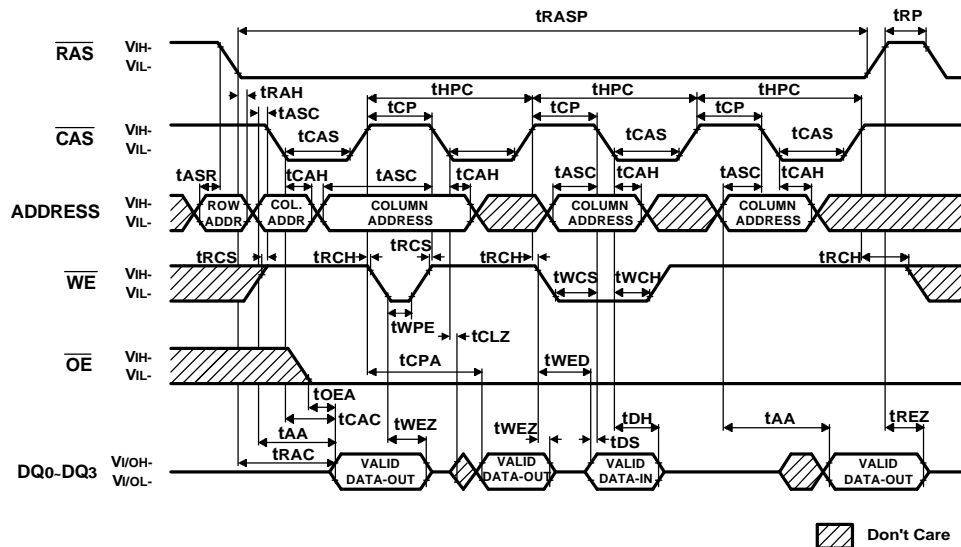
EDO Page Mode Early Write Cycle

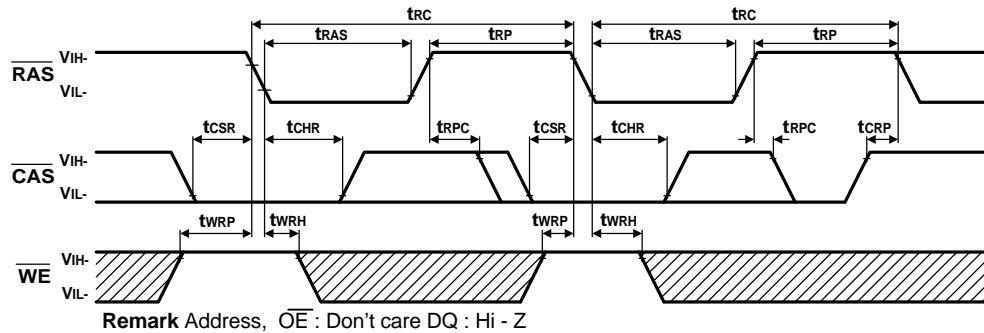
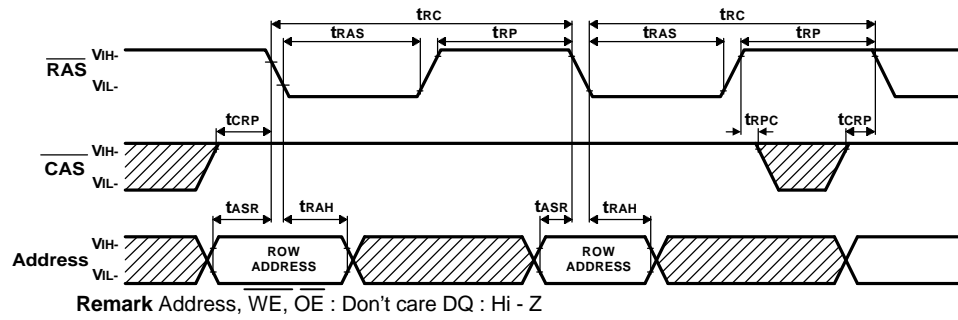
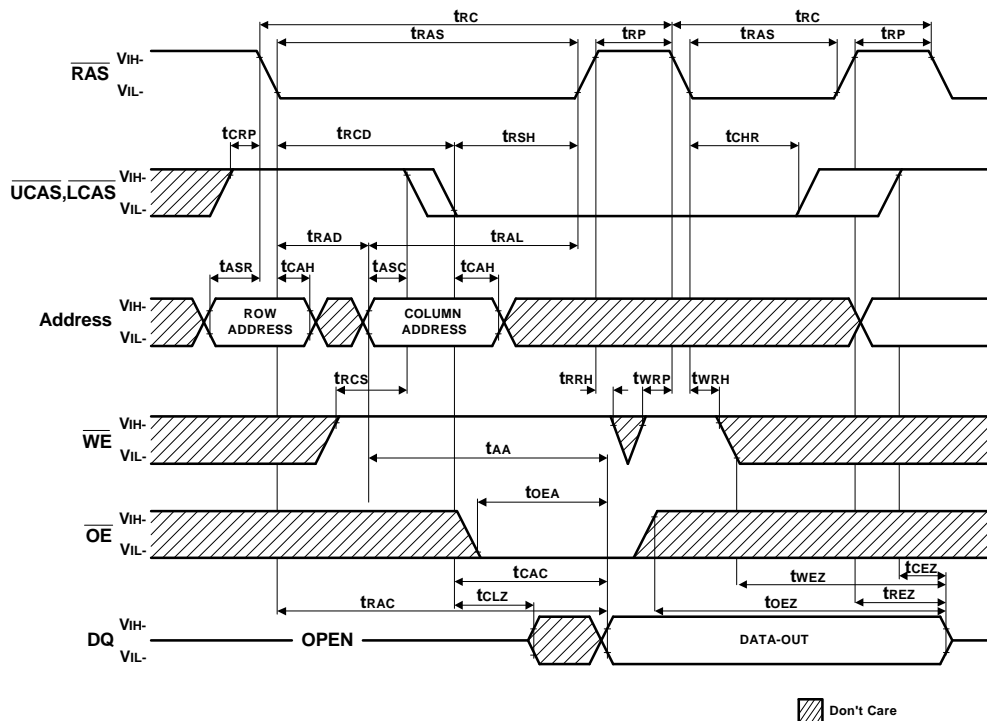


EDO Page Mode Read - Modify - Write Cycle

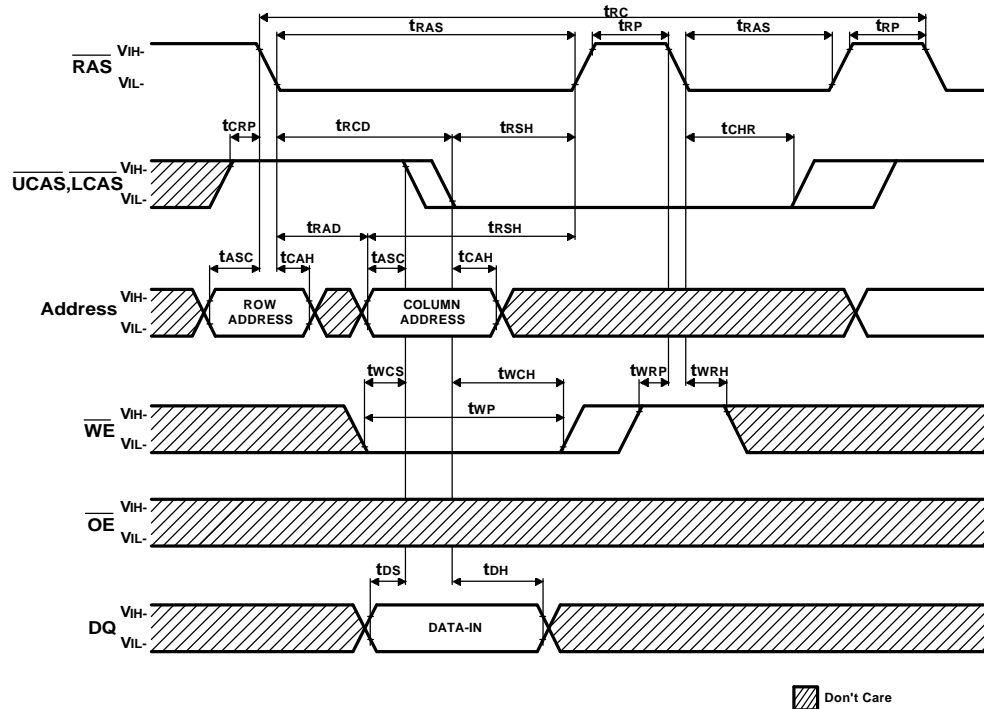


EDO Page Read And Write Mixed Ccycle



CAS - Before - RAS Refresh Cycle

RAS-Only Refresh Cycle

Hidden Refresh Cycle (Read)


Hidden Refresh Cycle (Write) NOTE : D_{OUT} = OPEN





Dec. 2001 (Rev. 1.1)

The diagram illustrates the timing relationships for three memory access modes: Read Cycle, Write Cycle, and Read-Modify-Write. It shows the signals RAS, CAS, Address, WE, OE, DQ, and VIOH-VIOL with their respective high and low levels (VIH, VIL, VOH, VOL).

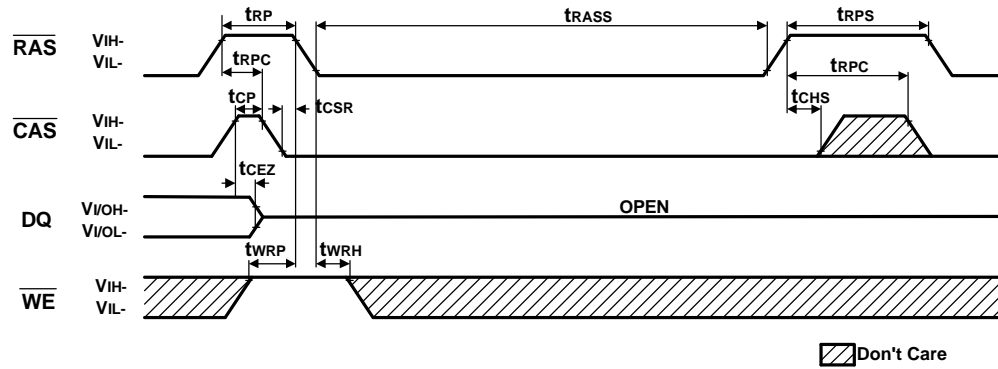
Read Cycle: Shows the sequence from RAS and CAS setup to data output. Key parameters include t_{CSR} , t_{CHR} , t_{CPT} , t_{CAS} , t_{ASC} , t_{CAH} , t_{RAL} , t_{TRP} , t_{TRH} , t_{TRCH} , t_{WRP} , t_{WRH} , t_{RCS} , t_{TAA} , t_{CAC} , t_{TOEA} , t_{CLZ} , t_{OEZ} , and t_{CEZ} .

Write Cycle: Shows the sequence from RAS and CAS setup to data input. Key parameters include t_{WRP} , t_{WRH} , t_{WCS} , t_{TWL} , t_{TCH} , t_{WTP} , t_{TDS} , and t_{TDH} .

Read-Modify-Write: Shows the sequence for reading, modifying, and writing data. Key parameters include t_{RCS} , t_{TAWD} , t_{TCWD} , t_{TCWL} , t_{TRWL} , t_{WTP} , t_{TCAC} , t_{TAA} , t_{TOEA} , t_{TOED} , t_{TDH} , t_{TCLZ} , t_{TOEZ} , and t_{TDS} .

Legend: \square Don't Care

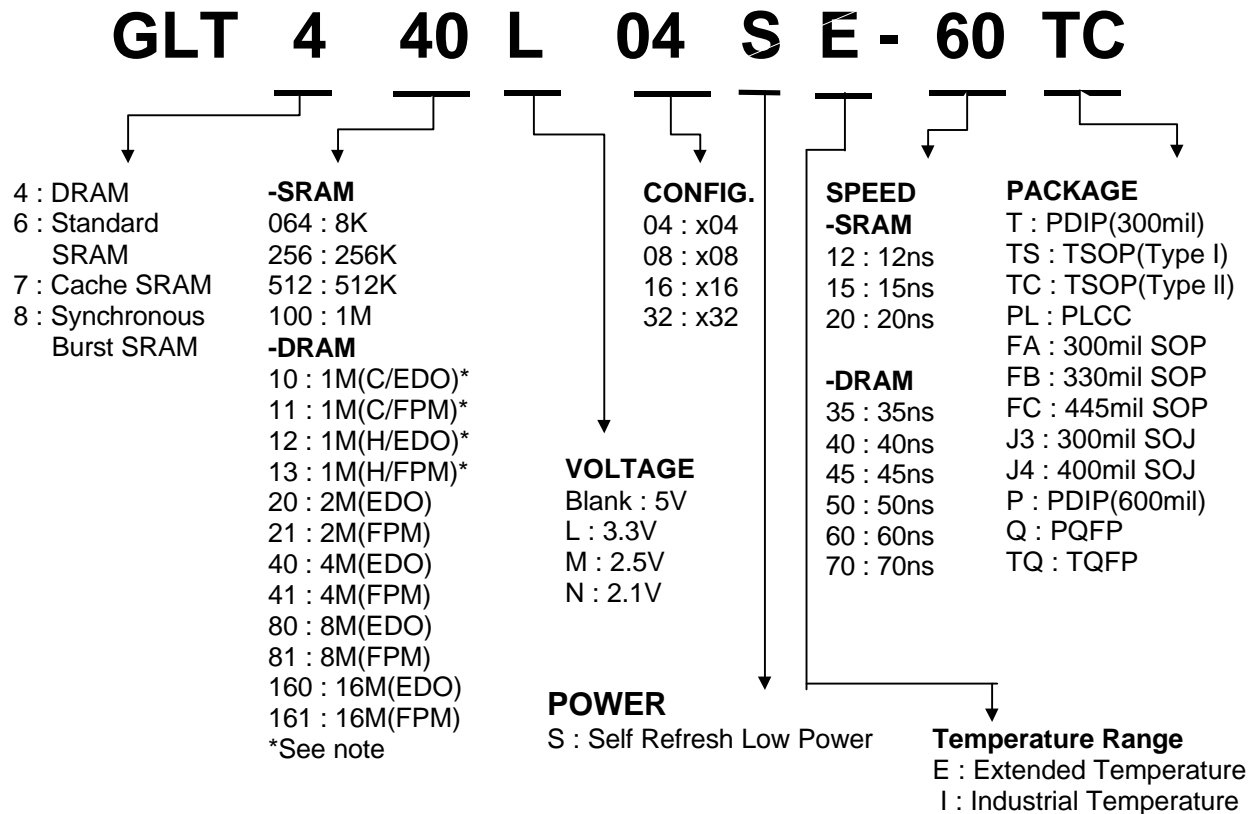
CAS-Before-RAS Self Refresh Cycle



NOTE : OE , Address = Don't Care

Ordering Information

| Part Number | SPEED | POWER | FEATURE | TEMPERATURE | PACKAGE |
|--------------------|--------------|------------------------|----------------|--------------------|-----------------------|
| GLT440L04-50J3 | 50ns | Normal | EDO | Commercial | SOJ 300mil 26(20)L |
| GLT440L04-60J3 | 60ns | Normal | EDO | Commercial | SOJ 300mil 26(20)L |
| GLT440L04-70J3 | 70ns | Normal | EDO | Commercial | SOJ 300mil 26(20)L |
| GLT440L04-50TC | 50ns | Normal | EDO | Commercial | TSOPII 300mil 26(20)L |
| GLT440L04-60TC | 60ns | Normal | EDO | Commercial | TSOPII 300mil 26(20)L |
| GLT440L04-70TC | 70ns | Normal | EDO | Commercial | TSOPII 300mil 26(20)L |
| GLT440L04E-50J3 | 50ns | Normal | EDO | Extended | SOJ 300mil 26(20)L |
| GLT440L04E-60J3 | 60ns | Normal | EDO | Extended | SOJ 300mil 26(20)L |
| GLT440L04E-70J3 | 70ns | Normal | EDO | Extended | SOJ 300mil 26(20)L |
| GLT440L04E-50TC | 50ns | Normal | EDO | Extended | TSOPII 300mil 26(20)L |
| GLT440L04E-60TC | 60ns | Normal | EDO | Extended | TSOPII 300mil 26(20)L |
| GLT440L04E-70TC | 70ns | Normal | EDO | Extended | TSOPII 300mil 26(20)L |
| GLT440L04S-50J3 | 50ns | Self Refresh Low Power | EDO | Commercial | SOJ 300mil 26(20)L |
| GLT440L04S-60J3 | 60ns | Self Refresh Low Power | EDO | Commercial | SOJ 300mil 26(20)L |
| GLT440L04S-70J3 | 70ns | Self Refresh Low Power | EDO | Commercial | SOJ 300mil 26(20)L |
| GLT440L04S-50TC | 50ns | Self Refresh Low Power | EDO | Commercial | TSOPII 300mil 26(20)L |
| GLT440L04S-60TC | 60ns | Self Refresh Low Power | EDO | Commercial | TSOPII 300mil 26(20)L |
| GLT440L04S-70TC | 70ns | Self Refresh Low Power | EDO | Commercial | TSOPII 300mil 26(20)L |
| GLT440L04SE-50J3 | 50ns | Self Refresh Low Power | EDO | Extended | SOJ 300mil 26(20)L |
| GLT440L04SE-60J3 | 60ns | Self Refresh Low Power | EDO | Extended | SOJ 300mil 26(20)L |
| GLT440L04SE-70J3 | 70ns | Self Refresh Low Power | EDO | Extended | SOJ 300mil 26(20)L |
| GLT440L04SE-50TC | 50ns | Self Refresh Low Power | EDO | Extended | TSOPII 300mil 26(20)L |
| GLT440L04SE-60TC | 60ns | Self Refresh Low Power | EDO | Extended | TSOPII 300mil 26(20)L |
| GLT440L04SE-70TC | 70ns | Self Refresh Low Power | EDO | Extended | TSOPII 300mil 26(20)L |

Parts Numbers (Top Mark) Definition :


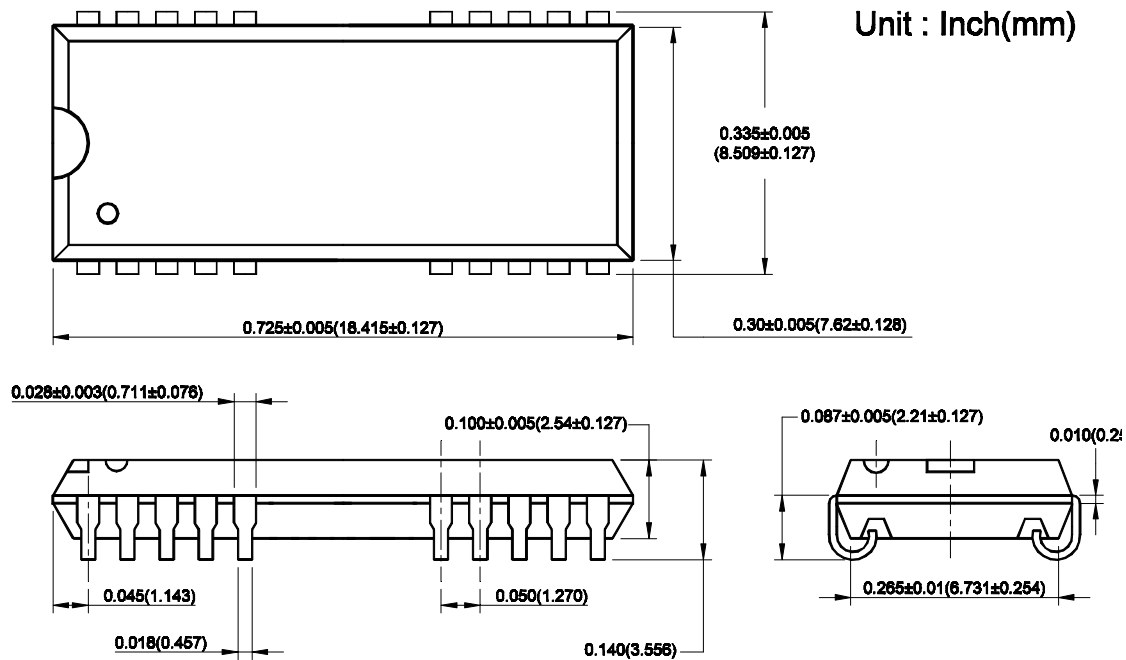
Note : C→CDROM , H→HDD.

Example :

1. GLT710008-15T 1Mbit(128Kx8)15ns 5V SRAM PDIP(300mil)Package type.
2. GLT44016-40J4 4Mbit(256Kx16)40ns 5V DRAM SOJ(400mil)Package type.

Package Information

300mil 20/26 Lead Thin Small Outline Package SOJ



300mil 20/26 Lead Thin Small Outline Package (TSOP) TYPE II

Unit : Inch

