

## Features :

- \* 524,288 words by 8 bits organization.
- \* Fast access time and cycle time.
- \* Low power dissipation.  
Operating Current-150mA max.  
TTL Standby Current-2mA max.
- \* Read-Modify-Write,  $\overline{\text{RAS}}$ -Only Refresh,  $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  Refresh, Hidden Refresh and Test Mode Capability.
- \* 1024 refresh cycles/16ms.
- \* Available in 28pin 400 mil SOJ
- \* Single +5.0V $\pm$ 10% Power Supply.
- \* All inputs and Outputs are TTL-compatible.
- \* Fast Page Mode supports sustained data rates up to 50MHZ.

## Description :

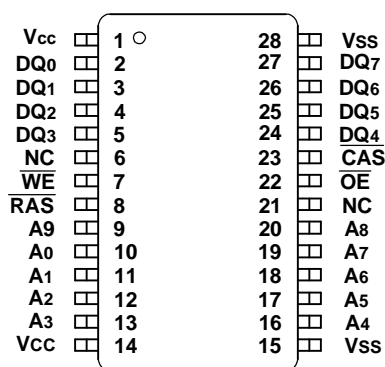
The GLT44108 is a 524,288 x 8 bit high-performance CMOS dynamic random access memory. The GLT44108 offers Fast Page mode with asymmetric address and accepts 512-cycle refresh in 8ms interval.

All inputs are TTL compatible. Fast Page Mode operation allows random access up to 512 x 8 bits within a page, with cycle times as short as 22ns.

The GLT44108 is best suited for graphics, digital signal processing and high performance peripherals.

## PIN CONFIGURATION :

**GLT44108**  
**28 Lead SOJ**

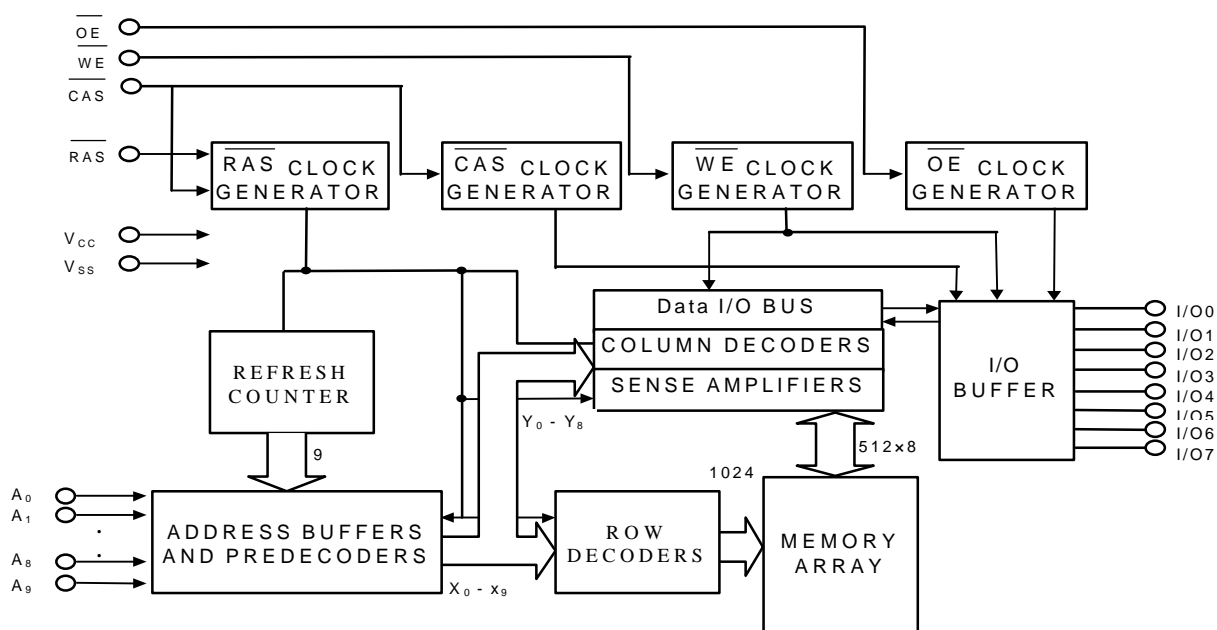


HIGH PERFORMANCE	-40	-50	-60
Max. RAS Access Time, ( $t_{RAC}$ )	40 ns	50 ns	60 ns
Max. Column Address Access Time, ( $t_{AA}$ )	20 ns	25 ns	30 ns
Min. Fast Page Mode Cycle Time, ( $t_{PC}$ )	22 ns	31 ns	40 ns
Min. Read/Write Cycle Time, ( $t_{RC}$ )	75 ns	90 ns	110 ns
Max. CAS Access Time ( $t_{CAC}$ )	12 ns	13 ns	15 ns

### Pin Descriptions:

Name	Function
$A_0 - A_9$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$DQ_0 - DQ_7$	Data Inputs / Outputs
$V_{CC}$	+5V Power Supply
$V_{SS}$	Ground

### Block Diagram:



### Absolute Maximum Ratings\*

Operating Temperature, T<sub>A</sub> (ambient)  
 .....-10°C to +80°C  
 Storage Temperature(plastic)....-55°C to +150°C  
 Voltage Relative to V<sub>SS</sub>.....-1.0V to + 7.0V  
 Short Circuit Output Current.....50mA  
 Power Dissipation.....1.0W

\*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

### Capacitance\*

T<sub>A</sub>=25°C, V<sub>CC</sub>=5V±10%, V<sub>SS</sub>=0V

Symbol	Parameter	Max.	Unit
C <sub>IN1</sub>	Address Input	5	pF
C <sub>IN2</sub>	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$	7	pF
C <sub>OUT</sub>	Data Input/Output	7	pF

\*Note: Capacitance is sampled and not 100% tested

### Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 200μs and then, execute eight  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  or  $\overline{\text{RAS}}$  only refresh cycles as dummy cycles to initialize internal circuit.

### DC and Operating Characteristics (1-2)

TA = 0°C to 70°C, V<sub>CC</sub>=5V±10%, V<sub>SS</sub>=0V, unless otherwise specified.

Sym.	Parameter	Test Conditions	Access Time	Min.	Typ	Max.	Unit	Notes
I <sub>LI</sub>	Input Leakage Current (any input pin)	0V ≤ V <sub>IN</sub> ≤ 5.5V (All other pins not under test=0V)		-10		+10	μA	
I <sub>LO</sub>	Output Leakage Current (for High-Z State)	0V ≤ V <sub>out</sub> ≤ 5.5V Output is disabled (Hiz)		-10		+10	μA	
I <sub>CC1</sub>	Operating Current, Random READ/WRITE	t <sub>RC</sub> = t <sub>RC</sub> (min.)	t <sub>RAC</sub> = 40ns t <sub>RAC</sub> = 50ns t <sub>RAC</sub> = 60ns			150 140 120	mA	1,2
I <sub>CC2</sub>	Standby Current,(TTL)	RAS, CAS, at V <sub>IH</sub> other inputs ≥ V <sub>SS</sub>				2	mA	
I <sub>CC3</sub>	Refresh Current, RAS -Only	RAS cycling, CAS at V <sub>IH</sub> t <sub>RC</sub> = t <sub>RC</sub> (min.)	t <sub>RAC</sub> = 40ns t <sub>RAC</sub> = 50ns t <sub>RAC</sub> = 60ns			150 140 120	mA	2
I <sub>CC4</sub>	Operating Current, FAST Page Mode	RAS at V <sub>IL</sub> , CAS ,address cycling:t <sub>PC</sub> =t <sub>PC</sub> (min.)	t <sub>RAC</sub> = 40ns t <sub>RAC</sub> = 50ns t <sub>RAC</sub> = 60ns			150 140 120	mA	1,2
I <sub>CC5</sub>	Refresh Current, CAS Before RAS	RAS, CAS, address cycling: t <sub>RC</sub> =t <sub>RC</sub> (min.)	t <sub>RAC</sub> = 40ns t <sub>RAC</sub> = 50ns t <sub>RAC</sub> = 60ns			150 140 120	mA	1
I <sub>CC6</sub>	Standby Current, (CMOS)	RAS ≥ V <sub>CC</sub> -0.2V, CAS ≥ V <sub>CC</sub> -0.2V, All other inputs ≥ V <sub>SS</sub>				1	mA	
V <sub>IL</sub>	Input Low Voltage			-1		+0.8	V	3
V <sub>IH</sub>	Input High Voltage			2.4		V <sub>CC</sub> +1	V	3
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 4.2mA				0.4	V	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -5mA		2.4			V	

#### Notes:

- I<sub>CC</sub> is dependent on output loading when the device output is selected. Specified I<sub>CC(max.)</sub> is measured with the output open.
- I<sub>CC</sub> is dependent upon the number of address transitions specified. I<sub>CC(max.)</sub> is measured with a maximum of one transition per address cycle in random Read/Write and Fast Page Mode.
- Specified V<sub>IL(min.)</sub> is steady state operation. During transitions, V<sub>IL(min.)</sub> may undershoot to -1.0V for a period not to exceed 20ns. All AC parameters are measured with V<sub>IL(min.)</sub> ≥ V<sub>SS</sub> and V<sub>IH(max.)</sub> ≤ V<sub>CC</sub>.

### AC Characteristics (0°C ≤ T<sub>A</sub> ≤ 70°C, See note 1,2)

Test condition: V<sub>CC</sub>=5.0V±10%, V<sub>IH</sub>/V<sub>IL</sub>=2.4V/0.8V, V<sub>OH</sub>/V<sub>OL</sub>=2.0V/0.8V

Parameter	Symbol	40 ns		50 ns		60 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t <sub>RC</sub>	75	-	90	-	110	-	ns	
Read Midify Write Cycle Time	t <sub>RWC</sub>	120	-	140	-	160	-	ns	
Access Time from $\overline{\text{RAS}}$	t <sub>RAC</sub>	-	40	-	50	-	60	ns	3,4
Access Time from CAS	t <sub>CAC</sub>	-	12	-	13	-	15	ns	3,4
Access Time from Column Address	t <sub>AA</sub>	-	20	-	25	-	30	ns	3,4
CAS to Output in Low-Z	t <sub>CLZ</sub>	0	-	0	-	0	-	ns	3
Output Buffer Turn-off Delay from $\overline{\text{CAS}}$	t <sub>OFF</sub>	0	8	0	10	0	13	ns	7
Transition Time(Rise and Fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	2
RAS Precharge Time	t <sub>RP</sub>	25	-	30	-	40	-	ns	
RAS Pulse Width	t <sub>RAS</sub>	40	10000	50	10000	60	10000	ns	
RAS Hold Time	t <sub>RSH</sub>	12	-	13	-	15	-	ns	
CAS Hold Time	t <sub>CSH</sub>	40	-	50	-	60	-	ns	
CAS Pulse Width	t <sub>CAS</sub>	12	10000	13	10000	15	10000	ns	
RAS to CAS Delay Time	t <sub>RCD</sub>	16	30	18	37	20	45	ns	4
RAS to Column Address Delay Time	t <sub>RAD</sub>	11	22	13	25	15	30	ns	4
CAS to RAS Precharge Time	t <sub>CRP</sub>	5	-	5	-	5	-	ns	8
Row Address Setup Time	t <sub>ASR</sub>	0	-	0	-	0	-	ns	
Row Address Hold Time	t <sub>RAH</sub>	6	-	8	-	10	-	ns	
Column Address Setup Time	t <sub>ASC</sub>	0	-	0	-	0	-	ns	
Column Address Hold Time	t <sub>CAH</sub>	6	-	8	-	10	-	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t <sub>AR</sub>	30	-	40	-	45	-	ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t <sub>RAL</sub>	20	-	25	-	30	-	ns	
Read Command Setup Time	t <sub>RCS</sub>	0	-	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t <sub>RRH</sub>	0	-	0	-	0	-	ns	9
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t <sub>RCH</sub>	0	-	0	-	0	-	ns	9
WE Hold Time Referenced to $\overline{\text{CAS}}$	t <sub>WCH</sub>	6	-	7	-	10	-	ns	10
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t <sub>WCR</sub>	30	-	40	-	45	-	ns	5

Parameter	Symbol	40 ns		50 ns		60 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{WE}}$ Pulse Width	$t_{\text{WP}}$	6	-	7	-	10	-	ns	10
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	$t_{\text{RWL}}$	13	-	17	-	15	-	ns	
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{CAS}}$	$t_{\text{CWL}}$	13	-	14	-	15	-	ns	
Data-In Setup Time	$t_{\text{DS}}$	0	-	0	-	0	-	ns	11
Data-In Hold Time	$t_{\text{DH}}$	6	-	7	-	10	-	ns	11
Data Hold Time Referenced to $\overline{\text{RAS}}$	$t_{\text{DHR}}$	33	-	40	-	45	-	ns	6
Refresh Time(256cycles)	$t_{\text{REF}}$	-	8	-	8	-	8	ms	
$\overline{\text{WE}}$ Setup Time	$t_{\text{WCS}}$	0	-	0	-	0	-	ns	5
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	$t_{\text{RWD}}$	60	-	70	-	85	-	ns	5
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	$t_{\text{CWD}}$	28	-	33	-	38	-	ns	5
Column Address to $\overline{\text{WE}}$ Delay Time	$t_{\text{AWD}}$	38	-	43	-	53	-	ns	5
$\overline{\text{CAS}}$ Setup Time( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	$t_{\text{CSR}}$	5	-	5	-	5	-	ns	
$\overline{\text{CAS}}$ Hold Time( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	$t_{\text{CHR}}$	10	-	10	-	10	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	$t_{\text{RPC}}$	5	-	5	-	5	-	ns	
$\overline{\text{CAS}}$ Precharge Time(CBR Counter Test Cycle)	$t_{\text{CPT}}$	20	-	20	-	20	-	ns	
Access Time from $\overline{\text{CAS}}$ Precharge	$t_{\text{CPA}}$	-	25	-	30	-	35	ns	3
Fast Page mode Read/Write Cycle Time	$t_{\text{PC}}$	30	-	35	-	40	-	ns	
Fast Page mode Read Modify Write Cycle Time	$t_{\text{PRWC}}$	65	-	80	-	90	-	ns	
$\overline{\text{CAS}}$ Precharge Time(Fast Page mode)	$t_{\text{CP}}$	7	-	8	-	10	-	ns	
$\overline{\text{RAS}}$ Pulse Width(Fast Page mode)	$t_{\text{RASP}}$	40	125000	50	125000	60	125000	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	$t_{\text{RHCP}}$	25	-	30	-	35	-	ns	
Access Time from $\overline{\text{OE}}$	$t_{\text{OEA}}$	-	10	-	13	-	15	ns	
$\overline{\text{OE}}$ to Delay Time	$t_{\text{OED}}$	8	-	10	-	13	-	ns	
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	$t_{\text{OEZ}}$	0	8	0	10	0	13	ns	7
$\overline{\text{OE}}$ Hold Time	$t_{\text{OEH}}$	0	-	0	-	0	-	ns	
$\overline{\text{WE}}$ Hold Time(Hidden Refresh Cycle)	$t_{\text{WHR}}$	15	-	15	-	15	-	ns	

## Notes

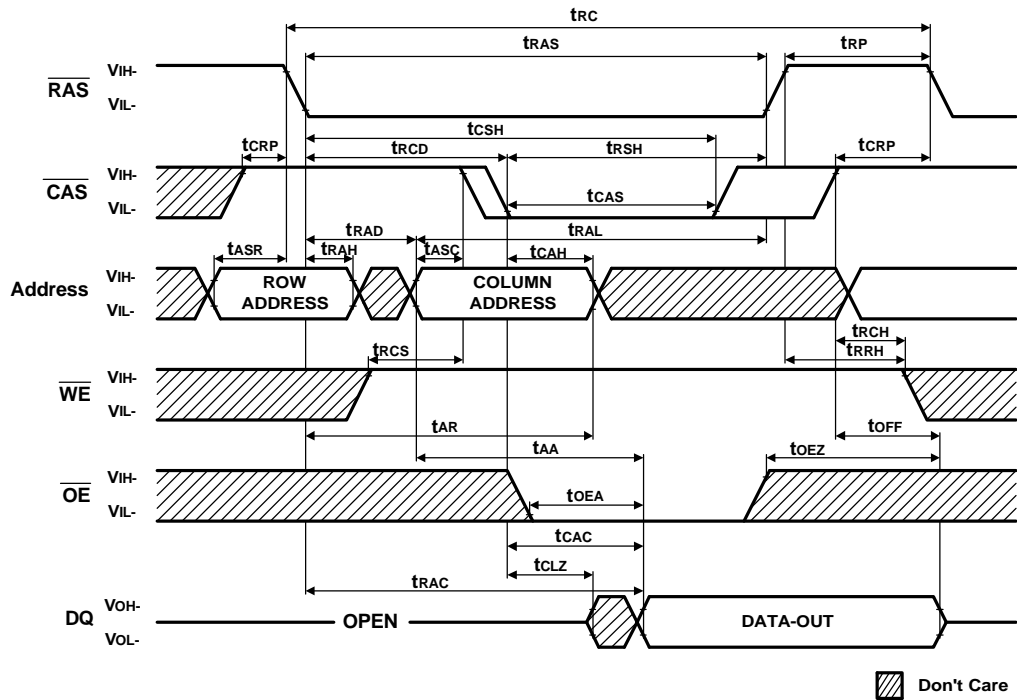
1. An initial pause of 200 $\mu$ s is required after power-up followed by any 8  $\overline{\text{RAS}}$  only Refresh or  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  Refresh cycles to initialize the internal circuit.
2.  $V_{IH(min.)}$  and  $V_{IL(min.)}$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH(min.)}$  and  $V_{IL(max.)}$  are assumed to be 5ns for all inputs.
3. Measured with an equivalent to 1 TTL loads and 50pF.
4. For read cycles, the access time is defined as follows:

Input Conditions	Access Time
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD(max.)} < t_{RAD}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$
$t_{RCD(max.)} < t_{RCD}$	$t_{CAC(MAX.)}$

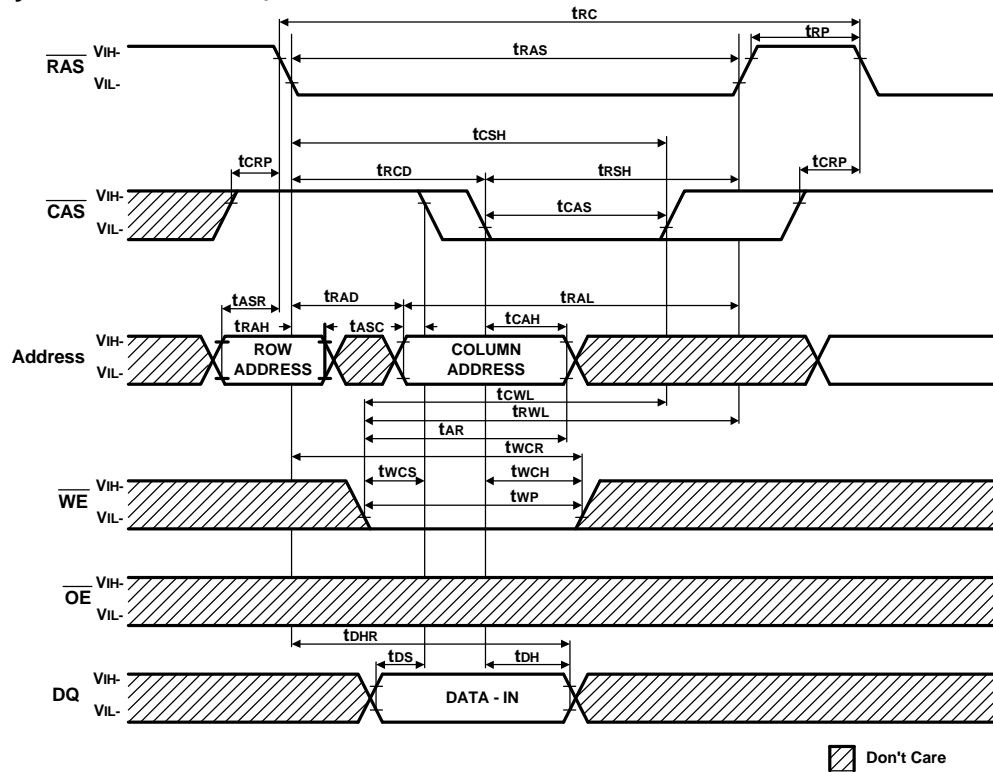
$t_{RAD(MAX.)}$  and  $t_{RCD(MAX.)}$  indicate the points which the access time changes and are not the limits of operation.

5.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If  $t_{WCS} \geq t_{WCS(min.)}$ , the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If  $t_{CWD} \geq t_{CWD(min.)}$ ,  $t_{RWD} \geq t_{RWD(min.)}$  and  $t_{AWD} \geq t_{AWD(min.)}$ , then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
6.  $t_{AR}$ ,  $t_{WCR}$ , and  $t_{DHR}$  are referenced to  $t_{RAD(max.)}$ .
7.  $t_{OFF(max.)}$  and  $t_{OEZ(max.)}$  define the time at which the output achieves the open circuit condition and are not referenced to  $V_{OH}$  or  $V_{OL}$ .
8.  $t_{CRP(min.)}$  requirement should be applicable for  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  cycle preceded by any cycles.
9. Either  $t_{RCH(min.)}$  or  $t_{RRH(min.)}$  must be satisfied for a read cycle.
10.  $t_{WP(min.)}$  is applicable for late write cycle or read modify write cycle. In early write cycles,  $t_{WCH(min.)}$  should be satisfied.
11. This specification is referenced to  $\overline{\text{CAS}}$  falling edge in early write cycles and to  $\overline{\text{WE}}$  falling edge in late write or read modify write cycles.

### Read Cycle

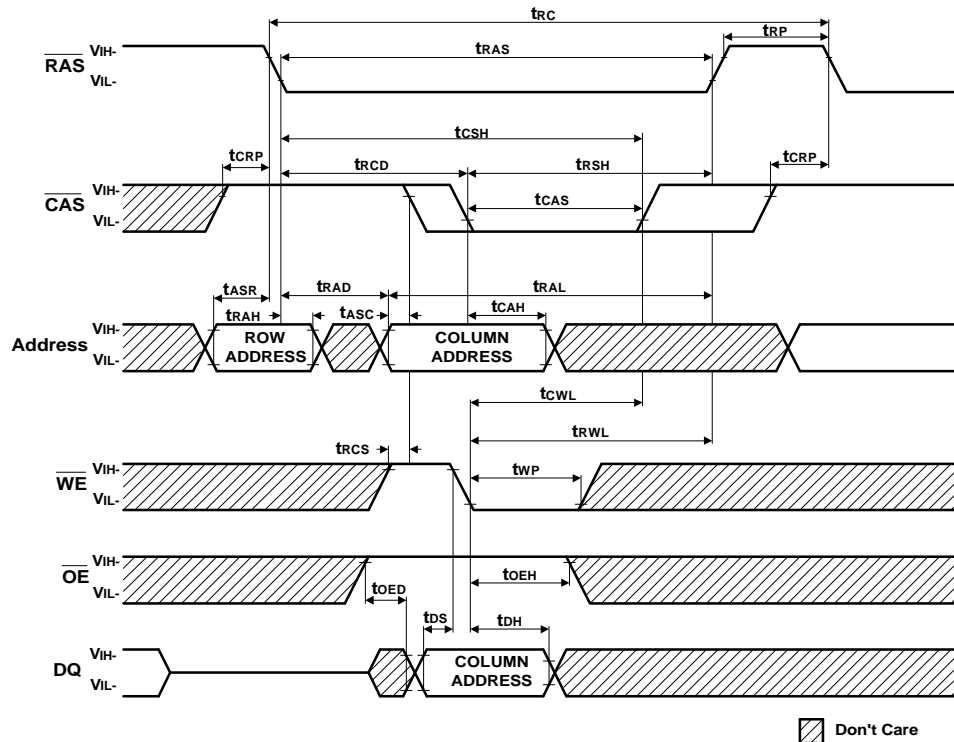


### Early Write Cycle NOTE : D<sub>OUT</sub> = Open

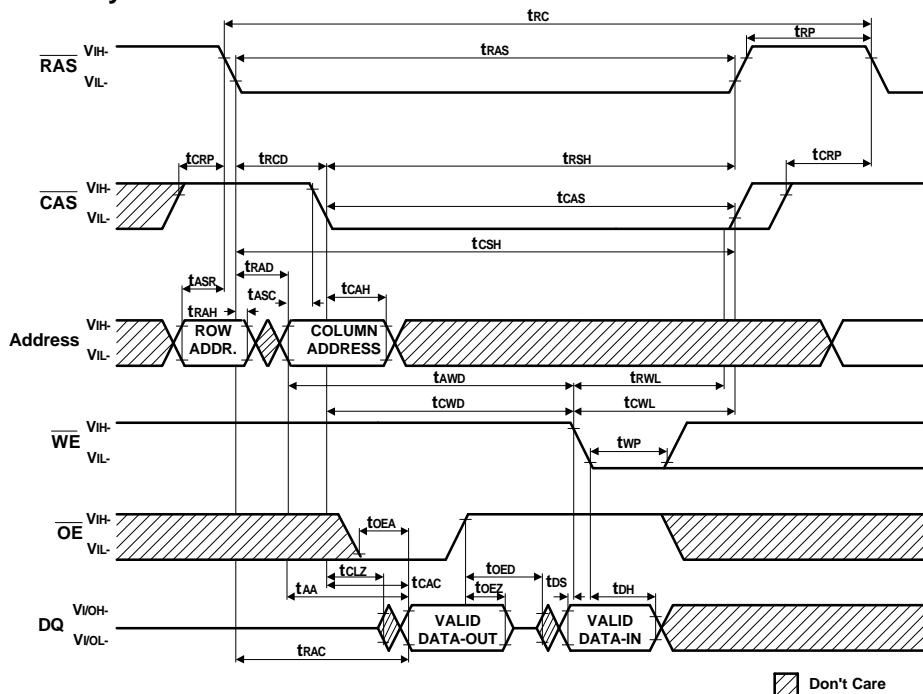




**Late Write Cycle (OE Controlled Write) NOTE : D<sub>OUT</sub> = Open**



**Read - Modify - Write Cycle**



[illegible]

The diagram illustrates the timing relationships for a memory device. The signals shown are RAS, CAS, Address, WE, OE, and DQ. The timing parameters are defined as follows:

- RAS:**  $t_{RAS}$  (RAS to output delay),  $t_{RHP}$  (RAS hold time),  $t_{RP}$  (RAS pulse width).
- CAS:**  $t_{CRP}$  (CAS to output delay),  $t_{RCD}$  (RAS to CAS delay),  $t_{CAS}$  (CAS to output delay),  $t_{CP}$  (CAS pulse width),  $t_{CSH}$  (CAS hold time),  $t_{SH}$  (CAS to output delay).
- Address:**  $t_{ASR}$  (Address to output delay),  $t_{RAH}$  (Row Address Hold),  $t_{ASC}$  (Address to output delay),  $t_{CAH}$  (Column Address Hold),  $t_{SC}$  (Address to output delay),  $t_{CAH}$  (Column Address Hold),  $t_{SC}$  (Address to output delay),  $t_{CAH}$  (Column Address Hold).
- WE:**  $t_{WCS}$  (WE to output delay),  $t_{WCH}$  (WE to output delay),  $t_{WP}$  (WE pulse width),  $t_{CWL}$  (WE to output delay),  $t_{RWL}$  (WE to output delay).
- OE:**  $t_{DS}$  (Output delay),  $t_{DH}$  (Output delay),  $t_{DS}$  (Output delay),  $t_{DS}$  (Output delay),  $t_{DS}$  (Output delay),  $t_{DS}$  (Output delay).
- DQ:**  $t_{DS}$  (Output delay),  $t_{DH}$  (Output delay),  $t_{DS}$  (Output delay),  $t_{DS}$  (Output delay),  $t_{DS}$  (Output delay),  $t_{DS}$  (Output delay).

The diagram also includes a legend for "Don't Care" states, indicated by a shaded box.

[illegible]

The diagram illustrates the timing relationships for a 2D array memory device. It shows the signals  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ , Address,  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ , and DQ (Data Out/In) over time. The signals are divided into three main sections: Row Address Strobe (RAS), Column Address Strobe (CAS), and Data Transfer (DQ).

**Signals and Timing Parameters:**

- $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$ :**
  - $t_{\text{RSH}}$ : RAS setup time before CAS.
  - $t_{\text{RCD}}$ : RAS to CAS delay.
  - $t_{\text{CAS}}$ : CAS setup time before RAS.
  - $t_{\text{RCS}}$ : RAS to CAS delay.
  - $t_{\text{RSH}}$ : RAS setup time before CAS.
  - $t_{\text{RCD}}$ : RAS to CAS delay.
  - $t_{\text{CAS}}$ : CAS setup time before RAS.
  - $t_{\text{RCS}}$ : RAS to CAS delay.
- Address:**
  - $t_{\text{ASR}}$ : Address setup time before RAS.
  - $t_{\text{RAH}}$ : Address hold time after RAS.
  - $t_{\text{CAH}}$ : Address hold time after CAS.
  - $t_{\text{ASC}}$ : Address setup time before CAS.
  - $t_{\text{CAH}}$ : Address hold time after CAS.
- $\overline{\text{WE}}$  (Write Enable):**
  - $t_{\text{WDL}}$ : Write data latency.
  - $t_{\text{WPL}}$ : Write pulse width.
  - $t_{\text{WDL}}$ : Write data latency.
  - $t_{\text{WPL}}$ : Write pulse width.
- $\overline{\text{OE}}$  (Output Enable):**
  - $t_{\text{OEA}}$ : Output enable setup time before RAS.
  - $t_{\text{OED}}$ : Output enable delay after RAS.
  - $t_{\text{OEA}}$ : Output enable setup time before CAS.
  - $t_{\text{OED}}$ : Output enable delay after CAS.
- DQ (Data Out/In):**
  - $t_{\text{DQ}}$ : Data output delay after RAS.
  - $t_{\text{DQ}}$ : Data output delay after CAS.
  - $t_{\text{DQ}}$ : Data output delay after RAS.
  - $t_{\text{DQ}}$ : Data output delay after CAS.

**Legend:** The shaded area represents "Don't Care".

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The diagram illustrates the timing relationships for a 256K16 DRAM. It features three main signal lines:  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ , and Address. The Address signal is shown as a series of pulses, with the active period shaded and labeled 'ROW'. The  $\overline{\text{RAS}}$  signal is a periodic square wave. The  $\overline{\text{CAS}}$  signal is a periodic square wave that is delayed relative to  $\overline{\text{RAS}}$ . Various timing parameters are indicated by arrows:  $t_{\text{RAS}}$  (RAS pulse width),  $t_{\text{RCP}}$  (RAS to CAS setup time),  $t_{\text{CAS}}$  (CAS pulse width),  $t_{\text{CRP}}$  (CAS to RAS setup time),  $t_{\text{RAS}}^{\text{min}}$  (minimum RAS pulse width),  $t_{\text{RAS}}^{\text{max}}$  (maximum RAS pulse width),  $t_{\text{CAS}}^{\text{min}}$  (minimum CAS pulse width),  $t_{\text{CAS}}^{\text{max}}$  (maximum CAS pulse width),  $t_{\text{RAS}}^{\text{min}} + t_{\text{CAS}}^{\text{min}}$  (minimum combined RAS and CAS pulse width),  $t_{\text{RAS}}^{\text{max}} + t_{\text{CAS}}^{\text{max}}$  (maximum combined RAS and CAS pulse width),  $t_{\text{RAS}}^{\text{min}} + t_{\text{CAS}}^{\text{min}} + t_{\text{RAS}}^{\text{min}}$  (minimum combined RAS and CAS pulse width with RAS to RAS interval),  $t_{\text{RAS}}^{\text{max}} + t_{\text{CAS}}^{\text{max}} + t_{\text{RAS}}^{\text{max}}$  (maximum combined RAS and CAS pulse width with RAS to RAS interval),  $t_{\text{RAS}}^{\text{min}} + t_{\text{CAS}}^{\text{min}} + t_{\text{RAS}}^{\text{min}} + t_{\text{CAS}}^{\text{min}}$  (minimum combined RAS and CAS pulse width with RAS to RAS and CAS to RAS intervals),  $t_{\text{RAS}}^{\text{max}} + t_{\text{CAS}}^{\text{max}} + t_{\text{RAS}}^{\text{max}} + t_{\text{CAS}}^{\text{max}}$  (maximum combined RAS and CAS pulse width with RAS to RAS and CAS to RAS intervals),  $t_{\text{RAS}}^{\text{min}} + t_{\text{CAS}}^{\text{min}} + t_{\text{RAS}}^{\text{min}} + t_{\text{CAS}}^{\text{min}} + t_{\text{RAS}}^{\text{min}}$  (minimum combined RAS and CAS pulse width with RAS to RAS, CAS to RAS, and RAS to RAS intervals),  $t_{\text{RAS}}^{\text{max}} + t_{\text{CAS}}^{\text{max}} + t_{\text{RAS}}^{\text{max}} + t_{\text{CAS}}^{\text{max}} + t_{\text{RAS}}^{\text{max}}$  (maximum combined RAS and CAS pulse width with RAS to RAS, CAS to RAS, and RAS to RAS intervals),  $t_{\text{RAS}}^{\text{min}} + t_{\text{CAS}}^{\text{min}} + t_{\text{RAS}}^{\text{min}} + t_{\text{CAS}}^{\text{min}} + t_{\text{RAS}}^{\text{min}} + t_{\text{CAS}}^{\text{min}}$  (minimum combined RAS and CAS pulse width with RAS to RAS, CAS to RAS, and RAS to RAS intervals),  $t_{\text{RAS}}^{\text{max}} + t_{\text{CAS}}^{\text{max}} + t_{\text{RAS}}^{\text{max}} + t_{\text{CAS}}^{\text{max}} + t_{\text{RAS}}^{\text{max}} + t_{\text{CAS}}^{\text{max}}$  (maximum combined RAS and CAS pulse width with RAS to RAS, CAS to RAS, and RAS to RAS intervals).

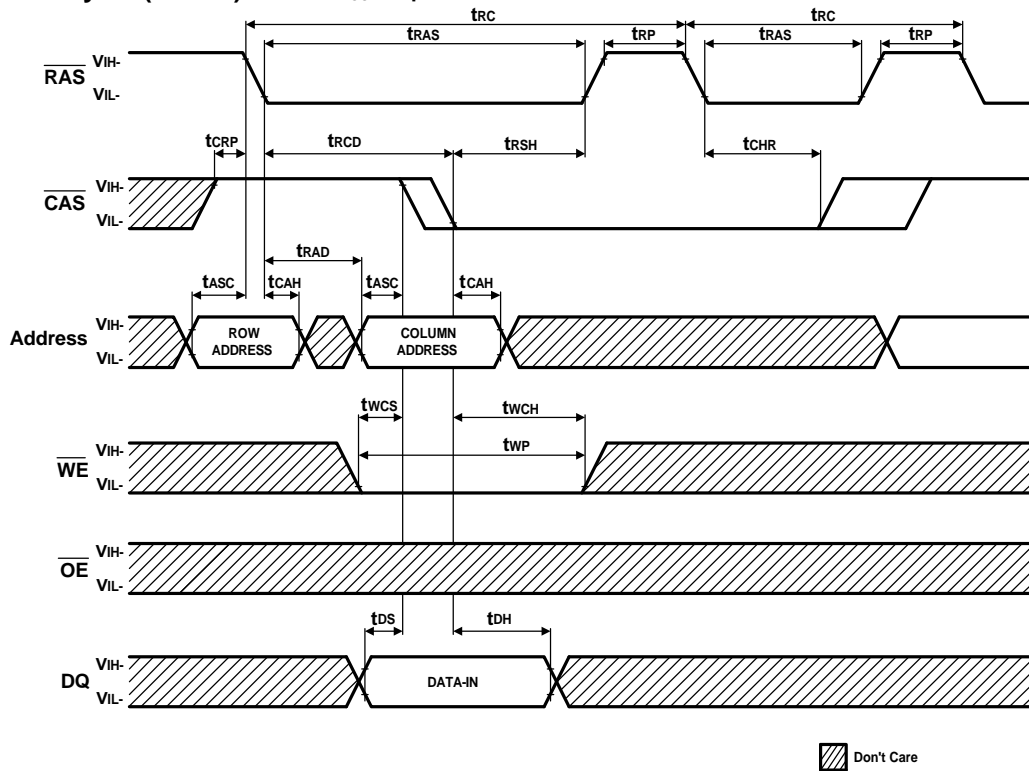
The diagram illustrates the timing relationships for the 16M1602 LCD module. It shows the following signals and their timing parameters:

- RAS**: Row Address Strobe. Timing parameters include  $t_{RC}$  (Row Address Strobe to Data Valid),  $t_{RP}$  (Row Address Strobe to Data Invalid),  $t_{RAS}$  (Row Address Strobe Pulse Width), and  $t_{RCD}$  (Row Address Strobe to Data Valid).
- CAS**: Column Address Strobe. Timing parameters include  $t_{CRP}$  (Column Address Strobe to Data Valid),  $t_{CD}$  (Column Address Strobe to Data Invalid),  $t_{RSH}$  (Row Address Strobe to Data Valid),  $t_{CHR}$  (Column Address Strobe to Data Invalid),  $t_{RAD}$  (Row Address Strobe to Data Valid), and  $t_{RAL}$  (Row Address Strobe to Data Invalid).
- Address**: Data Address. Timing parameters include  $t_{ASR}$  (Address Strobe to Data Valid),  $t_{CAH}$  (Address Strobe to Data Invalid),  $t_{ASC}$  (Address Strobe to Data Valid), and  $t_{CAH}$  (Address Strobe to Data Invalid).
- WE**: Write Enable. Timing parameters include  $t_{RCS}$  (Row Address Strobe to Data Valid),  $t_{AA}$  (Write Enable to Data Valid),  $t_{OEA}$  (Write Enable to Data Invalid),  $t_{WHR}$  (Write Enable to Data Invalid),  $t_{CAC}$  (Write Enable to Data Valid),  $t_{CLZ}$  (Write Enable to Data Invalid),  $t_{OEZ}$  (Write Enable to Data Invalid), and  $t_{OFF}$  (Write Enable to Data Invalid).
- OE**: Output Enable. Timing parameters include  $t_{OEZ}$  (Output Enable to Data Invalid) and  $t_{OFF}$  (Output Enable to Data Invalid).
- DQ**: Data Bus. Timing parameters include  $t_{OPEN}$  (Data Bus to Data Valid),  $t_{DATA-OUT}$  (Data Bus to Data Invalid),  $t_{TRAC}$  (Data Bus to Data Valid), and  $t_{CLZ}$  (Data Bus to Data Invalid).

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**Hidden Refresh Cycle ( Write ) NOTE : D<sub>OUT</sub> =Open**

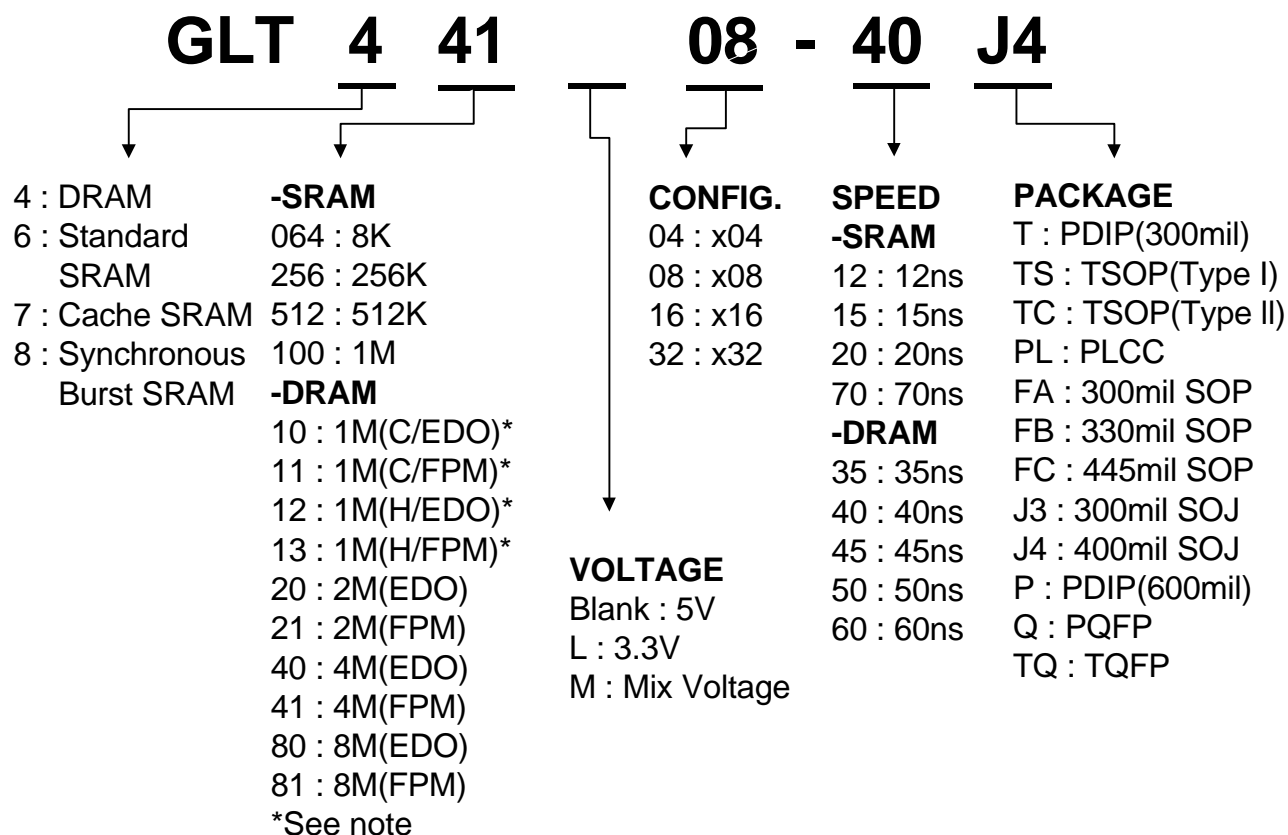


[illegible]

## Ordering Information

<b>Part Number</b>	<b>SPEED</b>	<b>POWER</b>	<b>FEATURE</b>	<b>PACKAGE</b>
GLT44108-40J4	40ns	Normal	FPM	SOJ 400mil 28L
GLT44108-50J4	50ns	Normal	FPM	SOJ 400mil 28L
GLT44108-60J4	60ns	Normal	FPM	SOJ 400mil 28L

## Parts Numbers (Top Mark) Definition :



Note : C→CDROM , H→HDD.

Example :

1. GLT710008-15T    1Mbit(128Kx8)15ns 5V SRAM PDIP(300mil)Package type.
2. GLT44016-40J4    4Mbit(256Kx16)40ns 5V DRAM SOJ(400mil)Package type.

**Package Information**

400mil 28 Lead Small Outline J-form Package (SOJ)

