

Features :

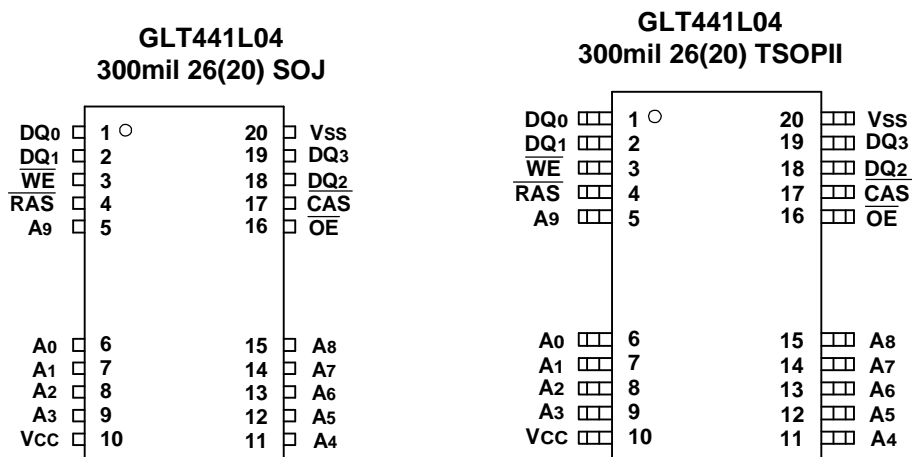
- * 1,048,576 words by 4 bits organization.
- * Fast access time and cycle time
- * Low power dissipation.
- * Read-Modify-Write, $\overline{\text{RAS}}$ -Only Refresh, $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh, Hidden Refresh.
- * 1,024 refresh cycles per 16ms.
- * Available in 300 mil 26(20) TSOPII, 300mil 26(20) SOJ.
- * $3.3\text{V} \pm 0.3\text{V}$ Vcc Power Supply voltage.
- * All inputs and Outputs are LVTTTL compatible.
- * FAST PAGE access cycle.
- * Self-refresh Capability.

Description :

The GLT441L04 is a high-performance CMOS dynamic random access memory containing 4,194,304 bits organized in a x4 configuration. The GLT4161L04 has 10 row and 10 column-addresses, and accepts 1024-cycle refresh in 16 ms.

The GLT441L04 provides FAST PAGE MODE operation which allows for fast data access within a row-address defined boundary, up to 1024 x 4 bits with cycle times as short as 35ns.

HIGH PERFORMANCE	50	60	70
Max. $\overline{\text{RAS}}$ Access Time, (t_{RAC})	50 ns	60 ns	70 ns
Max. Column Address Access Time, (t_{AA})	25 ns	30 ns	35 ns
Min. Extended Data Out Page Mode Cycle Time, (t_{PC})	35 ns	40 ns	45 ns
Min. Read/Write Cycle Time, (t_{RC})	90 ns	110 ns	130 ns
Max. $\overline{\text{CAS}}$ Access Time (t_{CAC})	13 ns	15 ns	20 ns

Pin Configuration :

Pin Descriptions:

Name	Function
A ₀ – A ₉	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
DQ ₀ - DQ ₃	Data Inputs / Outputs
V _{CC}	+3.3V Power Supply
V _{SS}	Ground
NC	No Connection

Absolute Maximum Ratings*

Operating Temperature, T_A (ambient)

.....0°C to +70°C

Storage Temperature(plastic).....-55°C to +150°C

Voltage Relative to V_{SS}-0.5V to + 4.6V

Short Circuit Output Current.....20mA

Power Dissipation.....1.0W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

$T_A=25^{\circ}\text{C}$, $V_{CC}=3.3\text{V}\pm 0.3\text{V}$, $V_{SS}=0\text{V}$

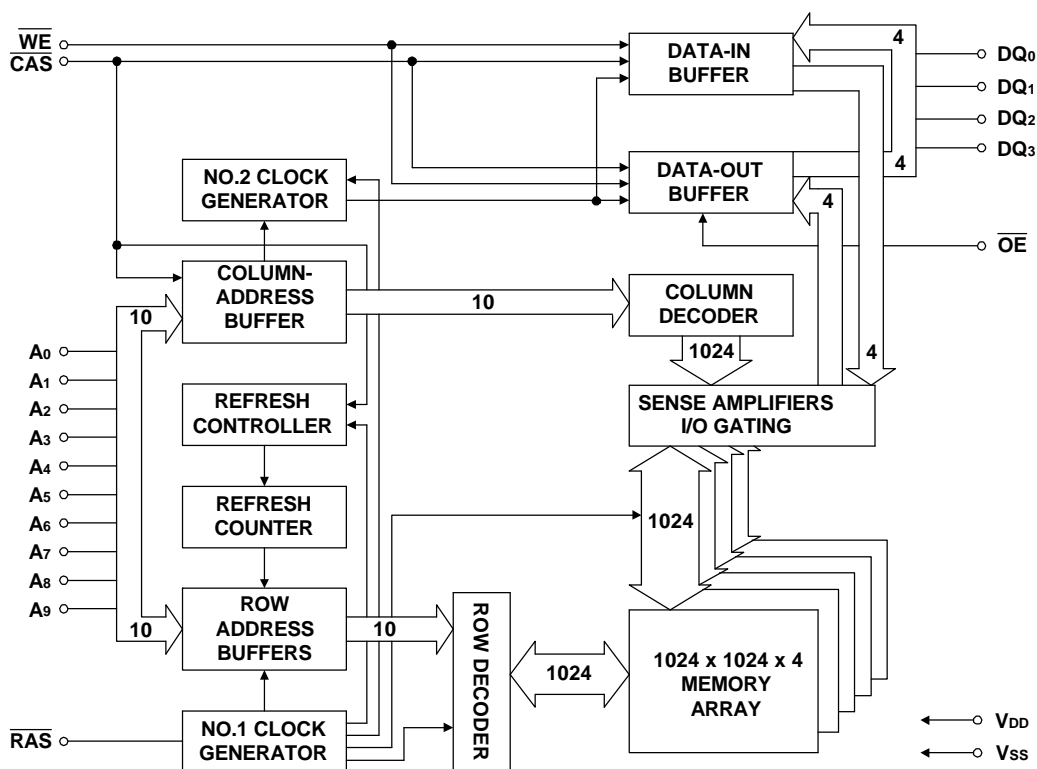
Symbol	Parameter	Max.	Unit
C_{IN1}	Address Input	5	pF
C_{IN2}	RAS, CAS, WE, OE	7	pF
C_{OUT}	Data Input/Output	7	pF

*Note: Capacitance is sampled and not 100% tested

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 200 μs and then, execute eight CAS-before-RAS or RAS-only refresh cycles as dummy cycles to initialize internal circuit.

Block Diagram :



Truth Table:

Function		RAS	CAS	WE	OE	ADDRESS		DATA-IN/OUT
						t _R	t _C	
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out,Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd cycle	L	H→L	H	L	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd cycle	L	H→L	L	X	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out,Data-In
	2nd cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out,Data-In
RAS -ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

DC and Operating Characteristics (1-2)

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC}=3.3\text{V}\pm 0.3\text{V}$, $V_{SS}=0\text{V}$, unless otherwise specified.

Sym.	Parameter	Test Conditions	Access Time	Min.	Typ	Max.	Unit	Notes
I_{LI}	Input Leakage Current (any input pin)	$0\text{V} \leq V_{IN} \leq V_{CC}+0.3\text{V}$ (All other pins not under test= 0V)		-5		+5	μA	
I_{LO}	Output Leakage Current (for High-Z State)	$0\text{V} \leq V_{out} \leq V_{CC}$ Output is disabled (Hiz)		-5		+5	μA	
I_{CC1}	Operating Current, Random READ/WRITE	$t_{RC} = t_{RC}(\text{min.})$	$t_{RAC} = 50\text{ns}$ $t_{RAC} = 60\text{ns}$ $t_{RAC} = 70\text{ns}$			90 80 70	mA	1,2
I_{CC2}	Standby Current	$\overline{\text{RAS}}, \overline{\text{CAS}}$ at V_{IH} other inputs $\geq V_{SS}$				1	mA	
I_{CC3}	Refresh Current, RAS -Only	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ at V_{IH} $t_{RC} = t_{RC}(\text{min.})$	$t_{RAC} = 50\text{ns}$ $t_{RAC} = 60\text{ns}$ $t_{RAC} = 70\text{ns}$			90 80 70	mA	2
I_{CC4}	Operating Current, FAST Page Mode	$\overline{\text{RAS}}$ at V_{IL} , $\overline{\text{CAS}}$ address cycling: $t_{PC}=t_{PC}(\text{min.})$	$t_{RAC} = 50\text{ns}$ $t_{RAC} = 60\text{ns}$ $t_{RAC} = 70\text{ns}$			90 70 60	mA	1,2
I_{CC5}	Refresh Current, CAS Before RAS	$\overline{\text{RAS}}, \overline{\text{CAS}}$ address cycling: $t_{RC}=t_{RC}(\text{min.})$	$t_{RAC} = 50\text{ns}$ $t_{RAC} = 60\text{ns}$ $t_{RAC} = 70\text{ns}$			90 80 70	mA	2
I_{CC6}	Standby Current, (CMOS)	$\overline{\text{RAS}} \geq V_{CC}-0.2\text{V}$, $\overline{\text{CAS}} \geq V_{CC}-0.2\text{V}$, All other inputs V_{SS}				300	μA	
I_{CC7}	Self refresh Current	$\overline{\text{RAS}} = \overline{\text{CAS}} = 0.2\text{V}$, $\overline{\text{WE}} = \overline{\text{OE}} = A_0 \sim A_{10} = V_{CC}-0.2\text{V}$ or 0.2V $\overline{\text{DQ}}_0 \sim \overline{\text{DQ}}_3 = V_{CC}-0.2\text{V}, 0.2\text{V}$ or Open				300	μA	
V_{IL}	Input Low Voltage			-0.3		+0.8	V	3
V_{IH}	Input High Voltage			2.0		$V_{CC}+0.3$	V	4
V_{OL}	Output Low Voltage	$I_{OL} = 2\text{mA}$				0.4	V	
V_{OH}	Output High Voltage	$I_{OH} = -2\text{mA}$		2.4			V	

Notes:

- I_{CC} is dependent on output loading when the device output is selected. Specified $I_{CC}(\text{max.})$ is measured with the output open.
- I_{CC} is dependent upon the number of address transitions specified $I_{CC}(\text{max.})$ is measured with a maximum of one transition per address cycle in random Read/Write and EDO Fast Page Mode.
- Specified $V_{IL}(\text{min.})$ is steady state operation. During transitions $V_{IL}(\text{min.})$ may undershoot to -0.9V for a period not to exceed 10ns. All AC parameters are measured with $V_{IL}(\text{min.}) \geq V_{SS}$ and $V_{IH}(\text{max.}) \leq V_{CC}$.
- Specified $V_{IH}(\text{max.})$ is steady state operation. During transitions $V_{IH}(\text{max.})$ may overshoot to $V_{CC}+0.9\text{V}$ for a period not to exceed 10ns. All AC parameters are measured with $V_{IL}(\text{min.}) \geq V_{SS}$ and $V_{IH}(\text{max.}) \leq V_{CC}$.

AC Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 3.3\text{ V} \pm 0.3\text{V}$, $V_{IH}/V_{IL} = 3.0/0\text{V}$, $V_{OH}/V_{OL} = 2/0.8\text{V}$

An initial pause of 200 μs and 8 CAS-before-RAS or RAS-only refresh cycles are required after power-up.

Parameter	Symbol	50		60		70		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read or Write Cycle Time	t_{RC}	90		110		130		ns	
Read Modify Write Cycle Time	t_{RWC}	133		155		185		ns	
RAS Precharge Time	t_{RP}	30		40		50		ns	
RAS Pulse Width	t_{RAS}	50	10k	60	10k	70	10k	ns	
Access Time from RAS	t_{RAC}		50		60		70	ns	1,2,3
Access Time from CAS	t_{CAC}		13		15		20	ns	1,3,7
Access Time from Column Address	t_{AA}		25		30		35	ns	1,5,6
CAS to Output Low-Z	t_{CLZ}	0		0		0		ns	3
RAS Hold Time	t_{RSH}	13		15		20		ns	
CAS Hold Time	t_{CSH}	50		60		70		ns	
CAS Pulse Width	t_{CAS}	13	10k	15	10k	20	10k	ns	
RAS to CAS Delay Time	t_{RCD}	20	37	20	45	20	50	ns	
RAS to Column Address Delay Time	t_{RAD}	15	25	15	30	15	35	ns	7
CAS to RAS Precharge Time	t_{CRP}	5		5		5		ns	
Row Address Set-Up Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		10		ns	
Column Address Set-Up Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	10		10		15		ns	
Column Address to RAS Lead Time	t_{RAL}	25		30		35		ns	
Read Command Set-Up Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to CAS	t_{RCH}	0		0		0		ns	4
Read Command Hold Time Referenced to RAS	t_{RRH}	0		0		0		ns	4
Write Command Set-Up Time	t_{WCS}	0		0		0		ns	8, 9
Write Command Hold Time	t_{WCH}	10		10		15		ns	
Write Command Pulse Width	t_{WP}	10		10		15		ns	
Write Command to RAS Lead Time	t_{RWL}	15		15		20		ns	
Write Command to CAS Lead Time	t_{CWL}	13		15		20		ns	
Data Set-Up Time	t_{DS}	0		0		0		ns	10
Data Hold Time	t_{DH}	10		10		15		ns	10

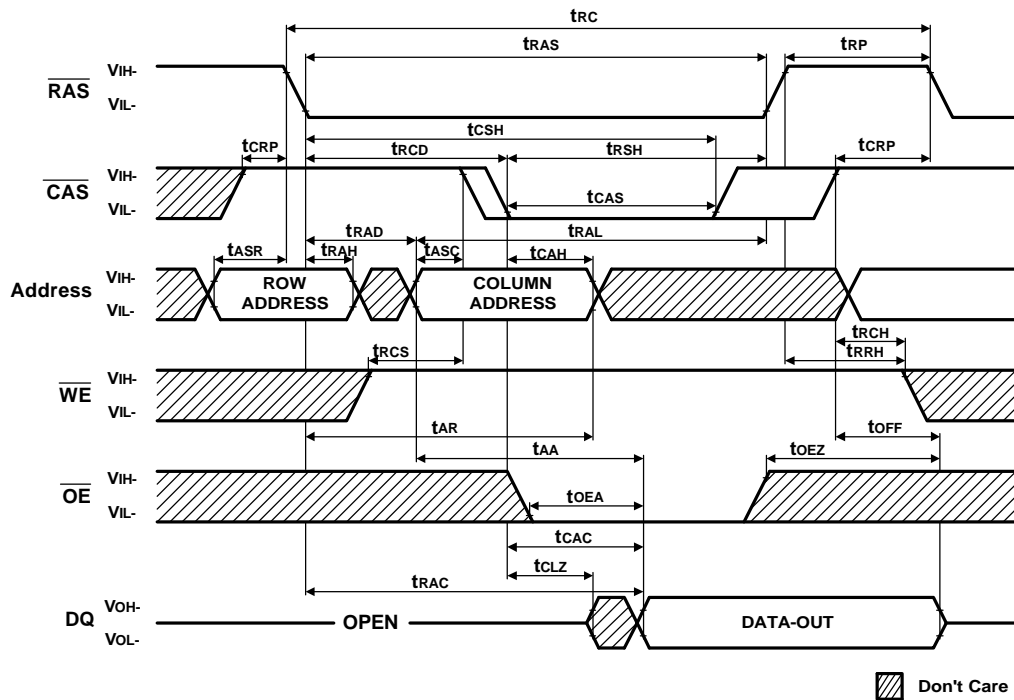
AC Characteristics

Parameter	Symbol	50		60		70		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
RAS to $\overline{\text{WE}}$ Delay Time	t_{RWD}	73		85		100		ns	
CAS to $\overline{\text{WE}}$ Delay Time	t_{CWD}	36		40		50		ns	
Column Address to $\overline{\text{WE}}$ Delay Time	t_{AWD}	48		55		65		ns	
CAS Precharge to $\overline{\text{WE}}$ Delay	t_{CPWD}	53		60		70		ns	
RAS to CAS Precharge Time	t_{RPC}	5		5		5		ns	
CAS precharge time (CAS Before RAS counter test cycle)	t_{CPT}	20		20		30		ns	
Access Time from CAS Precharge	t_{CPA}		30		35		40	ns	
Page Mode Cycle Time	t_{PC}	35		40		45		ns	
Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	76		85		100		ns	
CAS Precharge Time (Page Mode)	t_{CP}	10		10		10		ns	
RAS Pulse Width (Page Mode Only)	t_{RASP}	50	100k	60	200k	70	200k	ns	
RAS Hold Time From $\overline{\text{CAS}}$ Precharge	t_{RHCP}	30		35		40		ns	
Access Time from $\overline{\text{OE}}$	t_{OEA}		13		15		20	ns	
$\overline{\text{OE}}$ to Data Delay Time	t_{OED}	13		15		20		ns	
$\overline{\text{OE}}$ to Output High-Z	t_{OEZ}	0	13	0	15	0	20	ns	
$\overline{\text{OE}}$ Command Hold Time	t_{OEH}	13		15		20		ns	
CAS Set-Up Time for $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Cycle	t_{CSR}	5		5		5		ns	
CAS Hold Time for $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Cycle	t_{CHR}	10		10		15		ns	
$\overline{\text{WE}}$ to RAS Precharge Time (CAS Before RAS Refresh)	t_{WRP}	10		10		10		ns	
$\overline{\text{WE}}$ to RAS Hold Time (CAS Before RAS Refresh)	t_{WRH}	10		10		10		ns	
Transition Time	t_{T}	3	50	3	50	3	50	ns	11
Refresh Period (1,024 cycles)	t_{REF}		16		16		16	ms	
Refresh Period (S-Version)	t_{REF}		128		128		128	ms	
RAS Pulse Width (CAS Before RAS Self Refresh)	t_{RASS}	100		100		100		μs	
RAS precharge Time (CAS Before RAS Self Refresh)	t_{RPS}	90		110		130		ns	
CAS Hold Time (CAS Before RAS Self Refresh)	t_{CHS}	50		50		50		ns	

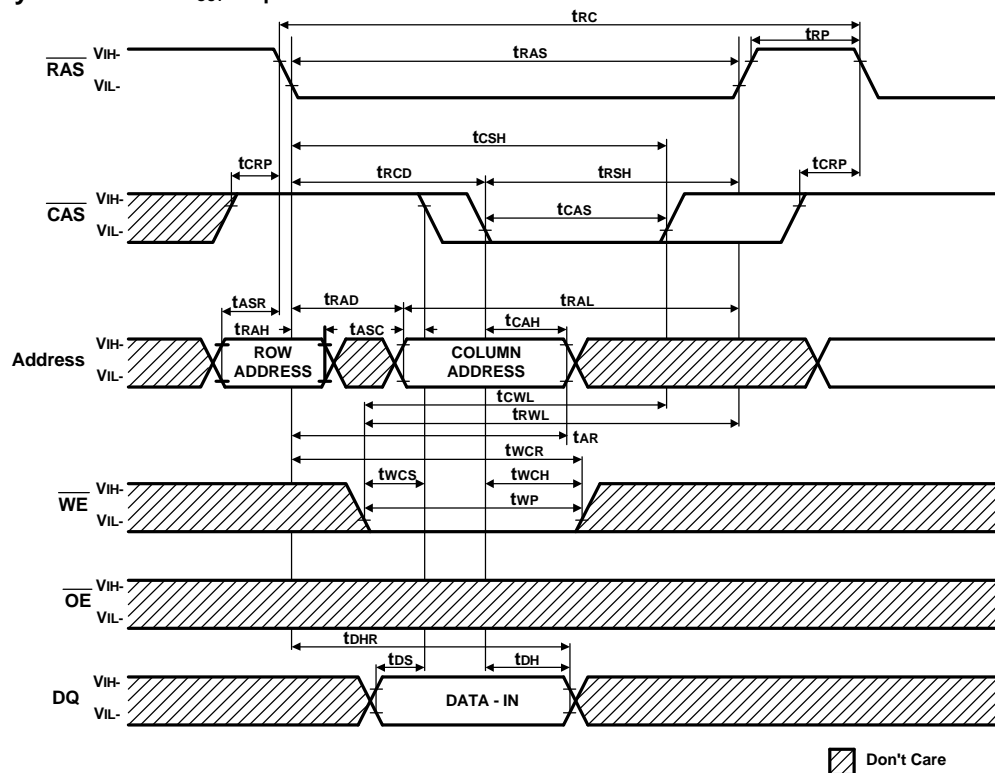
Notes:

1. Measure with a load equivalent to one TTL input and 100 pF.
2. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max.})$. If t_{RCD} is greater than $t_{\text{RCD}}(\text{max.})$, access time will be t_{AA} dominant.
3. Assumes that $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max.})$. If t_{RAD} is greater than $t_{\text{RAD}}(\text{max.})$, access time will be controlled by t_{CAC} .
4. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle.
5. Access time is determined by the longest of t_{AA} , t_{CAC} and t_{CPA} .
6. Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max.})$.
7. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max.})$.
8. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters.
9. $t_{\text{WCS}}(\text{min.})$ must be satisfied in an Early Write Cycle.
10. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{\text{CAS}}$ or $\overline{\text{WE}}$.
11. t_{T} is measured between $V_{\text{IH}}(\text{min.})$ and $V_{\text{IL}}(\text{max.})$. AC-measurements assume $t_{\text{T}} = 3 \text{ ns}$.

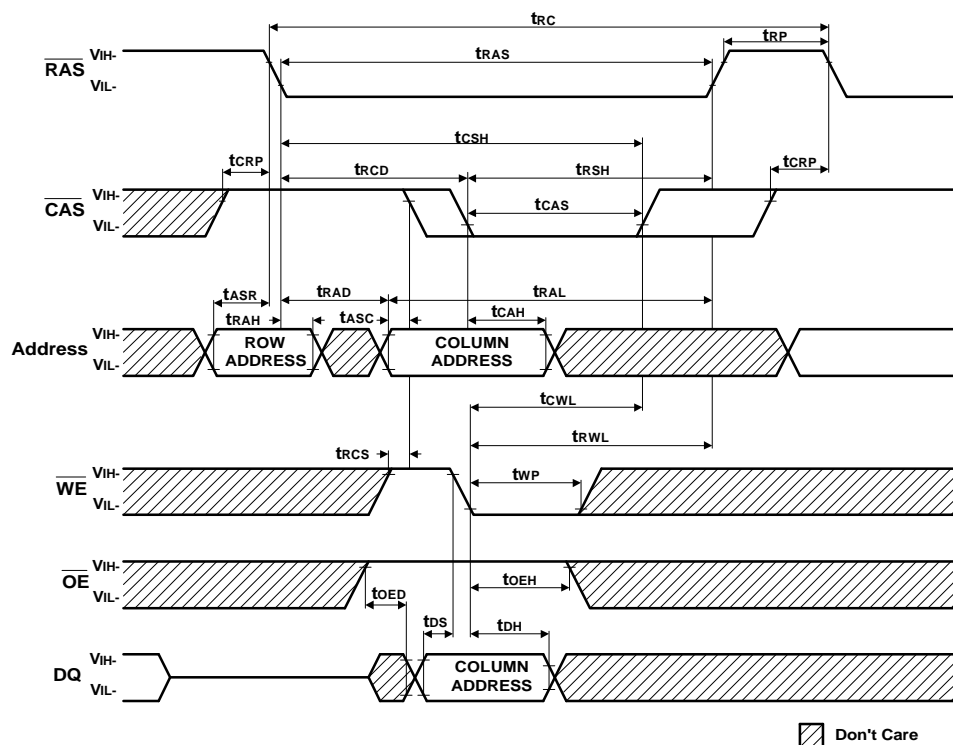
Read Cycle



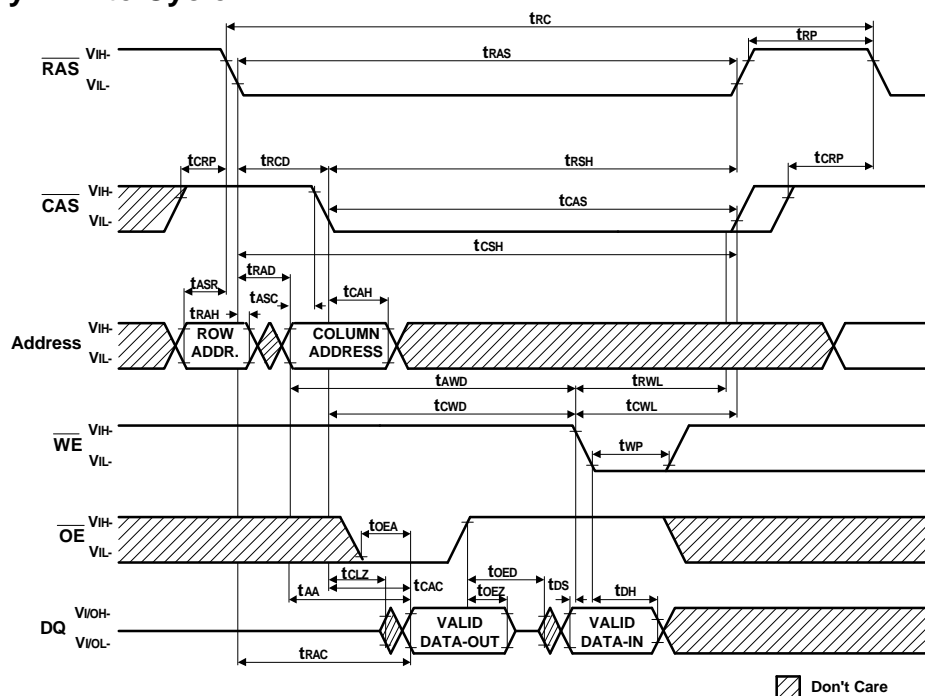
Early Write Cycle NOTE : D_{OUT} = Open



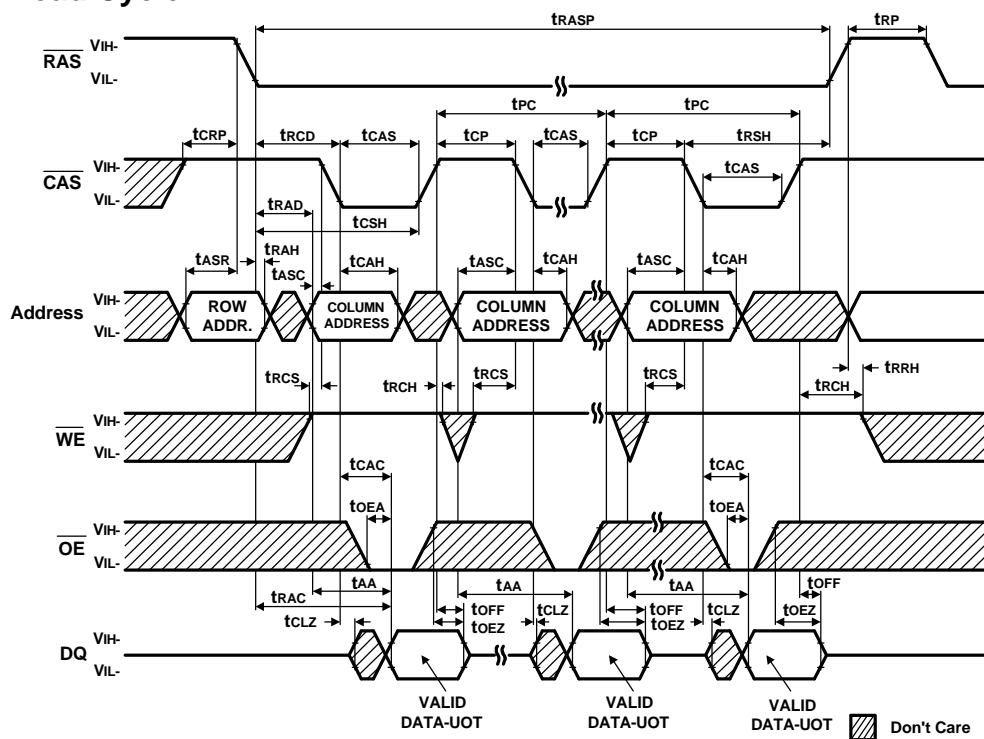
Late Write Cycle ($\overline{\text{OE}}$ Controlled Write) NOTE : $\text{D}_{\text{OUT}} = \text{Open}$



Read - Modify - Write Cycle

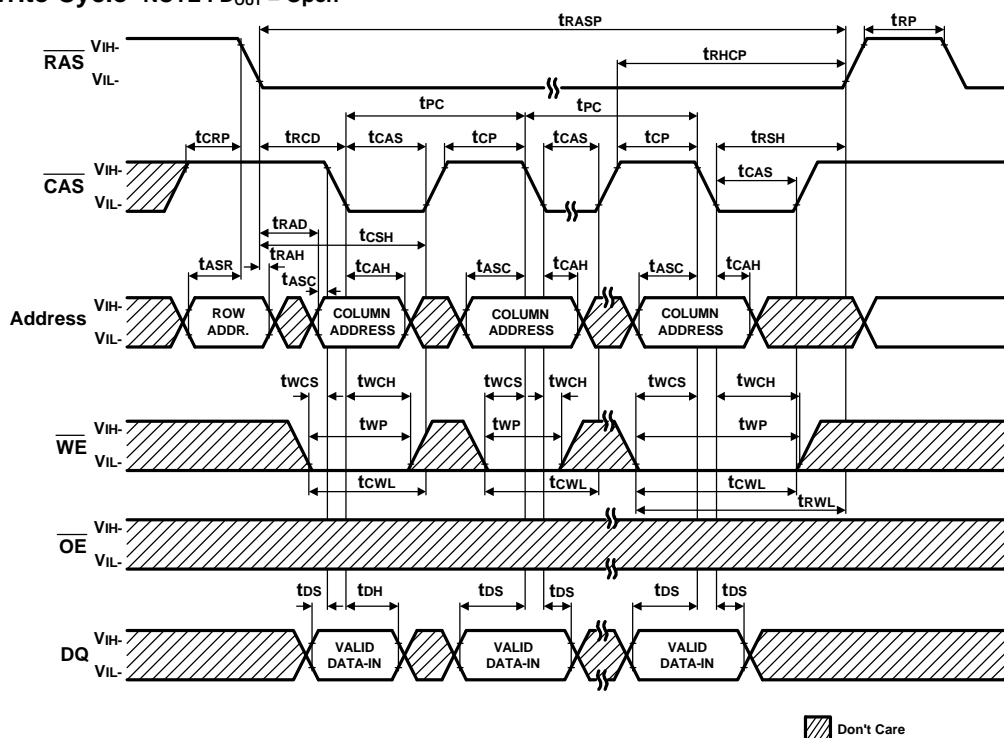


Fast Page Read Cycle

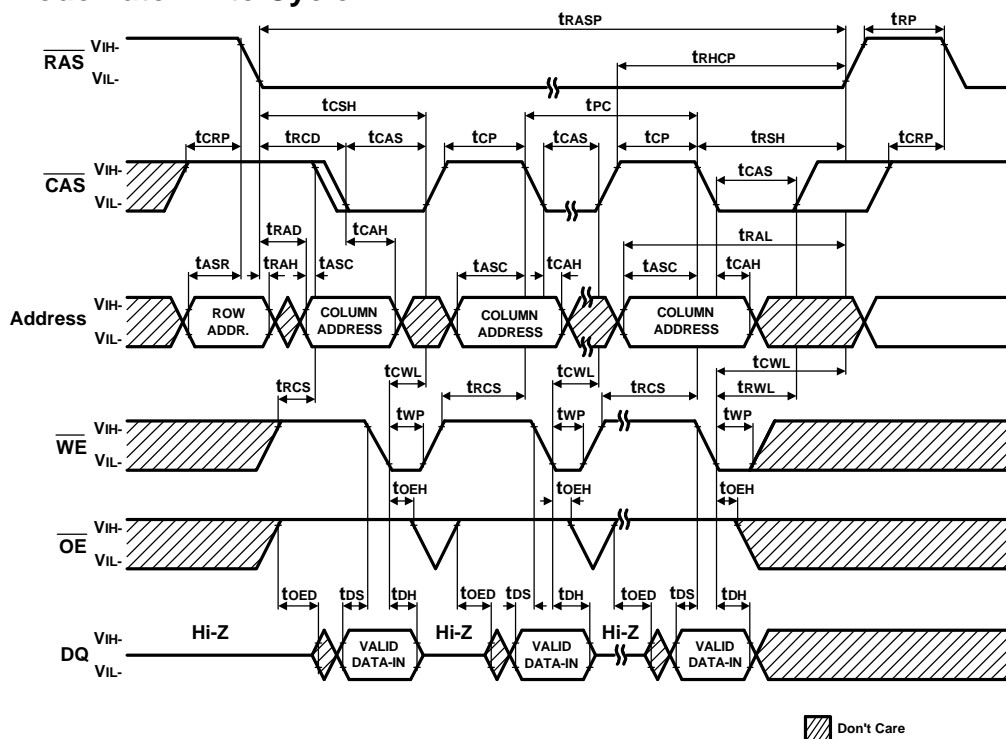


Fast Page Write Cycle NOTE : D_{OUT} = Open

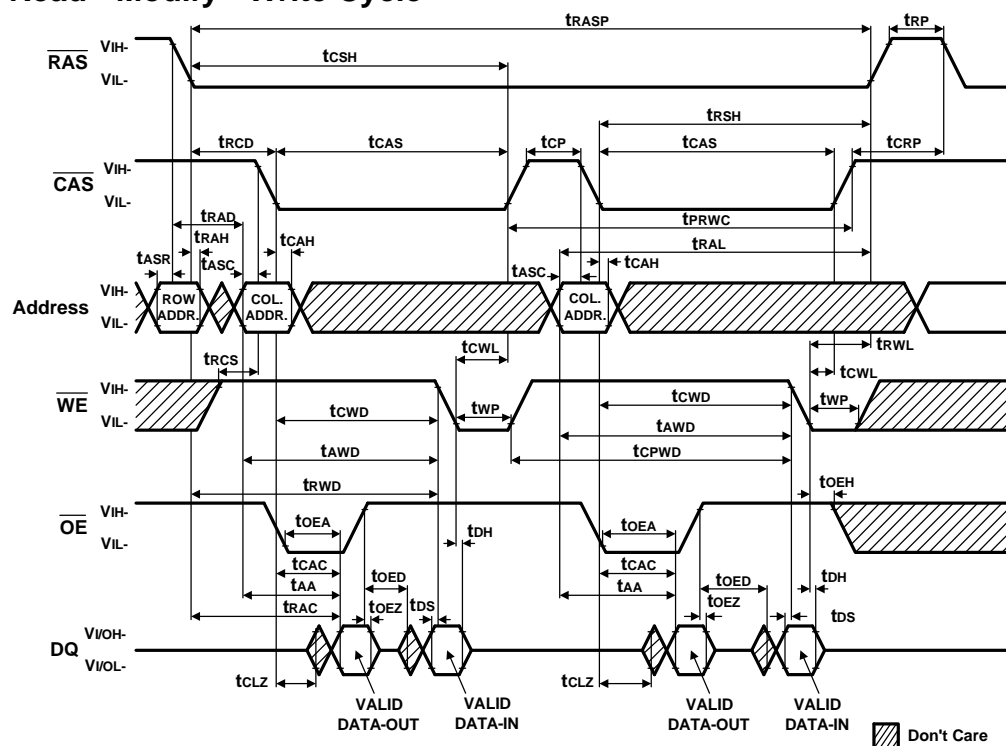
NOTE : $D_{OUT} = \text{Open}$



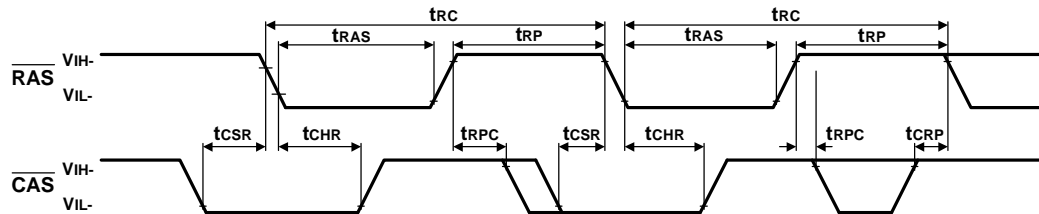
Fast Page Mode Late Write Cycle



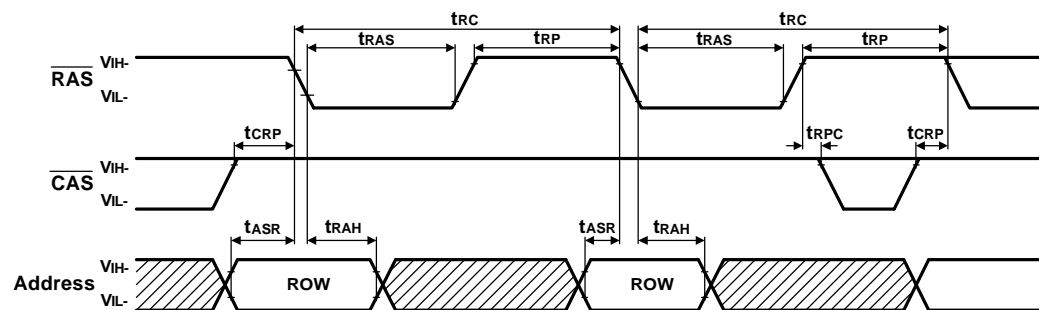
Fast Page Read - Modify - Write Cycle

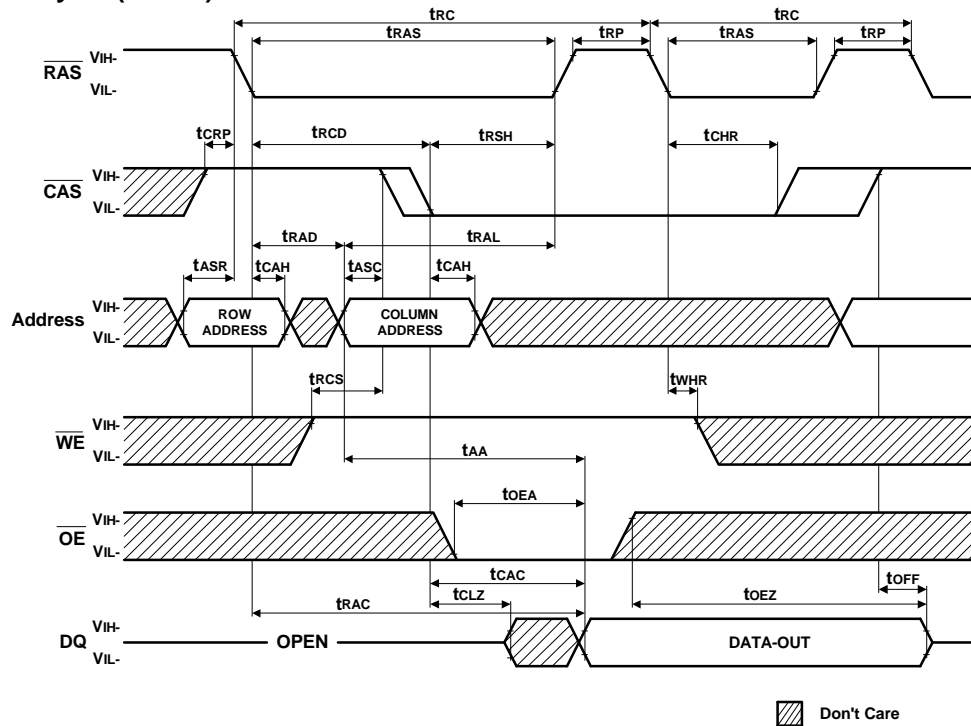
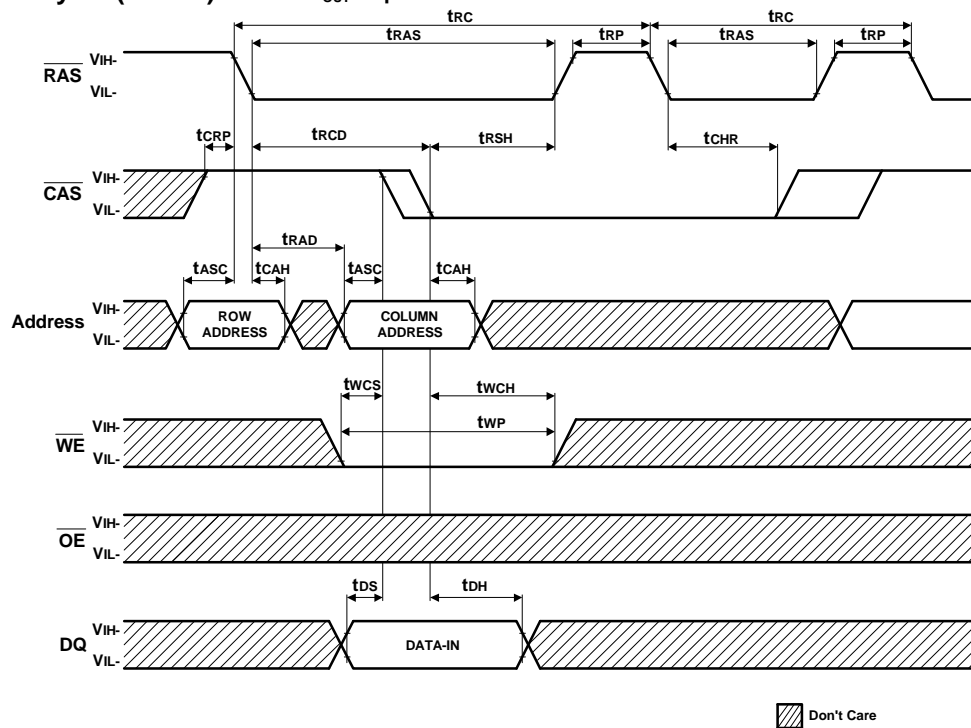


CAS Before RAS Refresh Cycle

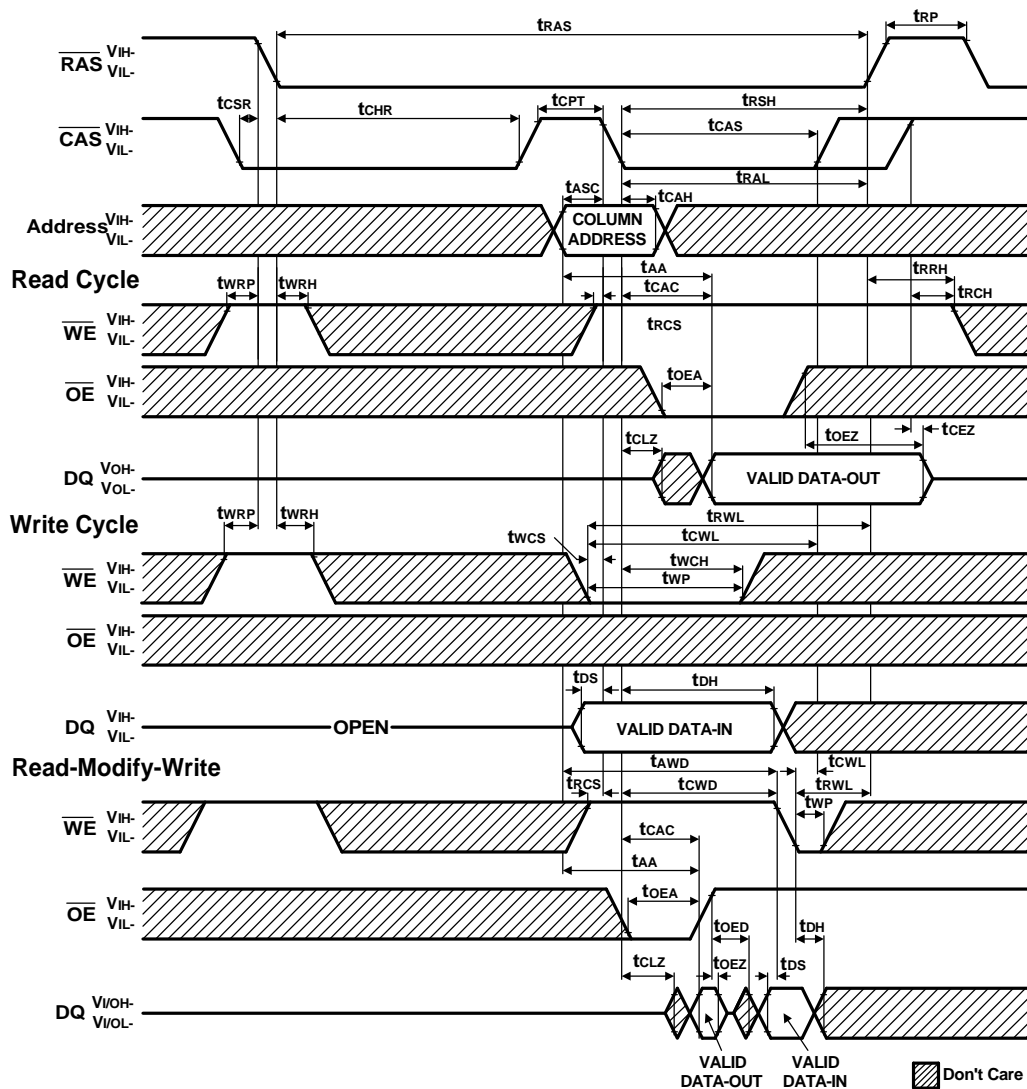


RAS -Only Refresh Cycle

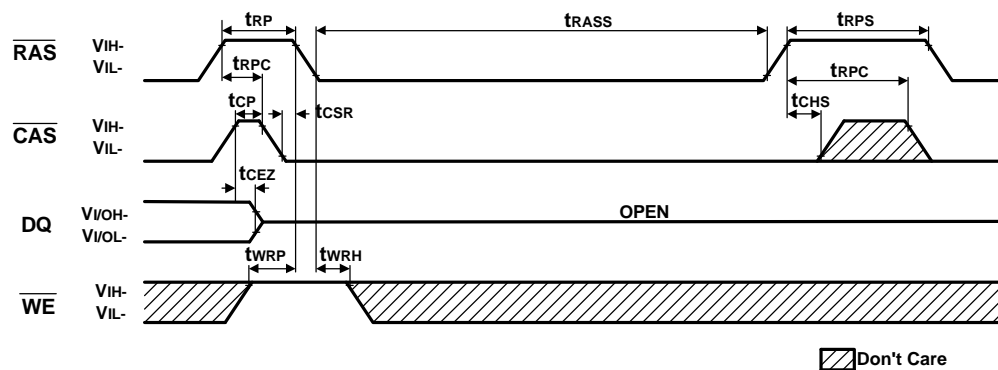


Hidden Refresh Cycle (Read)

Hidden Refresh Cycle (Write) NOTE : D_{OUT} = Open


CAS - Before **RAS** Refresh Counter Test Cycle



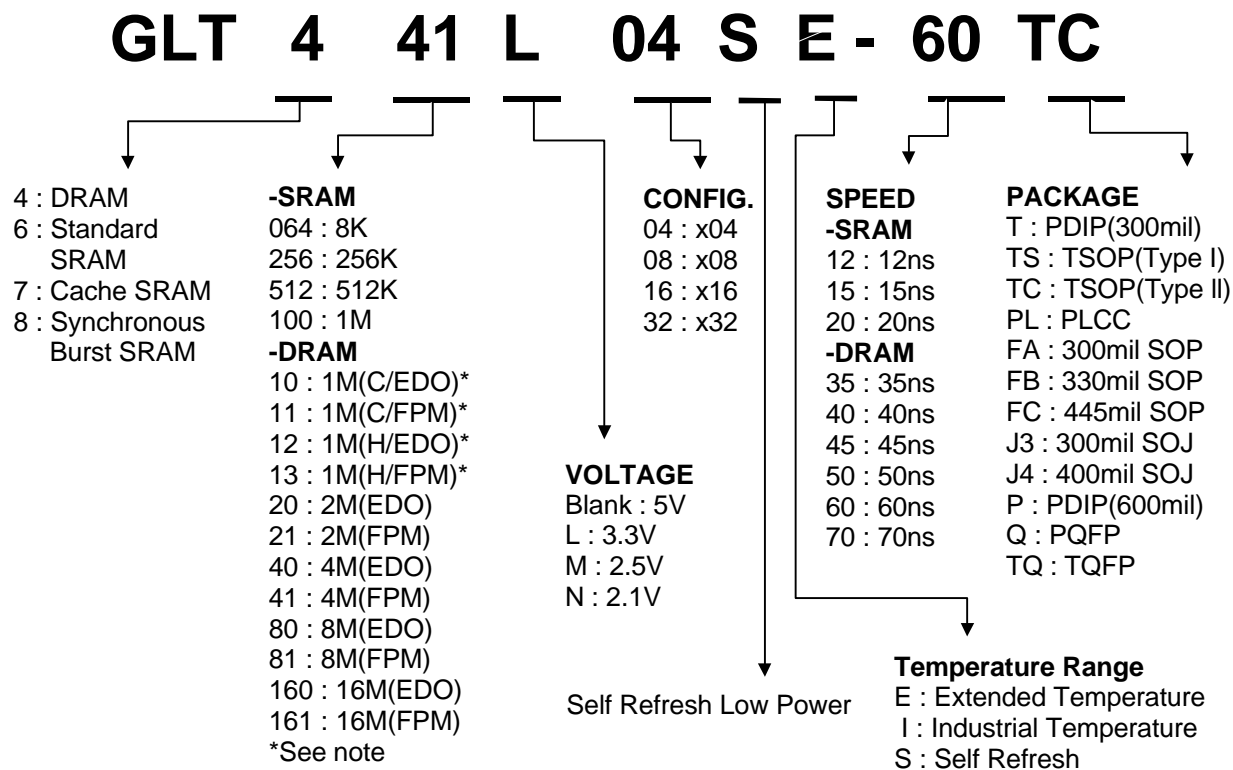
CAS-Before-RAS Self Refresh Cycle



NOTE : $\overline{\text{OE}}$, Address = Don't Care

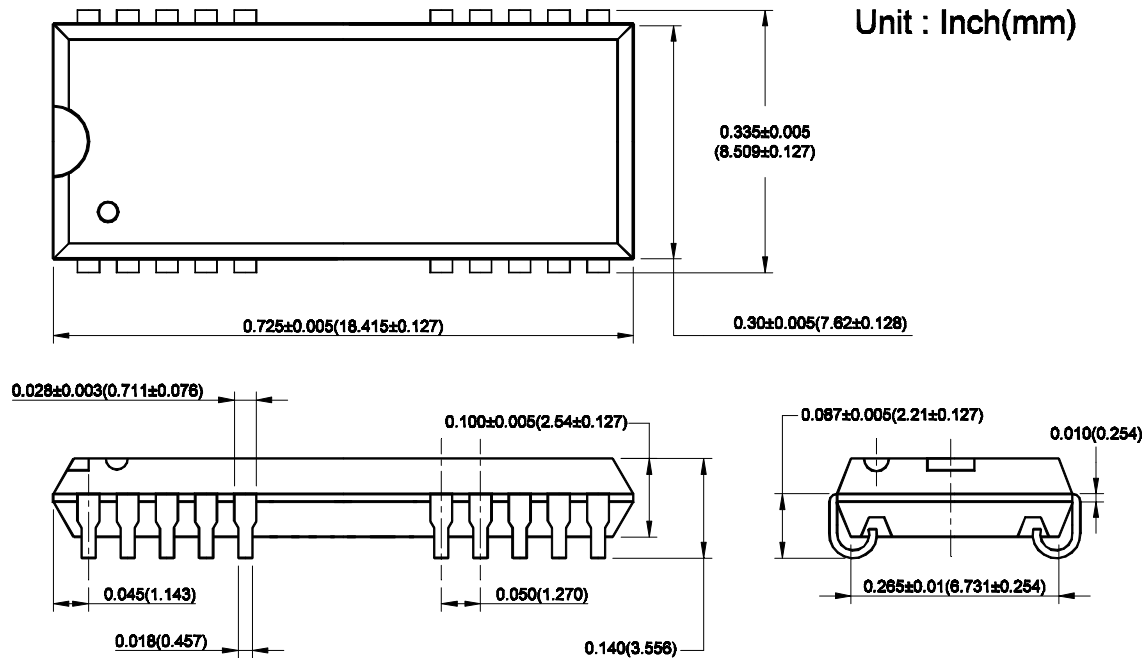
Ordering Information

Part Number	SPEED	POWER	FEATURE	TEMPERATURE	PACKAGE
GLT441L04-50J3	50ns	Normal	FPM	Commercial	SOJ 300mil 26(20)L
GLT441L04-60J3	60ns	Normal	FPM	Commercial	SOJ 300mil 26(20)L
GLT441L04-70J3	70ns	Normal	FPM	Commercial	SOJ 300mil 26(20)L
GLT441L04-50TC	50ns	Normal	FPM	Commercial	TSOPII 300mil 26(20)L
GLT441L04-60TC	60ns	Normal	FPM	Commercial	TSOPII 300mil 26(20)L
GLT441L04-70TC	70ns	Normal	FPM	Commercial	TSOPII 300mil 26(20)L
GLT441L04E-50J3	50ns	Normal	FPM	Extended	SOJ 300mil 26(20)L
GLT441L04E-60J3	60ns	Normal	FPM	Extended	SOJ 300mil 26(20)L
GLT441L04E-70J3	70ns	Normal	FPM	Extended	SOJ 300mil 26(20)L
GLT441L04E-50TC	50ns	Normal	FPM	Extended	TSOPII 300mil 26(20)L
GLT441L04E-60TC	60ns	Normal	FPM	Extended	TSOPII 300mil 26(20)L
GLT441L04E-70TC	70ns	Normal	FPM	Extended	TSOPII 300mil 26(20)L
GLT441L04S-50J3	50ns	Self Refresh	FPM	Commercial	SOJ 300mil 26(20)L
GLT441L04S-60J3	60ns	Self Refresh	FPM	Commercial	SOJ 300mil 26(20)L
GLT441L04S-70J3	70ns	Self Refresh	FPM	Commercial	SOJ 300mil 26(20)L
GLT441L04S-50TC	50ns	Self Refresh	FPM	Commercial	TSOPII 300mil 26(20)L
GLT441L04S-60TC	60ns	Self Refresh	FPM	Commercial	TSOPII 300mil 26(20)L
GLT441L04S-70TC	70ns	Self Refresh	FPM	Commercial	TSOPII 300mil 26(20)L
GLT441L04SE-50J3	50ns	Self Refresh	FPM	Extended	SOJ 300mil 26(20)L
GLT441L04SE-60J3	60ns	Self Refresh	FPM	Extended	SOJ 300mil 26(20)L
GLT441L04SE-70J3	70ns	Self Refresh	FPM	Extended	SOJ 300mil 26(20)L
GLT441L04SE-50TC	50ns	Self Refresh	FPM	Extended	TSOPII 300mil 26(20)L
GLT441L04SE-60TC	60ns	Self Refresh	FPM	Extended	TSOPII 300mil 26(20)L
GLT441L04SE-70TC	70ns	Self Refresh	FPM	Extended	TSOPII 300mil 26(20)L

Parts Numbers (Top Mark) Definition :


Package Information

300mil 20/26 Lead Thin Small Outline Package SOJ



300mil 20/26 Lead Thin Small Outline Package (TSOP) TYPE II

Unit : Inch

