

Features :

- * Low-power consumption.
 - active: 30mA I_{cc} at 55ns.
 - stand by :
 - 10 μ A (CMOS input / output , LL)
 - 2 μ A (CMOS input / output, SL)
- * Single +2.7V to 3.6V power supply.
- * Equal access and cycle time.
- * 55\70\85 ns access time.
- * Tri-state output.
- * Automatic power-down when deselected.
- * Multiple center power and ground pins for improved noise immunity.
- * Individual byte controls for both read and write cycles.
- * Industrial grade (-40°C ~ 85°C) available.
- * Available in 48-fpBGA/44L TSOPII.

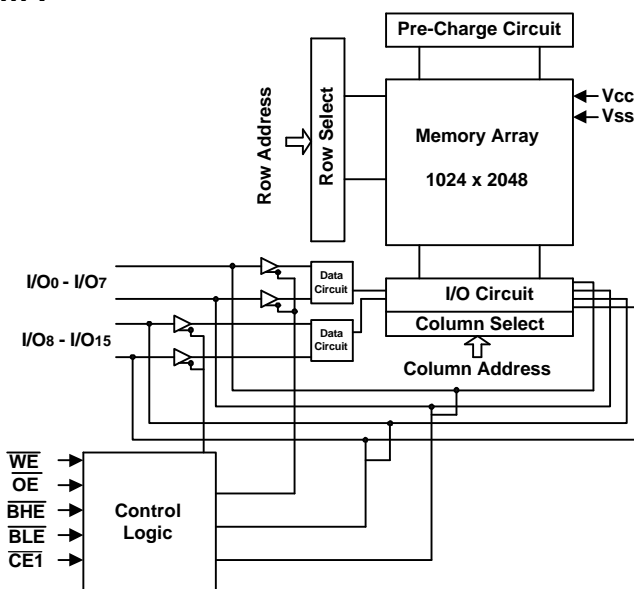
Description :

The GLT6200L16 is a low power CMOS Static RAM organized as 131,072 words by 16 bits. Easy memory expansion is provided by an active LOW $\overline{\text{CE1}}$ and $\overline{\text{OE}}$ pin.

This device has an automatic power – down mode feature when deselected. Separate Byte Enable controls ($\overline{\text{BLE}}$ and $\overline{\text{BHE}}$) allow individual bytes to be accessed. $\overline{\text{BLE}}$ controls the lower bits I/O0 – I/O7. $\overline{\text{BHE}}$ controls the upper bits I/O8 – I/O15.

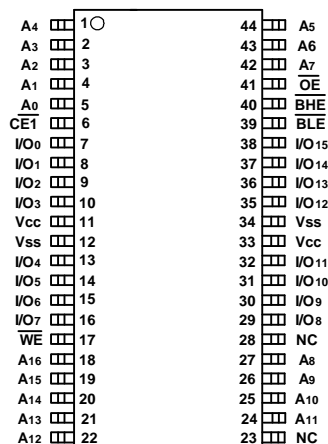
Writing to these devices is performed by taking Chip Enable $\overline{\text{CE1}}$ with Write Enable $\overline{\text{WE}}$ and byte Enable ($\overline{\text{BLE}}$ / $\overline{\text{BHE}}$) Low

Reading from the device is performed by taking Chip Enable $\overline{\text{CE1}}$ with Output enable $\overline{\text{OE}}$ and byte Enable ($\overline{\text{BLE}}$ / $\overline{\text{BHE}}$) Low while Write Enable $\overline{\text{WE}}$ are held HIGH.

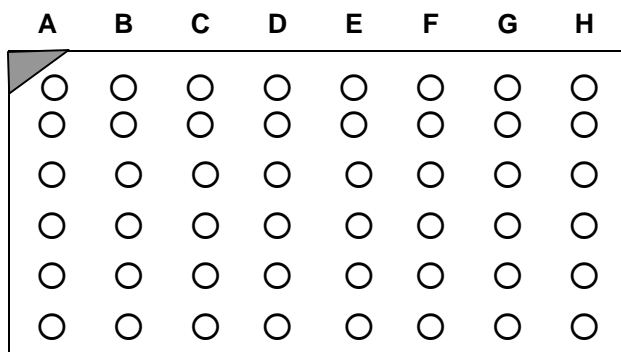
Function Block Diagram :


Pin Configurations :

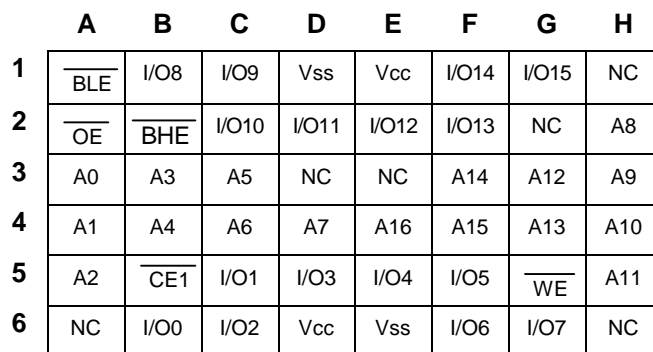
GLT6200L16



48 Ball fpBGA :



Bottom View



Bottom View

Note : NC means no Ball.

Pin Descriptions:

| Name | Function |
|--------------------------------------|--|
| A ₀ – A ₁₆ | Address Inputs |
| CE ₁ | Chip Enable Input |
| OE | Output Enable Input |
| WE | Write Enable Input |
| I/O ₀ – I/O ₁₅ | Data Input and Data Output |
| V _{CC} | 2.7V~3.6V Power Supply |
| BLE | Lower Byte Enable Input (I/O ₀ to I/O ₇) |
| BHE | Higher Byte Enable Input (I/O ₈ to I/O ₁₅) |
| GND | Ground |
| NC | No Connection |

Truth Table:

| $\overline{CE1}$ | \overline{OE} | \overline{WE} | \overline{BLE} | \overline{BHE} | I/O0-I/O7 | I/O8-I/O15 | Power | Mode |
|------------------|-----------------|-----------------|------------------|------------------|-----------|------------|---------|------------------|
| H | X | X | X | X | High-Z | High-Z | Standby | Deselected |
| X | X | X | H | H | High-Z | High-Z | Standby | Deselected |
| L | H | H | L | X | High-Z | High-Z | Active | Output Disabled |
| L | H | H | X | L | High-Z | High-Z | Active | Output Disabled |
| L | L | H | L | H | Data Out | High-Z | Active | Lower Byte Read |
| L | L | H | H | L | High-Z | Data Out | Active | Upper Byte Read |
| L | L | H | L | L | Data Out | Data Out | Active | Word Read |
| L | X | L | L | H | Data In | High-Z | Active | Lower Byte Write |
| L | X | L | H | L | High-Z | Data In | Active | Upper Byte Write |
| L | X | L | L | L | Data In | Data In | Active | Word Write |

Note ; X means don care. (Must be low or high state).

Absolute Maximum Ratings*

| Parameter | Symbol | Minimum | Maximum | Unit |
|------------------------------------|----------------|---------|-----------|------|
| Voltage on Any Pin Relative to Gnd | Vt | -0.5 | Vcc + 0.3 | V |
| Power Dissipation | P _T | - | 1.0 | W |
| Storage Temperature (Plastic) | Tstg | -55 | +150 | °C |
| Temperature Under Bias | Tbias | -25 | +85 | °C |

*Note : Stresses greater than those listed above Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions (TA = -25°C to 85°C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|----------------|-----------------|-------|-----|----------------------|------|
| Supply Voltage | V _{CC} | 2.7 | 3 | 3.6 | V |
| | Gnd | 0.0 | 0.0 | 0.0 | V |
| Input Voltage | V _{IH} | 2.2 | - | V _{CC} +0.2 | V |
| | V _{IL} | -0.5* | - | 0.6 | V |

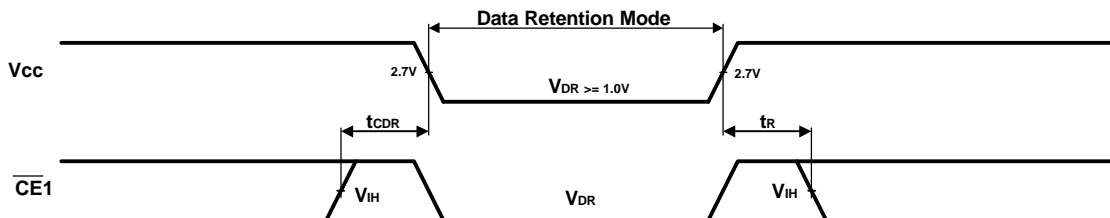
* V_{IL} min = -2.0V for pulse width less than t_{RC}/2.

DC Operating Characteristics ($V_{CC}=2.7$ to $3.6V$, $T_A = -25^{\circ}C$ to $85^{\circ}C$)

| Parameter | Sym. | Test Conditions | 55 | | 70 | | 85 | | Unit |
|---|------------|--|--------------|-----|-----|-----|-----|-----|---------|
| | | | Min | Max | Min | Max | Min | Max | |
| Input Leakage Current | $ I_{LI} $ | $V_{CC} = \text{Max}, V_{in} = \text{Gnd to } V_{CC}$ | | 1 | | 1 | | 1 | μA |
| Output Leakage Current | $ I_{LO} $ | $\overline{CE1} = V_{IH} \text{ or } V_{CC} = \text{Max}, V_{OUT} = \text{Gnd to } V_{CC}$ | | 1 | | 1 | | 1 | μA |
| Operating Power Supply Current | I_{CC} | $\overline{CE1} = V_{IL}, V_{IN}=V_{IH} \text{ or } V_{IL}, I_{OUT}=0$ | | 5 | | 5 | | 5 | mA |
| Average Operating Current | I_{CC1} | $I_{OUT} = 0mA, \text{Min Cycle, 100\% Duty}$ | | 30 | | 30 | | 25 | mA |
| | I_{CC2} | $\overline{CE1} \leq 0.2V, I_{OUT} = 0mA, \text{Cycle Time}=1\mu s, 100\% = \text{Duty}$ | | 3 | | 3 | | 3 | mA |
| Standby Power Supply Current(TTL Level) | I_{SB} | $\overline{CE1} = V_{IH}$ | | 0.5 | | 0.5 | | 0.5 | mA |
| Standby Power Supply Current (CMOS Level) | I_{SB1} | $\overline{CE1} \geq V_{CC}-0.2V, V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC}-0.2V$ | GLT6200L16LL | | | 10 | | 10 | μA |
| | | | GLT6200L16SL | | | 2 | | 2 | μA |
| Output Low Voltage | V_{OL} | $I_{OL} = 2.1 \text{ mA}$ | | 0.4 | | 0.4 | | 0.4 | V |
| Output High Voltage | V_{OH} | $I_{OH} = -1 \text{ mA}$ | 2.4 | | 2.4 | | 2.4 | | V |

Data Retention

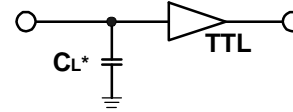
| Parameter | Sym. | Test Conditions | Min. | Max. | Unit |
|--|------------|--|----------|------|---------|
| V_{CC} for Data retention | V_{DR} | $\overline{CE1} \geq V_{CC} - 0.2V$ | 1.0 | - | V |
| Data Retention Current | I_{CCDR} | $V_{IN} \geq V_{CC} - 0.2V \text{ or } V_{IN} \leq 0.2V$ | - | 2 | μA |
| Chip Deselect to Data Retention Time | t_{CDR} | | 0 | - | ns |
| Operating Recovery Time ⁽²⁾ | t_R | | t_{RC} | - | ns |

Data Retention Waveform ($T_A = -25^{\circ}C$ to $+85^{\circ}C$)


AC Test Conditions

| | |
|---|--------------|
| Input Pulse Levels | 0.4V to 2.4V |
| Input Rise and Fall Time | 5 ns |
| Input and Output Timing Reference Level | 1.4V |

AC Test Loads and Waveforms



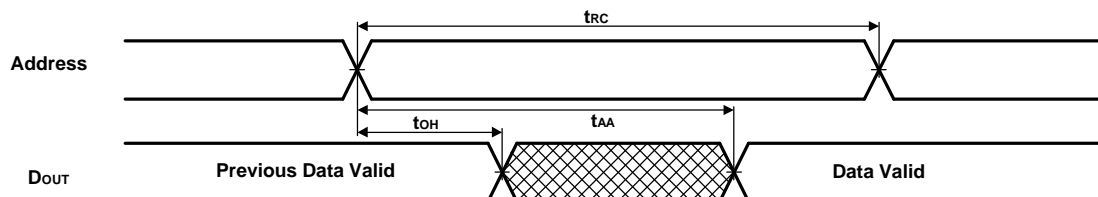
Output Load Condition
 $C_L = 30\text{pf} + 1\text{TTL Load}$

*Including Scope and Jig Capacitance

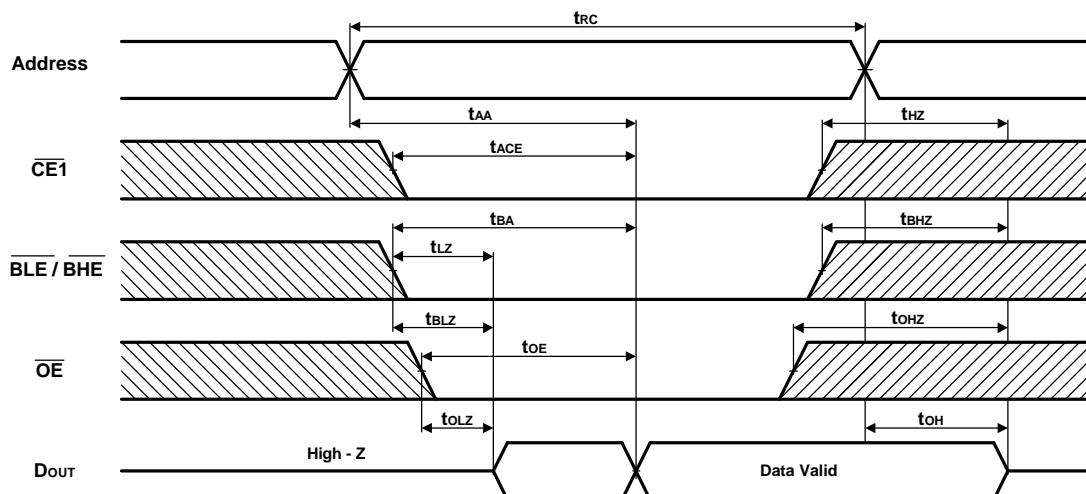
Read Cycle ⁽⁹⁾ ($V_{CC}=2.7\text{V}$ to 3.6V , $T_A = -25^\circ\text{C}$ to 85°C)

| Parameter | Symbol | 55 | | 70 | | 85 | | Unit | Note |
|---|-----------|-----|-----|-----|-----|-----|-----|------|-------|
| | | Min | Max | Min | Max | Min | Max | | |
| Read Cycle Time | t_{RC} | 55 | | 70 | | 85 | | ns | |
| Address Access Time | t_{AA} | | 55 | | 70 | | 85 | ns | |
| Chip Enable Access Time | t_{ACE} | | 55 | | 70 | | 85 | ns | |
| Output Enable Access Time | t_{OE} | | 35 | | 40 | | 40 | ns | |
| Output Hold from address Change | t_{OH} | 10 | | 10 | | 10 | | ns | |
| Chip Enable to Output in Low-Z | t_{LZ} | 10 | | 10 | | 10 | | ns | 4,5 |
| Chip Disable to Output in High-Z | t_{HZ} | | 25 | | 30 | | 35 | ns | 3,4,5 |
| Output Enable to Output in Low-Z | t_{OLZ} | 5 | | 5 | | 5 | | ns | |
| Output Disable to Output in High-Z | t_{OHZ} | | 25 | | 25 | | 30 | ns | |
| \overline{BLE} , \overline{BHE} Enable to Output in Low-Z | t_{BLZ} | 5 | | 5 | | 5 | | ns | 4,5 |
| \overline{BLE} , \overline{BHE} Disable to Output in High-Z | t_{BHZ} | | 25 | | 25 | | 30 | ns | 3,4,5 |
| \overline{BLE} , \overline{BHE} Access Time | t_{BA} | | 35 | | 40 | | 85 | ns | |

Timing Waveform of Read Cycle 1 (Address Controlled)



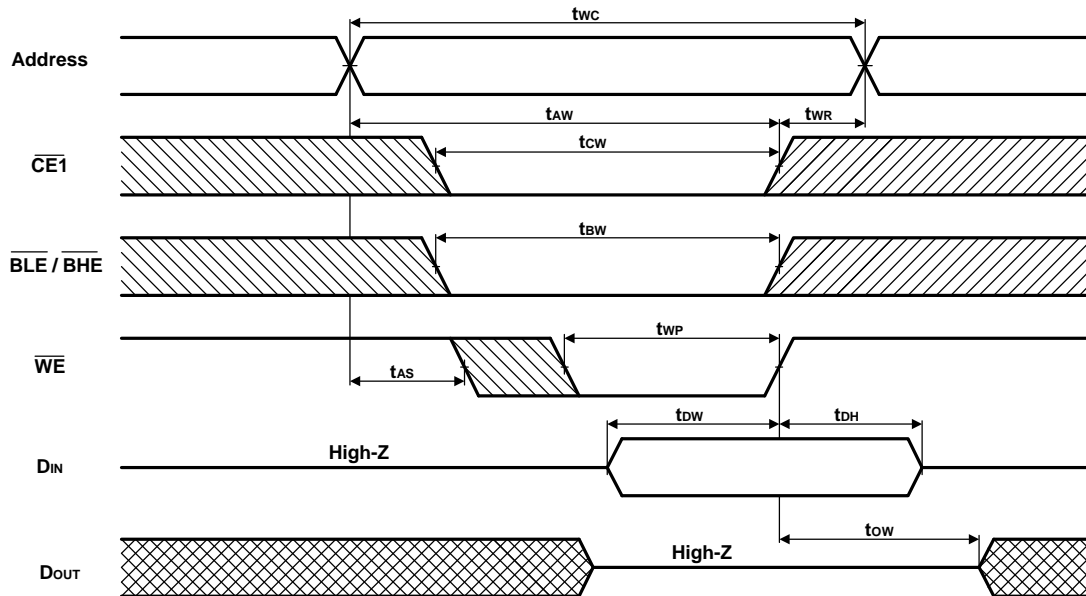
Timing Waveform of Read Cycle 2 ^(3~5)



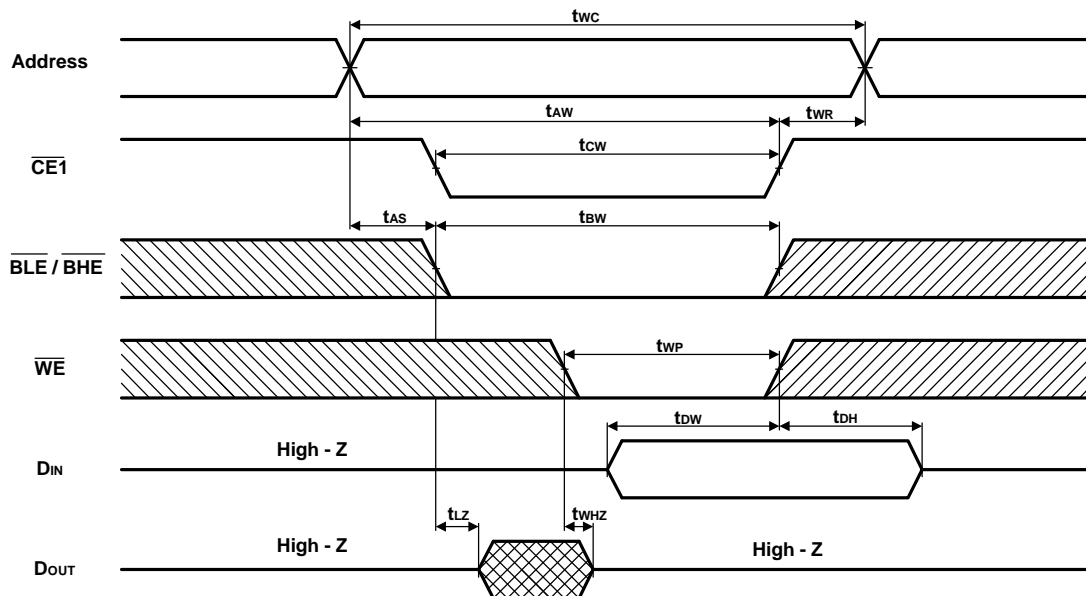
Write Cycle ⁽¹¹⁾ ($V_{CC}=2.7$ to $3.6V$, $T_A = -25^{\circ}C$ to $85^{\circ}C$)

| Parameter | Symbol | 55 | | 70 | | 85 | | Unit | Note |
|--|-----------|-----|-----|-----|-----|-----|-----|------|------|
| | | Min | Max | Min | Max | Min | Max | | |
| Write Cycle Time | t_{WC} | 55 | | 70 | | 85 | | ns | |
| Chip Enable to Write End | t_{CW} | 50 | | 60 | | 70 | | ns | |
| Address Setup to Write End | t_{AW} | 50 | | 60 | | 70 | | ns | |
| Address Setup Time | t_{AS} | 0 | | 0 | | 0 | | ns | |
| Write Pulse Width | t_{WP} | 45 | | 50 | | 60 | | ns | |
| Write Recovery Time | t_{WR} | 0 | | 0 | | 0 | | ns | |
| Data Valid to Write End | t_{DW} | 25 | | 30 | | 35 | | ns | |
| Data Hold Time | t_{DH} | 0 | | 0 | | 0 | | ns | |
| Write Enable to Output in High-Z | t_{WHZ} | | 25 | | 30 | | 35 | ns | |
| Output Active from Write End | t_{OW} | 5 | | 5 | | 5 | | ns | |
| \overline{BLE} , \overline{BHE} Setup to Write End | t_{BW} | 50 | | 60 | | 70 | | ns | |

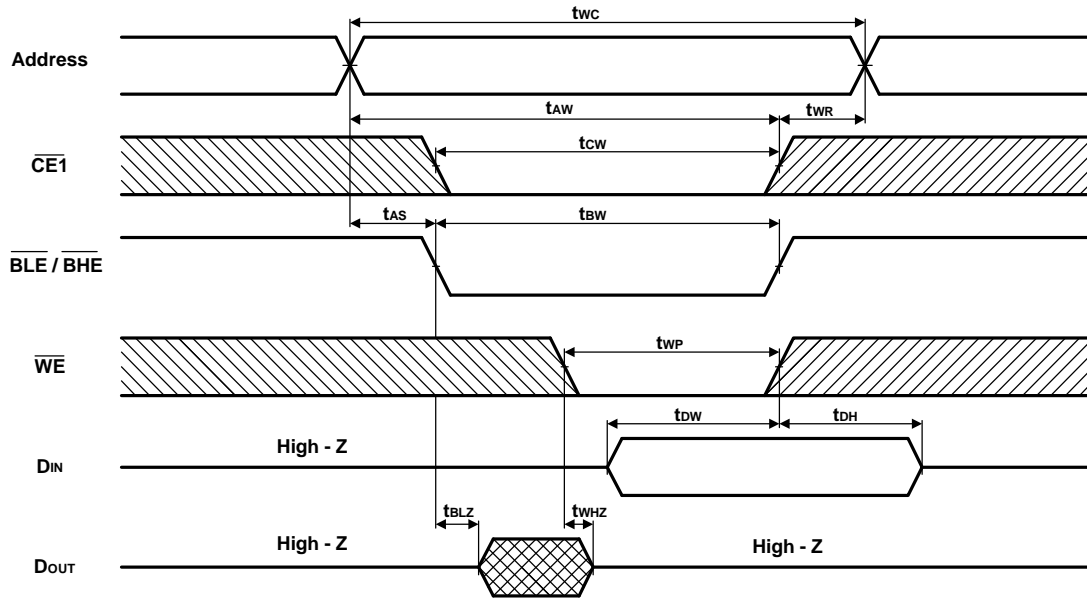
Timing Waveform of Write Cycle 1 (Address Controlled)^(2-6,8)



Timing Waveform of Write Cycle 2 ($\overline{CE1}$ Controlled)^(2-6,8)



Timing Waveform of Write Cycle 4 ($\overline{\text{BLE}}$ / $\overline{\text{BHE}}$ Controlled)^(2-6,8)

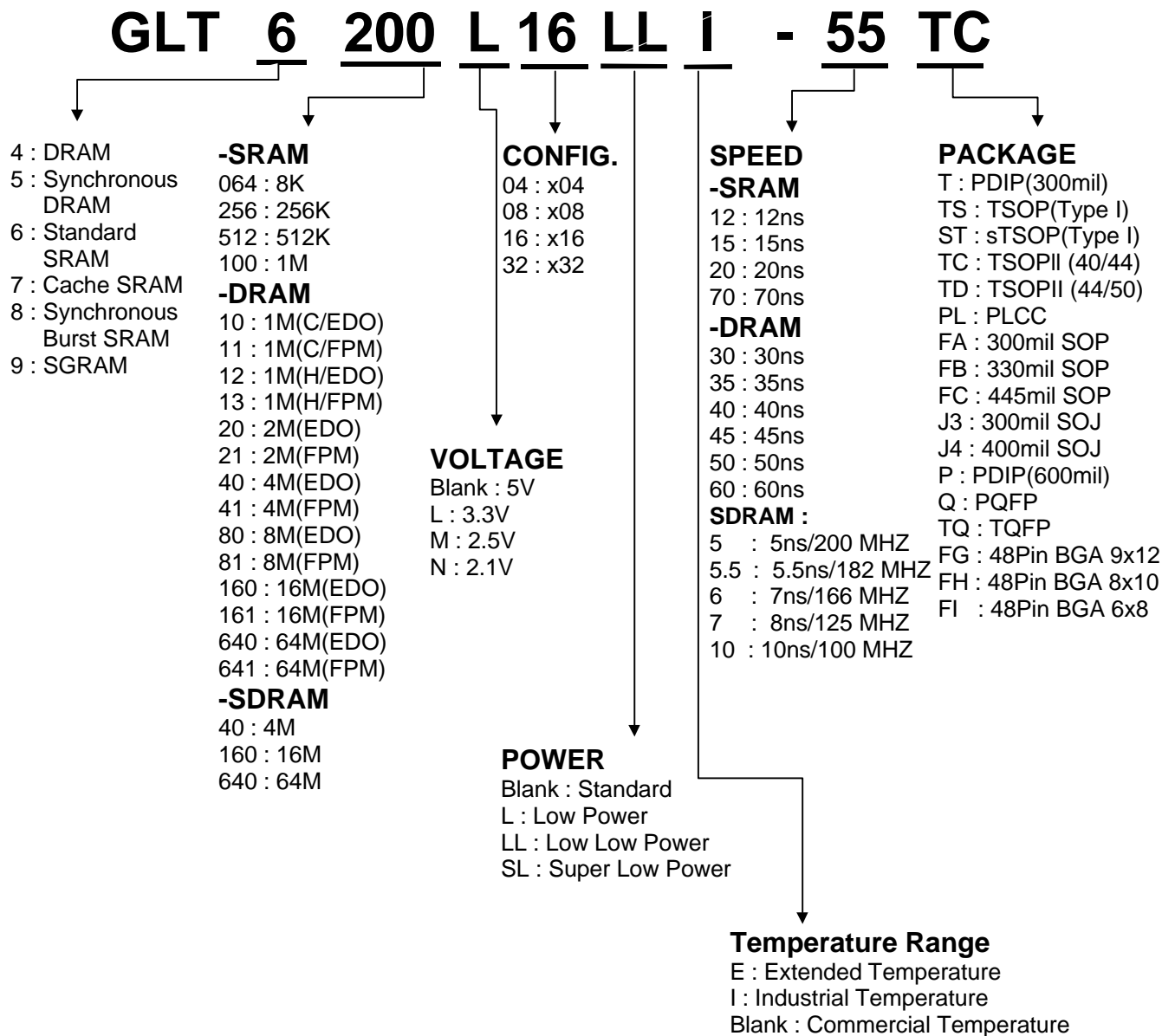


Notes :

1. L-version includes this feature.
2. This Parameter is samples and not 100% tested.
3. For test conditions, see AC Test Condition.
4. This parameter is tested with CL = 5pF. Transition is measured $\pm 500\text{mV}$ from steady – state voltage.
5. This parameter is guaranteed, but is not tested.
6. $\overline{\text{WE}}$ is HIGH for read cycle.
7. $\overline{\text{CE1}}$ and $\overline{\text{OE}}$ are LOW for read cycle.
8. Address valid prior to or coincident with $\overline{\text{CE1}}$ transition LOW.
9. All read cycle timings are referenced from the last valid address to the first transition address.
10. $\overline{\text{CE1}}$ or $\overline{\text{WE}}$ must be HIGH during address transition.
11. All write cycle timings are referenced from the last valid address to the first transition address.

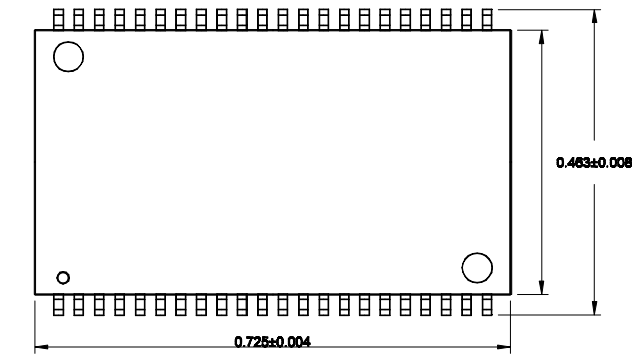
Ordering Information

| Part Number | SPEED | POWER | PACKAGE |
|--------------------|--------------|--------------|----------------|
| GLT6200L16LL-55TC | 55ns | Normal | TSOPII 44L |
| GLT6200L16LL-70TC | 70ns | Normal | TSOPII 44L |
| GLT6200L16LL-85TC | 85ns | Normal | TSOPII 44L |
| GLT6200L16LLI-55TC | 55ns | Normal | TSOPII 44L |
| GLT6200L16LLI-70TC | 70ns | Normal | TSOPII 44L |
| GLT6200L16LLI-85TC | 85ns | Normal | TSOPII 44L |
| GLT6200L16SL-55TC | 55ns | Normal | TSOPII 44L |
| GLT6200L16SL-70TC | 70ns | Normal | TSOPII 44L |
| GLT6200L16SL-85TC | 85ns | Normal | TSOPII 44L |
| GLT6200L16SLI-55TC | 55ns | Normal | TSOPII 44L |
| GLT6200L16SLI-70TC | 70ns | Normal | TSOPII 44L |
| GLT6200L16SLI-85TC | 85ns | Normal | TSOPII 44L |
| GLT6200L16LL-55FG | 55ns | Normal | fpBGA 48L |
| GLT6200L16LL-70FG | 70ns | Normal | fpBGA 48L |
| GLT6200L16LL-85FG | 85ns | Normal | fpBGA 48L |
| GLT6200L16LLI-55FG | 55ns | Normal | fpBGA 48L |
| GLT6200L16LLI-70FG | 70ns | Normal | fpBGA 48L |
| GLT6200L16LLI-85FG | 85ns | Normal | fpBGA 48L |
| GLT6200L16SL-55FG | 55ns | Normal | fpBGA 48L |
| GLT6200L16SL-70FG | 70ns | Normal | fpBGA 48L |
| GLT6200L16SL-85FG | 85ns | Normal | fpBGA 48L |
| GLT6200L16SLI-55FG | 55ns | Normal | fpBGA 48L |
| GLT6200L16SLI-70FG | 70ns | Normal | fpBGA 48L |
| GLT6200L16SLI-85FG | 85ns | Normal | fpBGA 48L |
| GLT6200L16LL-55FI | 55ns | Normal | fpBGA 48L |
| GLT6200L16LL-70FI | 70ns | Normal | fpBGA 48L |
| GLT6200L16LL-85FI | 85ns | Normal | fpBGA 48L |
| GLT6200L16LLI-55FI | 55ns | Normal | fpBGA 48L |
| GLT6200L16LLI-70FI | 70ns | Normal | fpBGA 48L |
| GLT6200L16LLI-85FI | 85ns | Normal | fpBGA 48L |
| GLT6200L16SL-55FI | 55ns | Normal | fpBGA 48L |
| GLT6200L16SL-70FI | 70ns | Normal | fpBGA 48L |
| GLT6200L16SL-85FI | 85ns | Normal | fpBGA 48L |
| GLT6200L16SLI-55FI | 55ns | Normal | fpBGA 48L |
| GLT6200L16SLI-70FI | 70ns | Normal | fpBGA 48L |
| GLT6200L16SLI-85FI | 85ns | Normal | fpBGA 48L |

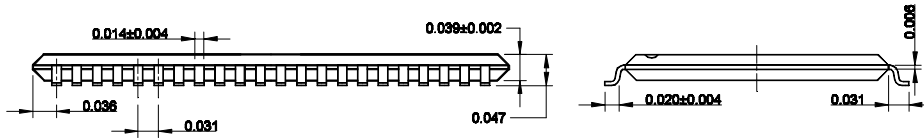
Parts Numbers (Top Mark) Definition :


Package Information

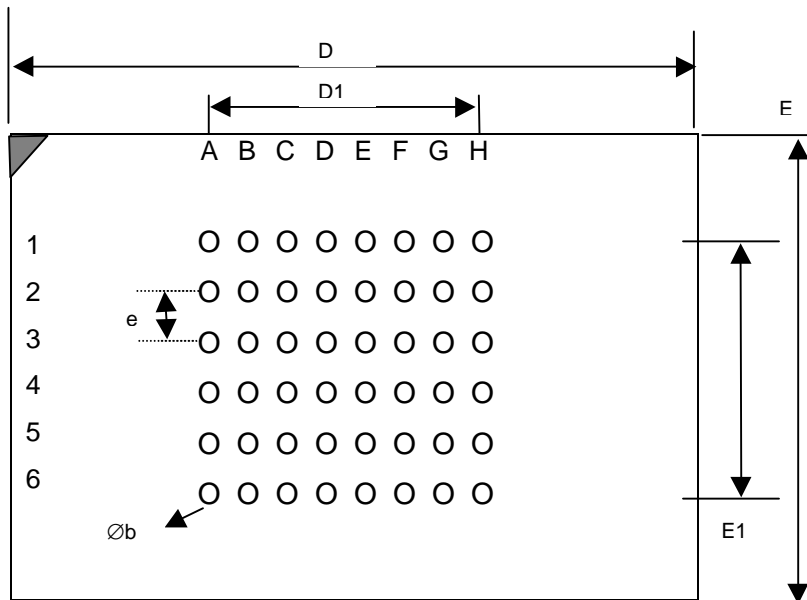
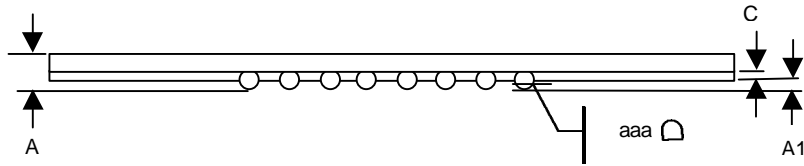
44 pin Small Outline J-form Package (TSOPII)




Unit : Inch



GLT6200L16 fpBGA



PACKAGE OUTLINE DWG.

| SYMBOL | UNIT : MM |
|---|-----------|
| A | 1.10±0.1 |
| A1 | 0.22±0.05 |
| Øb | 0.35 |
| C | 0.36TYP |
| D | 8.00±0.10 |
| D1 | 5.25 |
| E | 6.00±0.10 |
| E1 | 3.75 |
| e | 0.75TYP |
| aaa  | 0.10 |