

Microprocessor Reset IC

Features

- Precision Monitoring of +3V, +3.3V, and +5V Power-Supply Voltages
- Fully Specified Over Temperature
- Available in Three Output Configurations
 - Push-Pull $\overline{\text{RESET}}$ Output (G698L)
 - Push-Pull RESET Output (G698H)
 - Open-Drain $\overline{\text{RESET}}$ Output (G699L)
- Externally Programmable Time Delay Generator
- 14 μ A Supply Current
- Guaranteed Reset Valid to $V_{CC} = 0.8V$
- Power Supply Transient Immunity
- 5 pin SOT23-5 Packages
- 2% Threshold Accuracy

Applications

- Computers
- Controllers
- Intelligent Instruments
- Critical μ P and μ C Power Monitoring
- Portable / Battery-Powered Equipment
- Automotive

General Description

The G698/G699 are microprocessor (μ P) supervisory circuits used to monitor the power supplies in μ P and digital systems. They provide excellent circuit reliability and low cost and adjustments when used with +5V, +3.3V, +3.0V - powered circuits.

These circuits perform a single function: they assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, with hysteresis keeping it asserted for time delay determined by externally programmable time delay generator after V_{CC} has risen above the reset threshold. Reset thresholds suitable for operation with a variety of supply voltages are available.

The G699L has an open-drain output stage, while the G698 have push-pull outputs. The G699L's open-drain $\overline{\text{RESET}}$ output requires a pull-up resistor that can be connected to a voltage higher than V_{CC} . The G698L have an active-low $\overline{\text{RESET}}$ output, while the G698H has an active-high RESET output. The reset comparator is designed to ignore fast transients on V_{CC} , and the outputs are guaranteed to be in the correct logic state for V_{CC} down to 0.8V.

Low supply current makes the G698/G699 ideal for use in portable equipment. The G698/G699 are available in 5-pin SOT23-5 packages.

Ordering Information

ORDER NUMBER	TEMP. RANGE	PACKAGE
G698H(L)xxxT1U	-40°C ~ +105°C	SOT23-5
G699LxxxT1U	-40°C ~ +105°C	SOT23-5

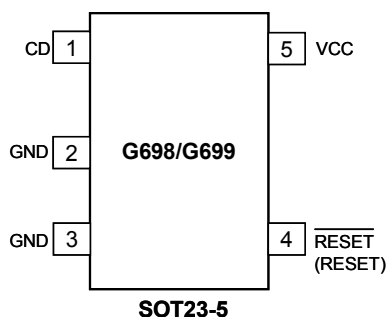
Note:T1 : SOT23-5

U : Tape & Reel

* xxx specifies the threshold voltage.

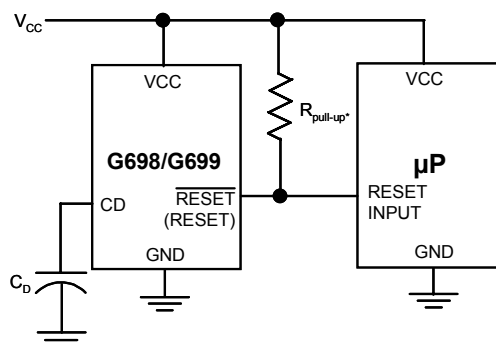
e.g. 263 denotes the 2.63V threshold voltage.

Pin Configuration



() is for G698H

Typical Application Circuit



*G699 ONLY

**Absolute Maximum Ratings**

Terminal Voltage (with respect to GND)

 V_{CC}-0.3V to +6.0VDelay Capacitor Pin Voltage, V_{CD}-0.3 to ($V_{CC} + 0.3V$)RESET, RESET (push-pull).....-0.3V to ($V_{CC} + 0.3V$)

RESET (open drain).....-0.3V to +6.0V

Input Current, V_{CC} 20mA

Output Current, RESET, RESET20mA

Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)5-Pin SOT23-5 (derate 2.17mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).174mWOperating Temperature Range -40°C to $+105^\circ\text{C}$ Storage Temperature Range..... -65°C to $+150^\circ\text{C}$ Lead Temperature (soldering, 10s)..... $+260^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = full range, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$, $V_{CC} = 5V$ for 463/438/400 versions, $V_{CC} = 3.3V$ for 308/293 versions, and $V_{CC} = 3V$ for 263 version.) (Note 1)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
V_{CC} Range		$T_A = 0^\circ\text{C} + 70^\circ\text{C}$	0.8	---	5.5	V
		$T_A = -40^\circ\text{C} + 105^\circ\text{C}$	1	---	5.5	
Supply Current (SOT23-5)	I_{CC}	$V_{CC} < 5.5V$, G69_ 463/438/400/330_	---	16.5	25	μA
		$V_{CC} < 3.6V$, G69_ 308/293/263_	---	13.9	22	
Reset Threshold	V_{TH}	G69_ 463_	4.50	4.60	4.69	V
		G69_ 438_	4.23	4.32	4.40	
		G69_ 400_	3.88	3.96	4.04	
		G69_ 330_	3.25	3.30	3.37	
		G69_ 308_	3.04	3.10	3.16	
		G69_ 293_	2.86	2.91	2.96	
		G69_ 263_	2.59	2.64	2.69	
Reset Threshold Hysteresis	V_{HYS}		3.6	5.3	7	%
Reset Threshold Tempco			---	70	---	ppm/ $^\circ\text{C}$
C_D Delay Pin Threshold Voltage	V_{TDC}		0.87	1.25	1.29	V
Delay Capacitor Pin Sink Current	I_{CD}	$V_{CC} = 1.5V$, $V_{CD} = 0.5V$	3	5	---	mA
Delay Capacitor Pin Source Current		$V_{CC} > V_{TH} + V_{HYS}$	0.5	0.88	1.2	μA
RESET Output Current Low (push-pull active low, and open-drain active-low, G698L and G699L)	I_{OL}	$V_{CC} = 2.5V$, $V_{RESET} = 0.5V$	8	---	---	mA
RESET Output Current High (push-pull active low, G698L)	I_{OH}	$V_{CC} = 5V$, $V_{RESET} = 4.5V$, G698L463/438/400/330	4.5	---	---	mA
		$V_{CC} = 3.3V$, $V_{RESET} = 2.8V$, G698L308/293	3	---	---	
		$V_{CC} = 3V$, $V_{RESET} = 2.5V$, G698L263	2	---	---	
RESET Output Current Low (push-pull active high, G698H)	I_{OL}	$V_{CC} = 5V$, $V_{RESET} = 0.5V$, G698H463/438/400/330	16	---	---	mA
		$V_{CC} = 3.3V$, $V_{RESET} = 0.5V$, G698H308/293	12	---	---	
		$V_{CC} = 3V$, $V_{RESET} = 0.5V$, G698H263	10	---	---	
RESET Output Current High (push-pull active high, G698H)	I_{OH}	$V_{CC} = 2.5V$, $V_{RESET} = 2V$	2	---	---	mA
RESET Open-Drain Output Leakage Current (G699L)		$V_{CC} > V_{TH}$, RESET deasserted	---	---	1	μA

Note 1: Production testing done at $T_A = +25^\circ\text{C}$; limits over temperature guaranteed by design.

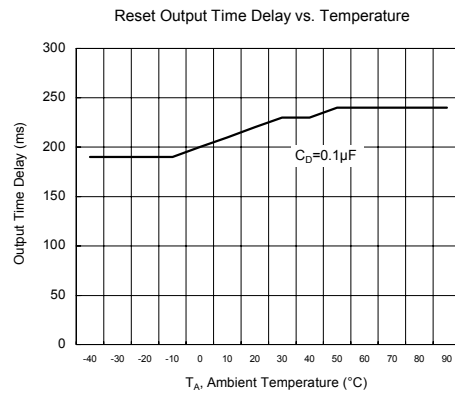
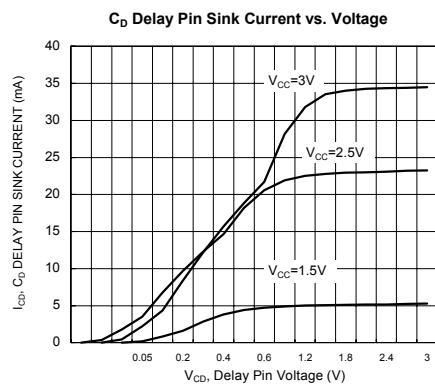
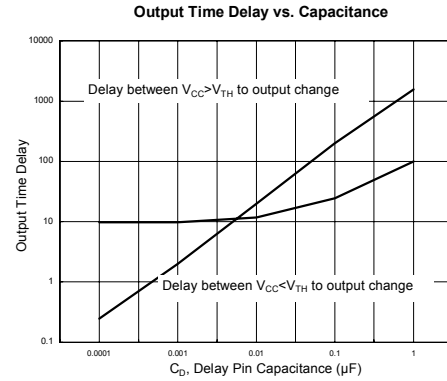
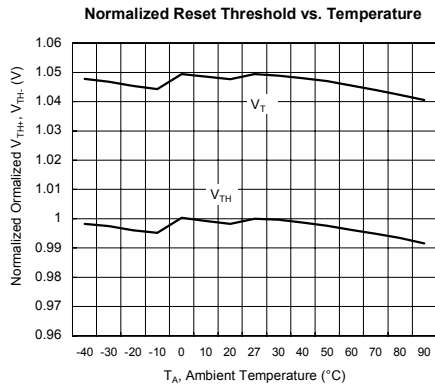
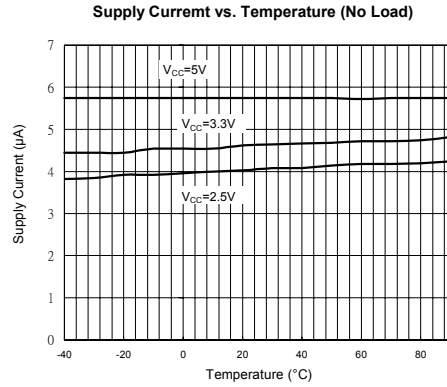
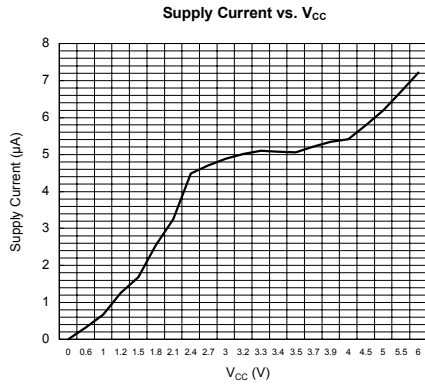
**Selector Guide**

PART/SUFFIX	RESET THRESHOLD (V)	OUTPUT TYPE	TOP MARK
G699L463T1U	4.60	Open-Drain $\overline{\text{RESET}}$	699Gx
G699L438T1U	4.32	Open-Drain $\overline{\text{RESET}}$	699Fx
G699L400T1U	3.96	Open-Drain $\overline{\text{RESET}}$	699Ex
G699L330T1U	3.30	Open-Drain $\overline{\text{RESET}}$	699Dx
G699L308T1U	3.10	Open-Drain $\overline{\text{RESET}}$	699Cx
G699L293T1U	2.91	Open-Drain $\overline{\text{RESET}}$	699Bx
G699L263T1U	2.64	Open-Drain $\overline{\text{RESET}}$	699Ax
G698H463T1U	4.60	Push-Pull $\overline{\text{RESET}}$	698Lx
G698H438T1U	4.32	Push-Pull $\overline{\text{RESET}}$	698Kx
G698H400T1U	3.96	Push-Pull $\overline{\text{RESET}}$	698Jx
G698H330T1U	3.30	Push-Pull $\overline{\text{RESET}}$	698Nx
G698H308T1U	3.10	Push-Pull $\overline{\text{RESET}}$	698Ix
G698H293T1U	2.91	Push-Pull $\overline{\text{RESET}}$	698Hx
G698H263T1U	2.64	Push-Pull $\overline{\text{RESET}}$	698Gx
G698L463T1U	4.60	Push-Pull $\overline{\text{RESET}}$	698Fx
G698L438T1U	4.32	Push-Pull $\overline{\text{RESET}}$	698Ex
G698L400T1U	3.96	Push-Pull $\overline{\text{RESET}}$	698Dx
G698L330T1U	3.30	Push-Pull $\overline{\text{RESET}}$	698Mx
G698L308T1U	3.10	Push-Pull $\overline{\text{RESET}}$	698Cx
G698L293T1U	2.91	Push-Pull $\overline{\text{RESET}}$	698Bx
G698L263T1U	2.64	Push-Pull $\overline{\text{RESET}}$	698Ax



Typical Operating Characteristics

(V_{CC} = full range, T_A = -40°C to $+105^{\circ}\text{C}$, unless otherwise noted. Typical values are at T_A = $+25^{\circ}\text{C}$, V_{CC} = 5V for 463/438/400/330 versions, V_{CC} = 3.3V for 308/293 versions, and V_{CC} = 3V for 263 version.)



Timing Diagram

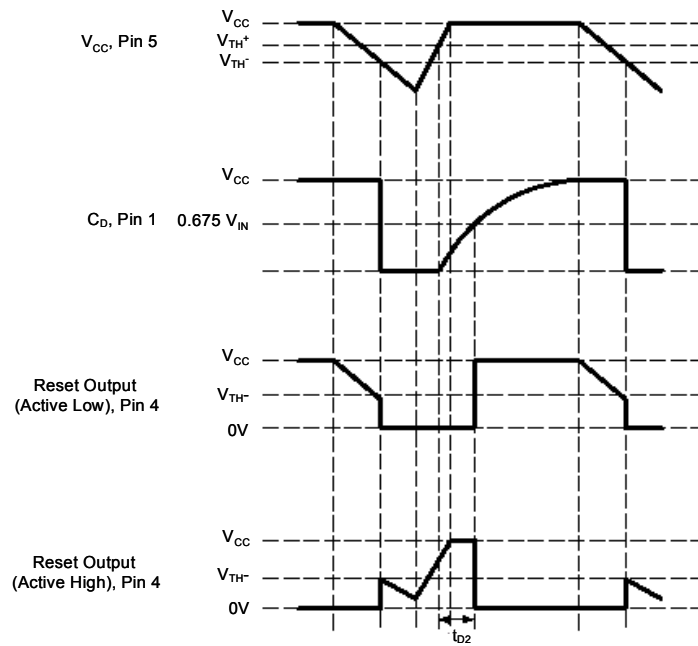


Figure 1

Functional Diagram

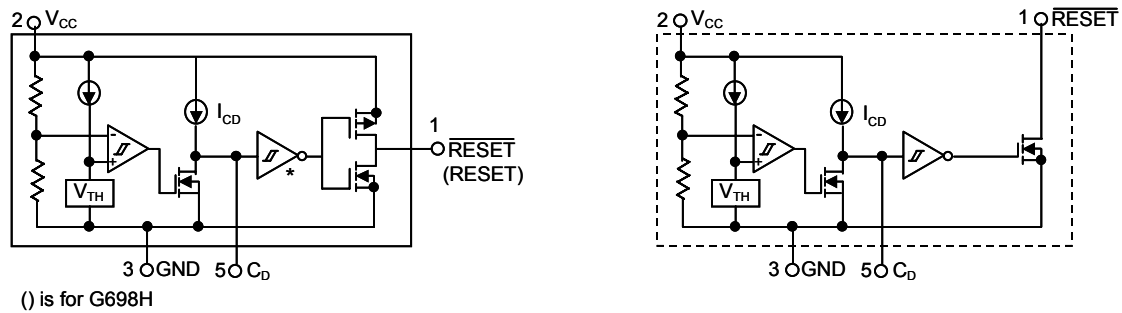


Figure 2

Pin Description

PIN	NAME	FUNCTION
1	CD	External Programmable time delay is set by the capacitor connect to C_D pin.
2,3	GND	Ground
4	$\overline{\text{RESET}}$ (G698L/G699L)	$\overline{\text{RESET}}$ Output remains low while V_{CC} is below the reset threshold, and for delay time set by C_D after V_{CC} rises above the reset threshold.
	RESET (G698H)	RESET Output remains high while V_{CC} is below the reset threshold, and for delay time set by C_D after V_{CC} rises above the reset threshold.
5	VCC	Supply Voltage (+5V, +3.3V, +3.0V)

Detailed Description

A microprocessor's (μP 's) reset input starts the μP in a known state. The G699L/G698L/G698H assert reset to prevent code-execution errors during power-up, power-down, or brownout conditions. They assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold (V_{TH-}), keeping it asserted for time delay set by capacitor connected to C_D pin, after V_{CC} has risen above the high reset threshold V_{TH+} ($V_{TH-} + V_{HYS}$). The G699L uses an open-drain output, and the G698L/G698H have a push-pull output stage. Connect a pull-up resistor on the G699L's $\overline{\text{RESET}}$ output to any supply between 0 and 5.5V.

The time delay is set by external capacitor C_D , and internal pull up current I_{CD} . When the voltage at C_D pin exceeds the buffer threshold, typically 1.25V, the $\overline{\text{RESET}}$ output high (RESET output low). The voltage detector and buffer have built-in hysteresis to prevent erratic reset operation. The formula of time delay is $T \text{ (ms)} \cong 1685 C_D \text{ (}\mu\text{F)}$. Fig1 and Fig2 show a timing diagram and a Functional Block.

Ensuring a Valid Reset Output Down to $V_{CC} = 0$

When V_{CC} falls below 0.8V, the G698 $\overline{\text{RESET}}$ output no longer sinks current—it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to $\overline{\text{RESET}}$ can drift to undetermined voltages. This presents no problem in most applications since most μP and other circuitry is inoperative with V_{CC} below 0.8V. However, in applications where $\overline{\text{RESET}}$

must be valid down to 0V, adding a pull-down resistor to $\overline{\text{RESET}}$ causes any stray leakage currents to flow to ground, holding $\overline{\text{RESET}}$ low (Figure 3). R1's value is not critical; 100k Ω is large enough not to load $\overline{\text{RESET}}$ and small enough to pull $\overline{\text{RESET}}$ to ground.

A 100k Ω pull-up resistor to V_{CC} is also recommended for the G699L if $\overline{\text{RESET}}$ is required to remain valid for $V_{CC} < 0.8V$.

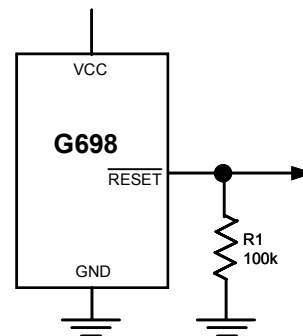


Figure3. $\overline{\text{RESET}}$ Valid to $V_{CC} = \text{Ground}$ Circuit

Interfacing to μ Ps with Bidirectional Reset Pins

Since the $\overline{\text{RESET}}$ output on the G699L is open drain, this device interfaces easily with μ Ps that have bidirectional reset pins, such as the Motorola 68HC11. Connecting the μ P supervisor's $\overline{\text{RESET}}$ output directly to the microcontroller's (μ C's) $\overline{\text{RESET}}$ pin with a single pull-up resistor allows either device to assert reset (Figure 4).

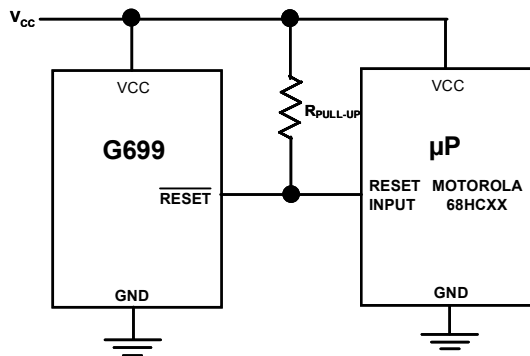


Figure 4. Interfacing to μ Ps with Bidirectional Reset I/O

G699L Open-Drain $\overline{\text{RESET}}$ Output Allows Use with Multiple Supplies

Generally, the pull-up connected to the G699L will connect to the supply voltage that is being monitored at the IC's V_{CC} pin. However, some systems may use the open-drain output to level-shift from the monitored supply to reset circuitry powered by some other supply (Figure 5). Note that as the G699L's V_{CC} decreases below 1V, so does the IC's ability to sink current at $\overline{\text{RESET}}$. Also, with any pull-up, $\overline{\text{RESET}}$ will be pulled high as V_{CC} decays toward 0. The voltage where this occurs depends on the pull-up resistor value and the voltage to which it is connected.

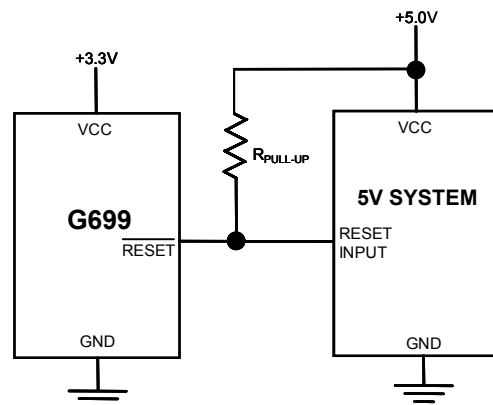


Figure 5. G699L Open-Drain $\overline{\text{RESET}}$ Output Allows Use with Multiple Supplies

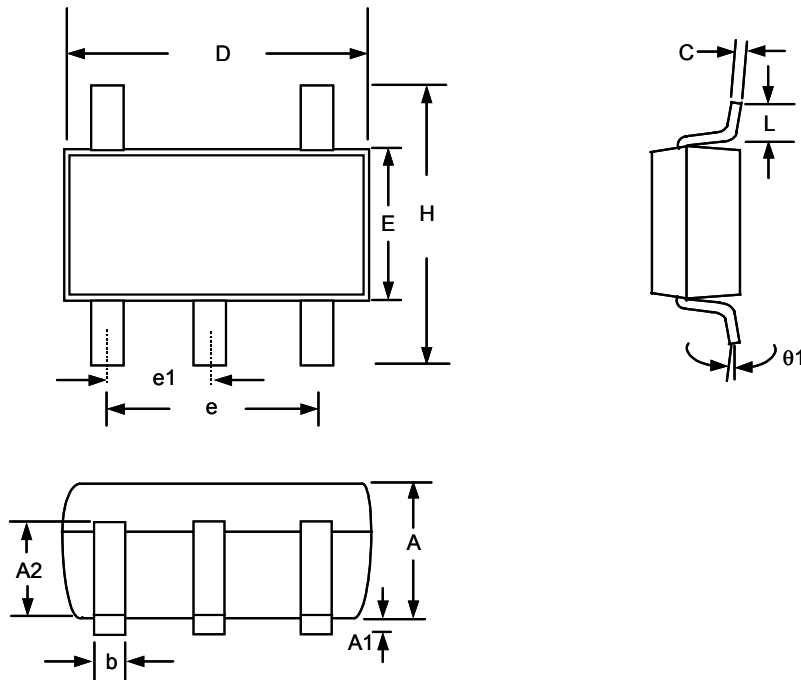
Benefits of Highly Accurate Reset Threshold

Most μ P supervisor ICs have reset threshold voltages between 5% and 10% below the value of nominal supply voltages. This ensures a reset will not occur within 5% of the nominal supply, but will occur when the supply is 10% below nominal.

When using ICs rated at only the nominal supply $\pm 5\%$, this leaves a zone of uncertainty where the supply is between 5% and 10% low, and where the reset may or may not be asserted.

The G69_463/G69_308 use highly accurate circuitry to ensure that reset is asserted close to the 5% limit, and long before the supply has declined to 10% below nominal.

Package Information

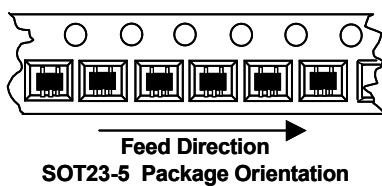


Note:

1. Package body sizes exclude mold flash protrusions or gate burrs
2. Tolerance ± 0.1000 mm (4mil) unless otherwise specified
3. Coplanarity: 0.1000mm
4. Dimension L is measured in gage plane

SYMBOL	DIMENSIONS IN MILLIMETER		
	MIN	NOM	MAX
A	1.00	1.10	1.30
A1	0.00	----	0.10
A2	0.70	0.80	0.90
b	0.35	0.40	0.50
C	0.10	0.15	0.25
D	2.70	2.90	3.10
E	1.40	1.60	1.80
e	----	1.90(TYP)	----
e1	----	0.95	----
H	2.60	2.80	3.00
L	0.37	----	----
$\theta 1$	1°	5°	9°

Taping Specification



GMT Inc. does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and GMT Inc. reserves the right at any time without notice to change said circuitry and specifications.

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