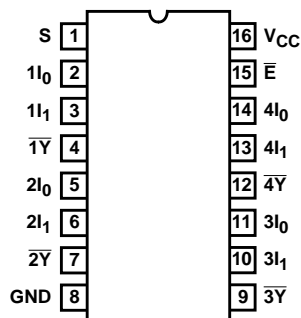


September 1997

### Features

- Common Select Inputs
- Separate Enable Inputs
- Buffered inputs and Outputs
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Pinout

 CD74HC157, CD74HCT157, CD74HC158, CD74HCT158  
 (PDIP, SOIC)  
 TOP VIEW


### Description

The Harris CD74HC157, CD74HCT157, CD74HC158 and CD74HCT158 are quad 2-input multiplexers which select four bits of data from two sources under the control of a common Select input (S). The Enable input ( $\bar{E}$ ) is active Low. When ( $\bar{E}$ ) is High, all of the outputs in the 158, the inverting type, ( $1\bar{Y}$ - $4\bar{Y}$ ) are forced High and in the 157, the non-inverting type, all of the outputs ( $1Y$ - $4Y$ ) are forced Low, regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of these devices. The state of the Select input determines the particular register from which the data comes. They can also be used as function generators.

### Ordering Information

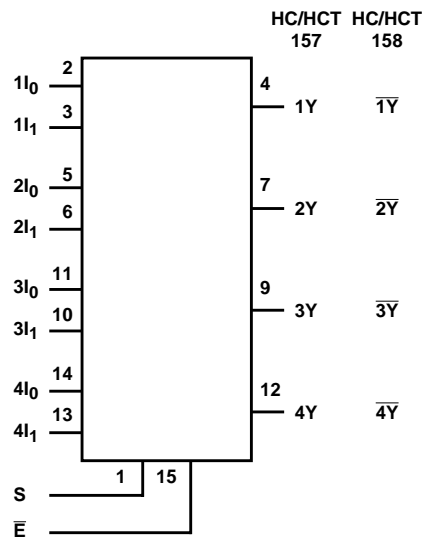
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC157E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT157E	-55 to 125	16 Ld PDIP	E16.3
CD74HC158E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT158E	-55 to 125	16 Ld PDIP	E16.3
CD74HC157M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT157M	-55 to 125	16 Ld SOIC	M16.15
CD74HC158M	-55 to 125	16 Ld SOIC	M16.15

#### NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer or die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

# CD74HC157, CD74HCT157, CD74HC158, CD74HCT158

## Functional Diagram



TRUTH TABLE

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT	
				157	158
$\bar{E}$	S	I0	I1	Y	$\bar{Y}$
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care

# CD74HC157, CD74HCT157, CD74HC158, CD74HCT158

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$	$\pm 50mA$

## Thermal Information

Thermal Resistance (Typical, Note 3)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package	90
SOIC Package	115
Maximum Junction Temperature	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$ (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range ( $T_A$ )	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types	.2V to 6V
HCT Types	4.5V to 5.5V
DC Input or Output Voltage, $V_I$ , $V_O$	0V to $V_{CC}$
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V <sub>IH</sub>	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
-			-	-	-	-	-	-	-	-	V	
-			4.5	3.98	-	-	3.84	-	3.7	-	V	
-5.2			6	5.48	-	-	5.34	-	5.2	-	V	
High Level Output Voltage TTL Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
-			-	-	-	-	-	-	-	-	V	
4			4.5	-	-	0.26	-	0.33	-	0.4	V	
5.2			6	-	-	0.26	-	0.33	-	0.4	V	
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
-			-	-	-	-	-	-	-	-	V	
4			4.5	-	-	0.26	-	0.33	-	0.4	V	
5.2			6	-	-	0.26	-	0.33	-	0.4	V	
Low Level Output Voltage TTL Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
-			-	-	-	-	-	-	-	-	V	
4			4.5	-	-	0.26	-	0.33	-	0.4	V	
5.2			6	-	-	0.26	-	0.33	-	0.4	V	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	-	6	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	μA

**CD74HC157, CD74HCT157, CD74HC158, CD74HCT158**

**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> and GND	0	5.5	-		±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE: For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

**HCT Input Loading Table**

INPUT	UNIT LOADS	
	HCT157	HCT158
I (All)	0.95	0.4
$\bar{E}$	0.6	0.6
S	3	2.8

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

**Switching Specifications** Input t<sub>r</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC/HCT157 TYPES											
Propagation Delay (Figure 1) Data to Output	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	125	-	155	-	190	ns
			4.5	-	-	25	-	31	-	38	ns
C <sub>L</sub> =15pF		5	-	10	-	-	-	-	-	ns	
			-	12	-	-	-	-	-	ns	
HC157		C <sub>L</sub> = 50pF	6	-	-	21	-	26	-	32	ns
HCT157				-	-	21	-	26	-	32	ns

**CD74HC157, CD74HCT157, CD74HC158, CD74HCT158**

**Switching Specifications** Input  $t_r, t_f = 6\text{ns}$  (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Enable to Output	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	135	-	170	-	205	ns
			4.5	-	-	27	-	34	-	41	ns
		C <sub>L</sub> =15pF	5	-	11	-	-	-	-	-	ns
				-	12	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	23	-	29	-	35	ns
Select to Output	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	145	-	180	-	220	ns
			4.5	-	-	29	-	36	-	44	ns
		C <sub>L</sub> =15pF	5	-	12	-	-	-	-	-	ns
				-	15	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	25	-	31	-	38	ns
Power Dissipation Capacitance (Notes 4, 5)	C <sub>PD</sub>	-	5								
HC157				-	62	-	-	-	-	-	pF
HCT157				-	70	-	-	-	-	-	pF
HC/HCT158 TYPES											
Data to Output	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	140	-	175	-	210	ns
			4.5	-	-	28	-	35	-	42	
		C <sub>L</sub> =15pF	5	-	11	-	-	-	-	-	ns
				-	13	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	24	-	30	-	36	ns
Enable to Output	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	160	-	200	-	240	ns
			4.5	-	-	32	-	40	-	48	ns
		C <sub>L</sub> =15pF	5	-	13	-	-	-	-	-	ns
				-	15	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	27	-	34	-	41	ns
Select to Output	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	150	-	190	-	225	ns
			4.5	-	-	30	-	38	-	45	ns
		C <sub>L</sub> =15pF	5	-	12	-	-	-	-	-	ns
				-	14	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	26	-	33	-	38	ns
Output Transition Time	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Power Dissipation Capacitance (Notes 4, 5)	C <sub>PD</sub>	-	5								
HC158				-	35	-	-	-	-	-	pF
HCT 158				-	35	-	-	-	-	-	pF
Input Capacitance	C <sub>IN</sub>	C <sub>L</sub> = 50pF	-	-	-	10	-	10	-	10	pF

**NOTES:**

- $C_{PD}$  is used to determine the dynamic power consumption, per multiplexer.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

## Test Circuits and Waveforms

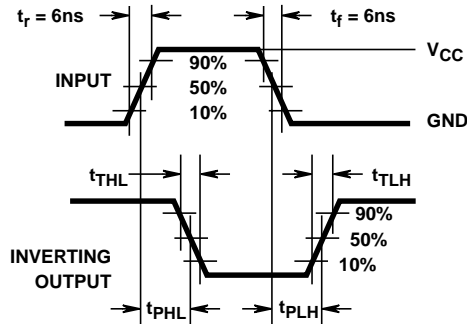


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

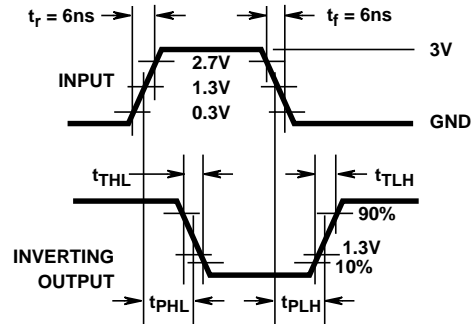


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

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