

2SJ486

Silicon P Channel MOS FET
Low Frequency Power Switching

HITACHI

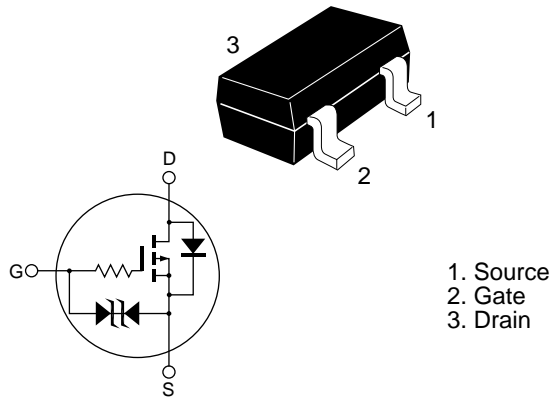
ADE-208-512 A
2nd. Edition

Features

- Low on-resistance
 $R_{DS(on)} = 0.5 \Omega$ typ. (at $V_{GS} = -4V$, $I_D = -100$ mA)
- 2.5V gate drive devices.
- Small package (MPAK).

Outline

MPAK



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	−30	V
Gate to source voltage	V _{GSS}	±10	V
Drain current	I _D	−0.3	A
Drain peak current	I _{D(pulse)} ^{*1}	−0.6	A
Channel dissipation	P _{ch}	150	mW
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	−55 to +150	°C

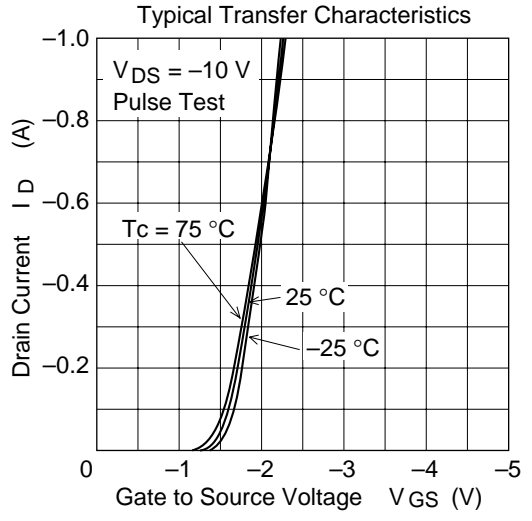
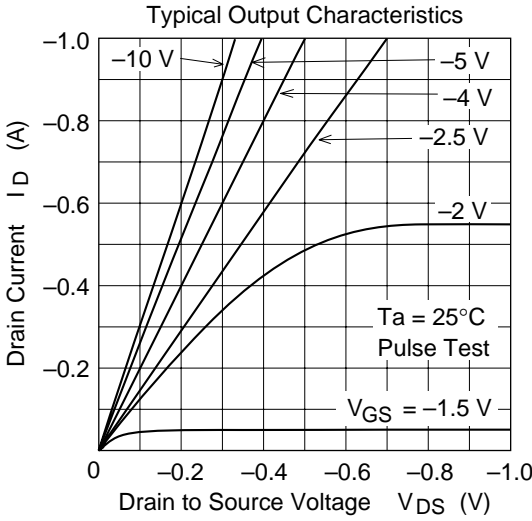
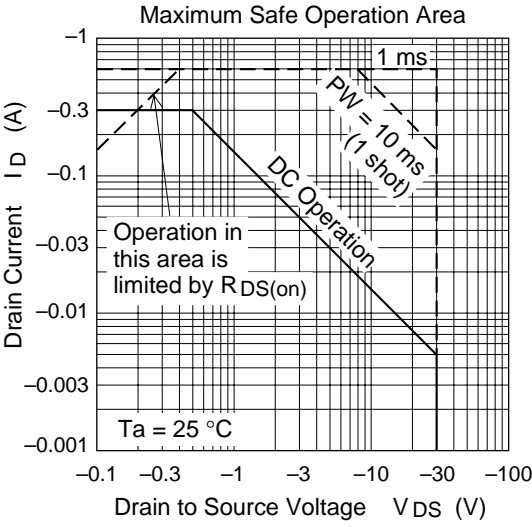
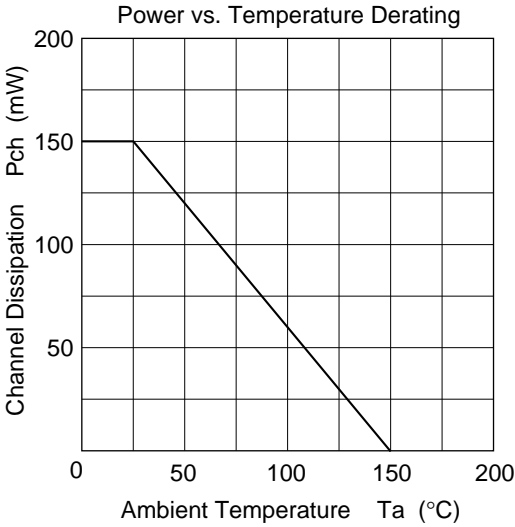
Note: 1. PW ≤ 10μs, duty cycle ≤ 1 %

Electrical Characteristics (Ta = 25°C)

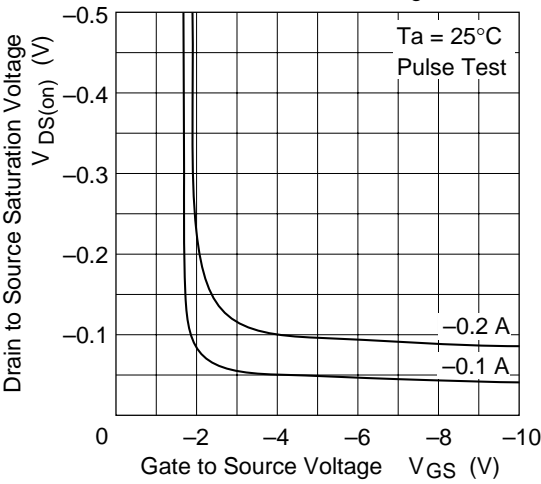
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR)DSS}	−30	—	—	V	I _D = −10μA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR)GSS}	±10	—	—	V	I _G = ±100μA, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	−1.0	μA	V _{DS} = −30 V, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±5.0	μA	V _{GS} = ±6.5V, V _{DS} = 0
Gate to source cutoff voltage	V _{GS(off)}	−0.5	—	−1.5	V	I _D = −10μA, V _{DS} = −5V
Static drain to source on state resistance	R _{DS(on)}	—	0.5	0.65	Ω	I _D = −100mA V _{GS} = −4V ^{*1}
	R _{DS(on)}	—	0.7	1.2	Ω	I _D = −40mA V _{GS} = −2.5V ^{*1}
Forward transfer admittance	y _{fs}	0.4	0.65	—	S	I _D = −100mA V _{DS} = −10V ^{*1}
Input capacitance	C _{iss}	—	45	—	pF	V _{DS} = −10V
Output capacitance	C _{oss}	—	76	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	5.4	—	pF	f = 1MHz
Turn-on delay time	t _{d(on)}	—	120	—	ns	V _{GS} = −4V
Rise time	t _r	—	340	—	ns	I _D = −150mA
Turn-off delay time	t _{d(off)}	—	850	—	ns	R _L = 66.6Ω
Fall time	t _f	—	550	—	ns	

Notes: 1. Pulse test
2. Marking is “ZU−”.

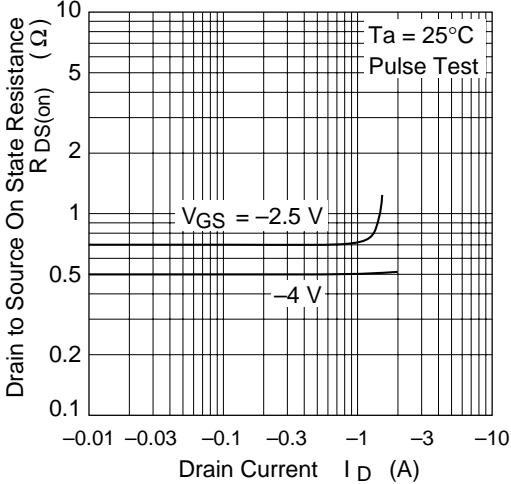
Main Characteristics



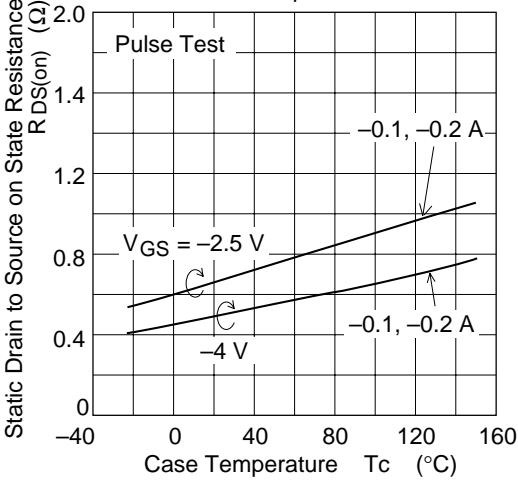
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



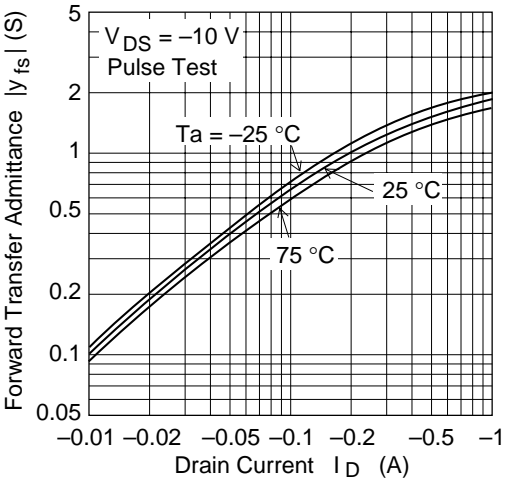
Static Drain to Source on State Resistance
vs. Drain Current



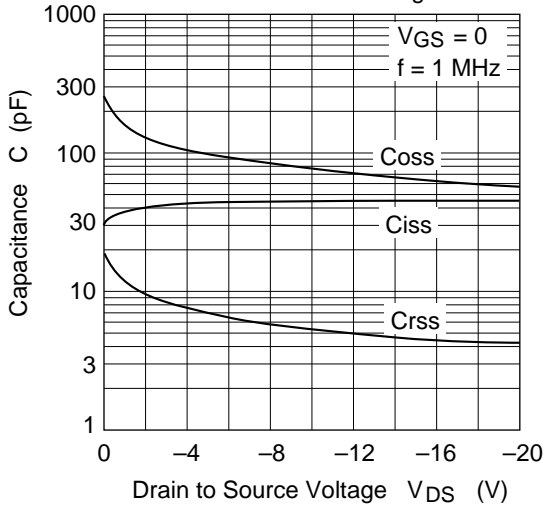
Static Drain to Source on State Resistance
vs. Temperature



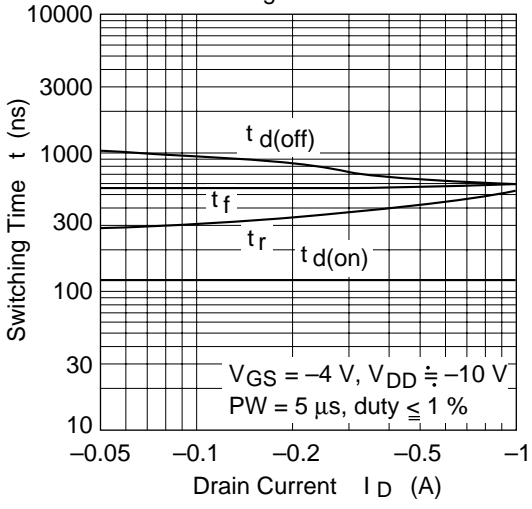
Forward Transfer Admittance vs.
Drain Current



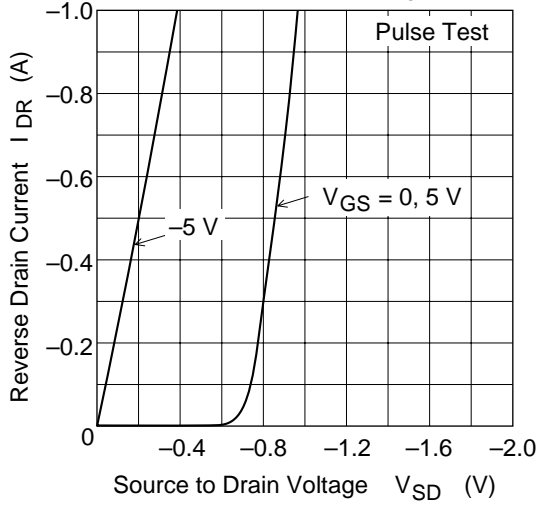
Typical Capacitance vs.
Drain to Source Voltage



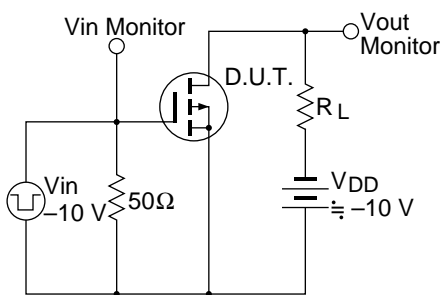
Switching Characteristics



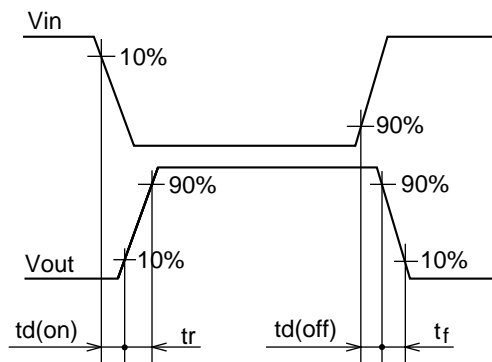
Reverse Drain Current vs.
Source to Drain Voltage



Switching Time Test Circuit

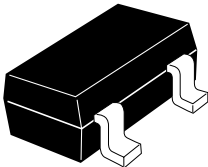
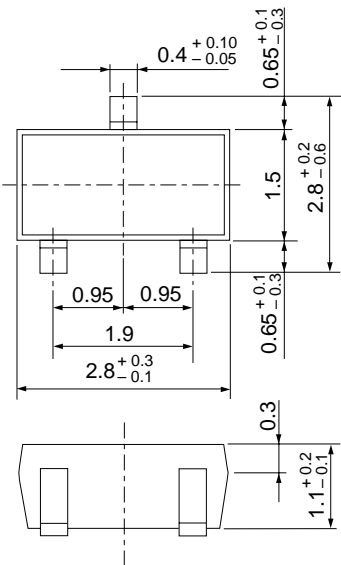


Waveform



Package Dimensions

Unit: mm



Hitachi Code	MPAK
EIAJ	SC-59A
JEDEC	TO-236Mod

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