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# HD66137T

High-Voltage Durable 240-Channel Common Driver  
for Dot-Matrix STN LCD

# HITACHI

ADE-207-291(Z)

Rev. 2

Aug. 03, 1999

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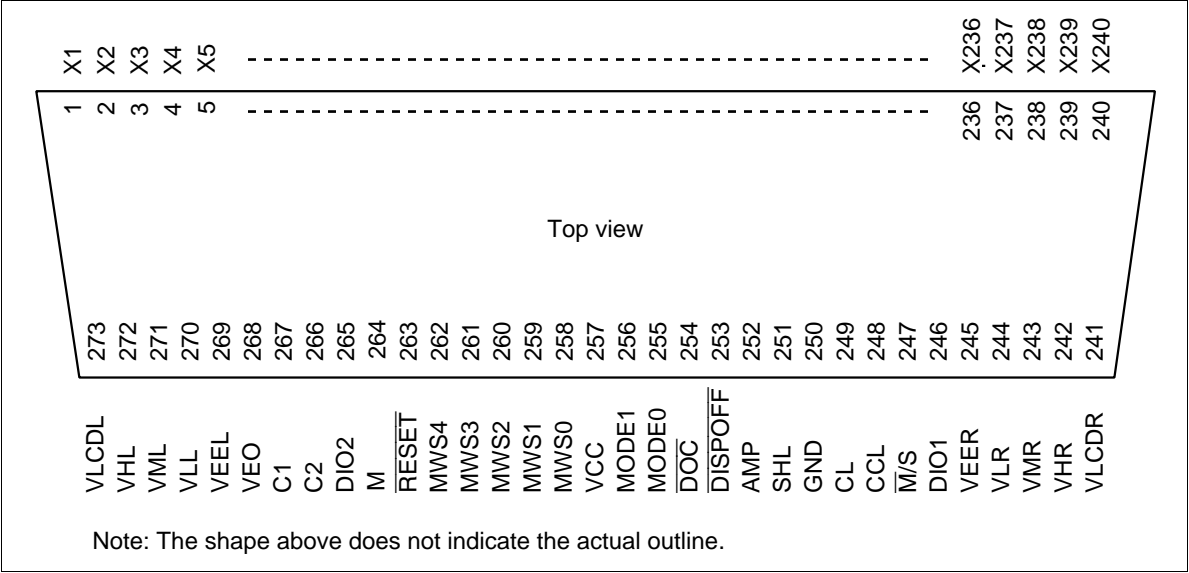
## Description

The HD 66137T is a 240-channel common driver which drives a dot matrix STN LCD panel. By changing the mode, this can be applied to 240- and 200- and 160- channel output. Through the use of a 43-V high-voltage CMOS process technology, a high-voltage drive of +21.5 V and -21.5 V, centering on VM is possible. -21.5V generated from +21.5 V with built-in switching circuit and external capacity. Low logic-drive voltage (3 V) is used. This device is used together with the segment driver HD66130, HD66134ST or HD66136.

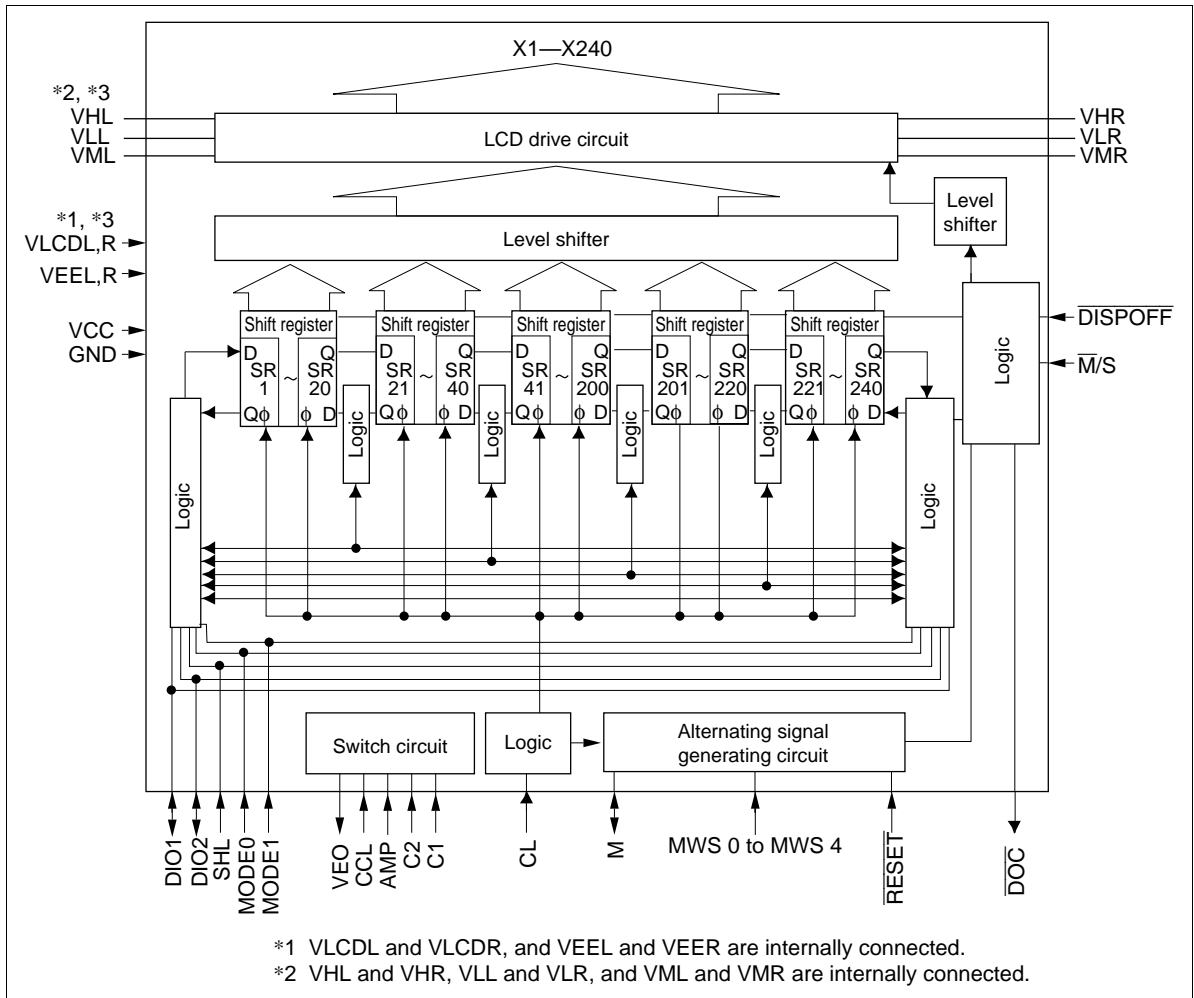
## Features

- Display duty: Up to 1/240
- LCD drive voltage: 43 V max
- Built-in switching circuit (to generate -21.5 V)
- Number of LCD drive circuit: 240
- Operating voltage: 2.5 to 5.5 V
- Intermediate voltage I/F
- Built-in alternating signal generation circuit Pin programmable
- Output mode change: 240-output mode  
200-output mode  
160-output mode
- Built-in display-off function
- Flex TCP

Pin Arrangement



## Block Diagram



Internal Block Diagram

1. LCD drive Circuit

This circuit selects and outputs the three level signals for the LCD drive. By a combination of the data in the shift register and M, either VH, VL, or VM is selected and transmitted to the output circuit.

2. Level shifter

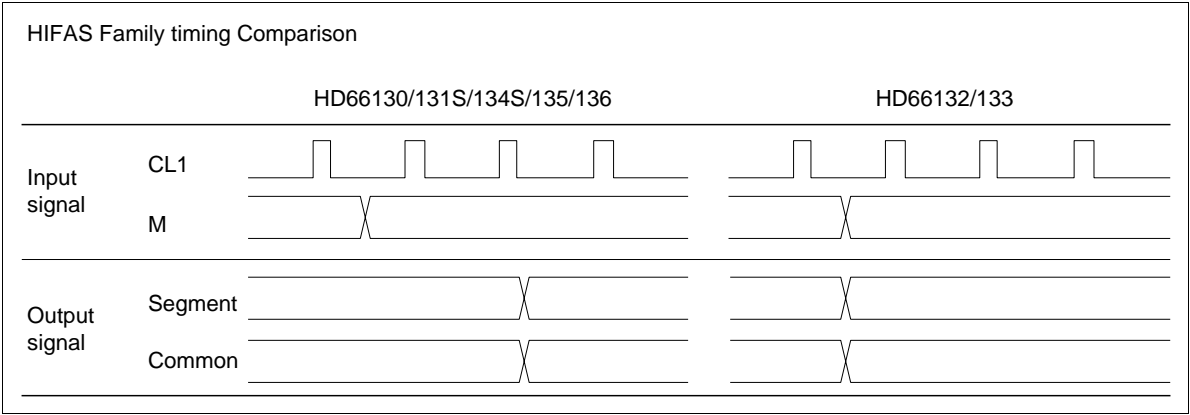
This boosts a 5-V signal to a high-voltage signal for LCD drive.

3. Shift register

This is a 240-bit bidirectional shift register circuit. The first line marker signal output from the DIO1 pin and DIO2 pin is sequentially shifted by shift clock CL. The shift direction is determined by the SHL pin.

4. Alternating signal generating circuit

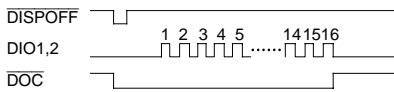
This circuit generates an alternating signal (M signal) for LCD display. To suppress cross-talk, the signal is alternated in a unit from several lines to several tens of lines. By connecting MWS0 to MWS4 pins to V<sub>CC</sub> or GND, the desired number of signals can be alternated. When alternating signals are externally input, all pins (MWS0 to MWS4) are connected to GND.



Pin Function

| Classification | Symbol  | Pin No.  | Connected to            | I/O  | Functions  |                     |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
|----------------|---|--|-------------------------|--|--|---------------------|---------------------------|--------------|------|------|------|------|---------------------------|--------------|---|---|---|---|---|---|---|-------|---|---|---|---|---|---|------------|--------|---|---|---|---|---|---|--------------------|--|---|---|---|---|---|---|--------------------|--|---|---|---|---|---|---|---|--|----|---|---|---|---|---|---------------------|--|
| Power supply   | VLCDL, R  | 273, 241   | Power supply            | —  | VLCDL, R–VEEL, R : Power supply for LCD drive  |                     |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
|                | VEEL, R   | 269, 245   |                         |  | VLCDL, R : Power supply for switch circuit   |                     |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
|                | V <sub>CC</sub> , R   | 257  |                         |  | V <sub>CC</sub> –GND : Power supply for logic circuit  |                     |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
|                | GND   | 250  |                         |  |  |                     |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
|                | VHL, R  | 272, 242   | Power supply            | Input  | Power supply for LCD drive level   |                     |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
| VLL, R         | 270, 244  | VHL, R : Selected level (Set to the same voltage as VLCDL, R.)   |                         |  |  |                     |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
| VML, R         | 271, 243  | VLL, R : Selected level (Set to the same voltage as VEEL, R.)<br>VML, R : Non-selected level and Power supply for switch circuit |                         |  |  |                     |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
| VEO            | 268   | VEEL, R  | output                  | When use built -in switching circuit and generate VEE, VEO pin connect to VEEL, R pins. VM voltage is point of reference and reversed and output the voltage input to the voltage between VLCD and VM. If built-in switching circuit is not used, don't connect any lines to this pin. |  |                     |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
| C1, C2         | 267, 266  | Capacitance  | —                       | External capacitance should be connected here when using the switch circuit for generate VEE.<br>If built-in switching circuit is not used, don't connect any lines to this pin.   |  |                     |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
| Control signal | CL  | 249  | MPU                     | Input  | Shift clock input. Data is shifted at the falling edge of shift clock CL of the shift register.  |                     |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
|                | M   | 264  | Extension driver or MPU | I/O  | Inputs or outputs the alternating current for LCD drive output.  |                     |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
|                | MWS0  | 258  | —                       | Input  | This pin specifies the cycle of the alternating signal (M signal) in the unit of the number of lines. The number of lines, which is an integer from 2 to 31, is specified as follows. Usually, specify the number of lines within a range from 10 to 31. When the HD66131T is driven by an external alternating signal, specify the number of lines as zero. |                     |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
|                | MWS1  | 259  |                         |  |  |                     |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
|                | MWS2  | 260  |                         |  |  |                     |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
|                | MWS3  | 261  |                         |  |  |                     |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
|                | MWS4  | 262  |                         |  |  |                     |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
|                | <table><tr><th>Number of lines</th><th>MWS4</th><th>MWS3</th><th>MWS2</th><th>MWS1</th><th>MWS0</th><th>Line alternating waveform</th><th>M-pin status</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>—</td><td>Input</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Prohibited</td><td>Output</td></tr><tr><td>2</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2 lines alternated</td><td></td></tr><tr><td>3</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>3 lines alternated</td><td></td></tr><tr><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td></td></tr><tr><td>31</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>31 lines alternated</td><td></td></tr></table> |  |                         |  |  |                     | Number of lines           | MWS4         | MWS3 | MWS2 | MWS1 | MWS0 | Line alternating waveform | M-pin status | 0 | 0 | 0 | 0 | 0 | 0 | — | Input | 1 | 0 | 0 | 0 | 0 | 1 | Prohibited | Output | 2 | 0 | 0 | 0 | 1 | 0 | 2 lines alternated |  | 3 | 0 | 0 | 0 | 1 | 1 | 3 lines alternated |  | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |  | 31 | 1 | 1 | 1 | 1 | 1 | 31 lines alternated |  |
|                | Number of lines   | MWS4   | MWS3                    | MWS2   | MWS1   | MWS0                | Line alternating waveform | M-pin status |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
|                | 0   | 0  | 0                       | 0  | 0  | 0                   | —                         | Input        |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
| 1              | 0   | 0  | 0                       | 0  | 1  | Prohibited          | Output                    |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
| 2              | 0   | 0  | 0                       | 1  | 0  | 2 lines alternated  |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
| 3              | 0   | 0  | 0                       | 1  | 1  | 3 lines alternated  |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
| ⋮              | ⋮   | ⋮  | ⋮                       | ⋮  | ⋮  | ⋮                   |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |
| 31             | 1   | 1  | 1                       | 1  | 1  | 31 lines alternated |                           |              |      |      |      |      |                           |              |   |   |   |   |   |   |   |       |   |   |   |   |   |   |            |        |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |                    |  |   |   |   |   |   |   |   |  |    |   |   |   |   |   |                     |  |

Pin Functions (cont)

| Classification   | Symbol                                | Pin No.   | Connected to            | I/O  | Function   |
|--|---------------------------------------|---|-------------------------|--|--|
| Control signal   | MODE0                                 | 256   | —                       | Input  | Switch terminals for the number of LCD drive output pins.          |
|  | MODE1                                 | 256   |                         |  |  |
|  | <b>MODE0 MODE1    Shift direction</b> |   |                         |  |  |
|  | "H"    "H"                            | 240 - output (X1, X2, X3.....X238, X239, X240)    |                         |  |  |
|  | "H"    "L"                            | 200 - output (X21, X22, X23.....X218, X219, X220) |                         |  |  |
|  | "L"    "H"                            | 160 - output (X41, X42, X43.....X198, X199, X200) |                         |  |  |
|  | "L"    "L"                            | Prohibited  |                         |  |  |
|  | DIO1                                  | 246   | Extension driver or MPU | I/O  | Serial data input output pin                                       |
|  | DIO2                                  | 265   |                         |  |  |
| <b>SHL                      DIO1                      DIO2</b>   |                                       |   |                         |  |  |
|  | "H" level                             |   | serial output pin       | serial input pin   |  |
|  | "L" level                             |   | seiral input pin        | seiral output pin  |  |
| CCL  | 248                                   | MPU   | Input                   | Built-in switching circuit clock input. When use built-in switching circuit and generate V <sub>EE</sub> , this pin connect CL pin.<br>If built-in switching circuit is not used, CCL must be fixed to GND |  |
| AMP  | 252                                   | —   | Input                   | Built-in swiching circuit on-off control. When use built-in switching circuit, this pin must be fixed to V <sub>CC</sub> .<br>If built-in switching circuit is not used, this pin must be fixed to GND     |  |
| RESET  | 263                                   | MPU or V <sub>CC</sub>                            | Input                   | Setting this pin to GND sets initializes the alternating signal (M signal) circuit. A V <sub>CC</sub> level RESET is normally used.  |  |
| DISPOFF  | 253                                   | MPU   | Input                   | Setting this pin to GND sets LCD drive output X1 to X240 to the VM level.  |  |
| M/S  | 247                                   | —   | Input                   | Controls the display-off function, and display-off signal output from $\overline{\text{DOC}}$ pin.   |  |
|  |                                       |   |                         |  | <b>M/S    DISPOFF pin state and functions</b>                      |
|  |                                       |   |                         |  | "H" level    When DISPOFF is Low level, X1-240 set VM level        |
|  |                                       |   |                         |  | "L" level    Until serial data input 16 times X1-X240 set VM level |
| $\overline{\text{DOC}}$  | 254                                   | —   | Output                  | <b>M/S    <math>\overline{\text{DOC}}</math></b>   |  |
|  |                                       |   |                         | "H" level    When $\overline{\text{DISPOFF}}$ is Low level, output low level<br>When $\overline{\text{DISPOFF}}$ is High level, output High level  |  |
|  |                                       |   |                         | "L" level    Until serial data input 16 times output low level from $\overline{\text{DOC}}$ pin  |  |
|  |                                       |   |                         |    |  |
|  |                                       |   |                         |  |  |
| When using M/S is low level, $\overline{\text{DOC}}$ pin should be connect to SEG LSI Dispoff control pin. |                                       |   |                         |  |  |

Pin Functions (cont)

| Classification   | Symbol     | Pin No.  | Connected to             | I/O    | Function   |     |       |       |                 |     |  |  |             |       |     |     |                         |  |     |     |                          |  |     |     |                          |     |  |  |            |       |     |     |                         |  |     |     |                          |  |     |     |                          |
|------------------|------------|----------|--------------------------|--------|--|-----|-------|-------|-----------------|-----|--|--|-------------|-------|-----|-----|-------------------------|--|-----|-----|--------------------------|--|-----|-----|--------------------------|-----|--|--|------------|-------|-----|-----|-------------------------|--|-----|-----|--------------------------|--|-----|-----|--------------------------|
| Control signal   | SHL        | 251      | —                        | Input  | <div>This pin switches shift directions.</div> <table><tr><th>SHL</th><th>MODE0</th><th>MODE1</th><th>Shift direction</th></tr><tr><td>"H"</td><td></td><td></td><td>Right shift</td></tr><tr><td>level</td><td>"H"</td><td>"H"</td><td>DIO2→SR1.....SR240→DIO1</td></tr><tr><td></td><td>"H"</td><td>"L"</td><td>DIO2→SR21.....SR220→DIO1</td></tr><tr><td></td><td>"L"</td><td>"H"</td><td>DIO2→SR41.....SR200→DIO1</td></tr><tr><td>"L"</td><td></td><td></td><td>Left shift</td></tr><tr><td>level</td><td>"H"</td><td>"H"</td><td>DIO1→SR240.....SR1→DIO2</td></tr><tr><td></td><td>"H"</td><td>"L"</td><td>DIO1→SR220.....SR21→DIO2</td></tr><tr><td></td><td>"L"</td><td>"H"</td><td>DIO1→SR200.....SR41→DIO2</td></tr></table> <div>SR1, SR2...SR240 correspond to X1, X2...X240.</div> <div>Note: The 40 or 80 pins invalidated at the 200-output or 160-output mode output the non-selected level synchronized every time; release these pins.</div> | SHL | MODE0 | MODE1 | Shift direction | "H" |  |  | Right shift | level | "H" | "H" | DIO2→SR1.....SR240→DIO1 |  | "H" | "L" | DIO2→SR21.....SR220→DIO1 |  | "L" | "H" | DIO2→SR41.....SR200→DIO1 | "L" |  |  | Left shift | level | "H" | "H" | DIO1→SR240.....SR1→DIO2 |  | "H" | "L" | DIO1→SR220.....SR21→DIO2 |  | "L" | "H" | DIO1→SR200.....SR41→DIO2 |
| SHL              | MODE0      | MODE1    | Shift direction          |        |  |     |       |       |                 |     |  |  |             |       |     |     |                         |  |     |     |                          |  |     |     |                          |     |  |  |            |       |     |     |                         |  |     |     |                          |  |     |     |                          |
| "H"              |            |          | Right shift              |        |  |     |       |       |                 |     |  |  |             |       |     |     |                         |  |     |     |                          |  |     |     |                          |     |  |  |            |       |     |     |                         |  |     |     |                          |  |     |     |                          |
| level            | "H"        | "H"      | DIO2→SR1.....SR240→DIO1  |        |  |     |       |       |                 |     |  |  |             |       |     |     |                         |  |     |     |                          |  |     |     |                          |     |  |  |            |       |     |     |                         |  |     |     |                          |  |     |     |                          |
|                  | "H"        | "L"      | DIO2→SR21.....SR220→DIO1 |        |  |     |       |       |                 |     |  |  |             |       |     |     |                         |  |     |     |                          |  |     |     |                          |     |  |  |            |       |     |     |                         |  |     |     |                          |  |     |     |                          |
|                  | "L"        | "H"      | DIO2→SR41.....SR200→DIO1 |        |  |     |       |       |                 |     |  |  |             |       |     |     |                         |  |     |     |                          |  |     |     |                          |     |  |  |            |       |     |     |                         |  |     |     |                          |  |     |     |                          |
| "L"              |            |          | Left shift               |        |  |     |       |       |                 |     |  |  |             |       |     |     |                         |  |     |     |                          |  |     |     |                          |     |  |  |            |       |     |     |                         |  |     |     |                          |  |     |     |                          |
| level            | "H"        | "H"      | DIO1→SR240.....SR1→DIO2  |        |  |     |       |       |                 |     |  |  |             |       |     |     |                         |  |     |     |                          |  |     |     |                          |     |  |  |            |       |     |     |                         |  |     |     |                          |  |     |     |                          |
|                  | "H"        | "L"      | DIO1→SR220.....SR21→DIO2 |        |  |     |       |       |                 |     |  |  |             |       |     |     |                         |  |     |     |                          |  |     |     |                          |     |  |  |            |       |     |     |                         |  |     |     |                          |  |     |     |                          |
|                  | "L"        | "H"      | DIO1→SR200.....SR41→DIO2 |        |  |     |       |       |                 |     |  |  |             |       |     |     |                         |  |     |     |                          |  |     |     |                          |     |  |  |            |       |     |     |                         |  |     |     |                          |  |     |     |                          |
| LCD drive output | X1 to X240 | 1 to 240 | LCD                      | Output | <div>LCD drive output</div> <div>By a combination of the display data and the M signal, when <math>\overline{\text{DISPOFF}}</math> is set to <math>V_{\text{CC}}</math>, either VH, VL, or VM is selected and transmitted to the output circuit.</div> <div></div>  |     |       |       |                 |     |  |  |             |       |     |     |                         |  |     |     |                          |  |     |     |                          |     |  |  |            |       |     |     |                         |  |     |     |                          |  |     |     |                          |

Note: Configuring the LCD panel using the HD66137 when using the select SEGMENT driver.

The Select SEGMENT driver

| SEGMENT driver     | Select |
|--------------------|--------|
| HD66130 (320 OUT)  | ○      |
| HD66132 (240 OUT)  | ×      |
| HD66134S (240 OUT) | ○      |
| HD66136 (400 OUT)  | ○      |

## Application Example

### Application Example (1)

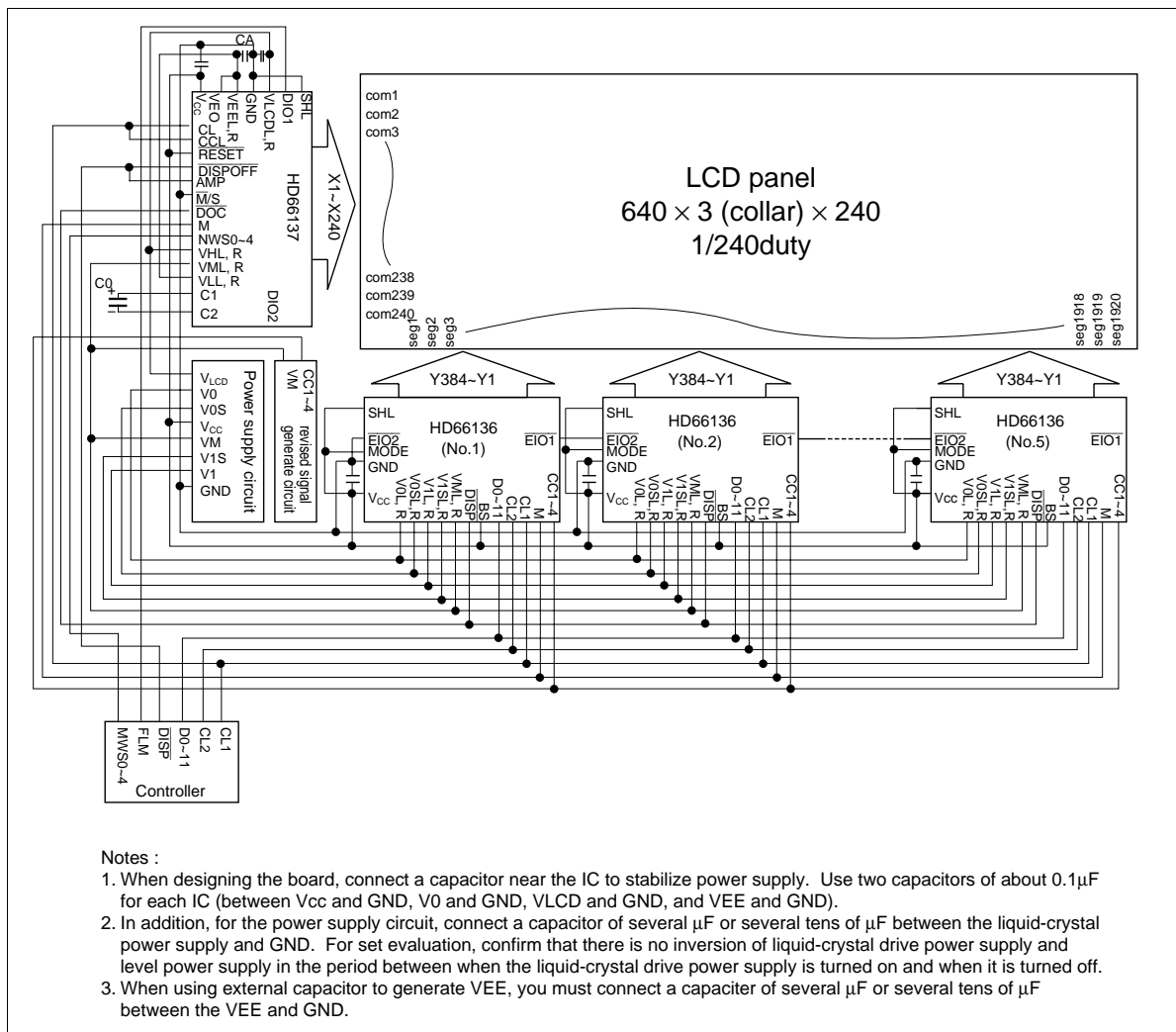
Figure 1 shows an application example  $640 \times 3$  (collar)  $\times 240$  dot Half VGA Size STN color panel.

This panel configured HD66137  $\times$  1 piece and HD66136  $\times$  5 pieces.

HD66137 generates M signal and DOC signal. M signal pin is connected M signal pin of HD66136 and DOC signal pin is connected DISP signal pin of HD66136.

HD66137 is able to generate voltage by external capacitor.

VEO pin is connected VEE pin and VL pin.



### Figure 1 Application Example (1)



## Application Example (2)

Figure 2 shows an application example  $320 \times 3$  (collar)  $\times 240$  dot Quarter VGA Size STN color panel.

This panel configured HD66137  $\times 1$  piece and HD66130  $\times 3$  pieces.

HD66137 generates M signal and DOC signal. M signal pin is connected M signal pin of HD66130 and DOC signal pin is connected DISP signal pin of HD66136.

HD66137 is able to generate - voltage by external capacitor.

VEO pin is connected VEE pin and VL pin.

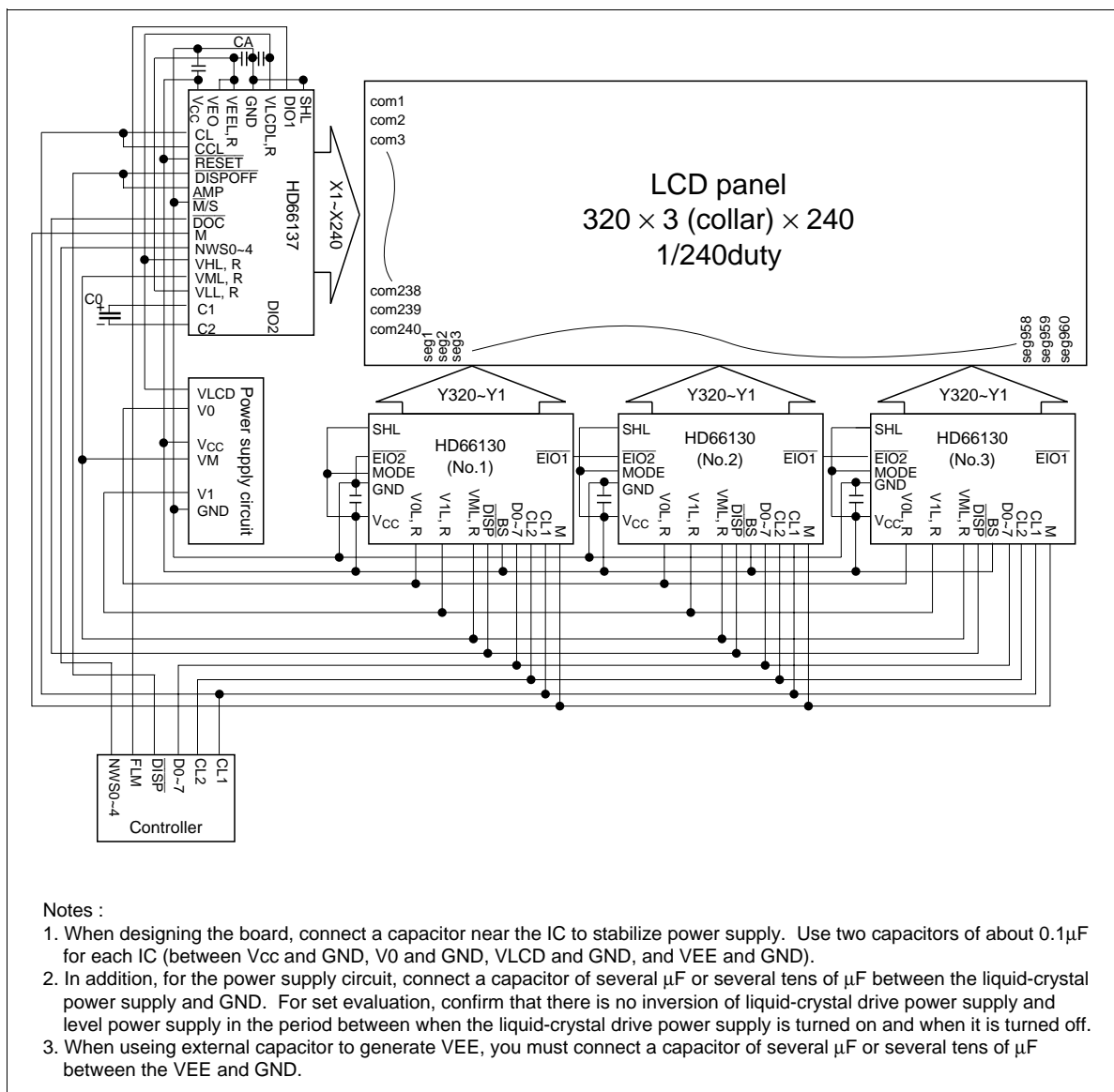


Figure 2 Application Example (2)

Power Supply Circuit Example

Figure 3 shows a power supply circuit example.

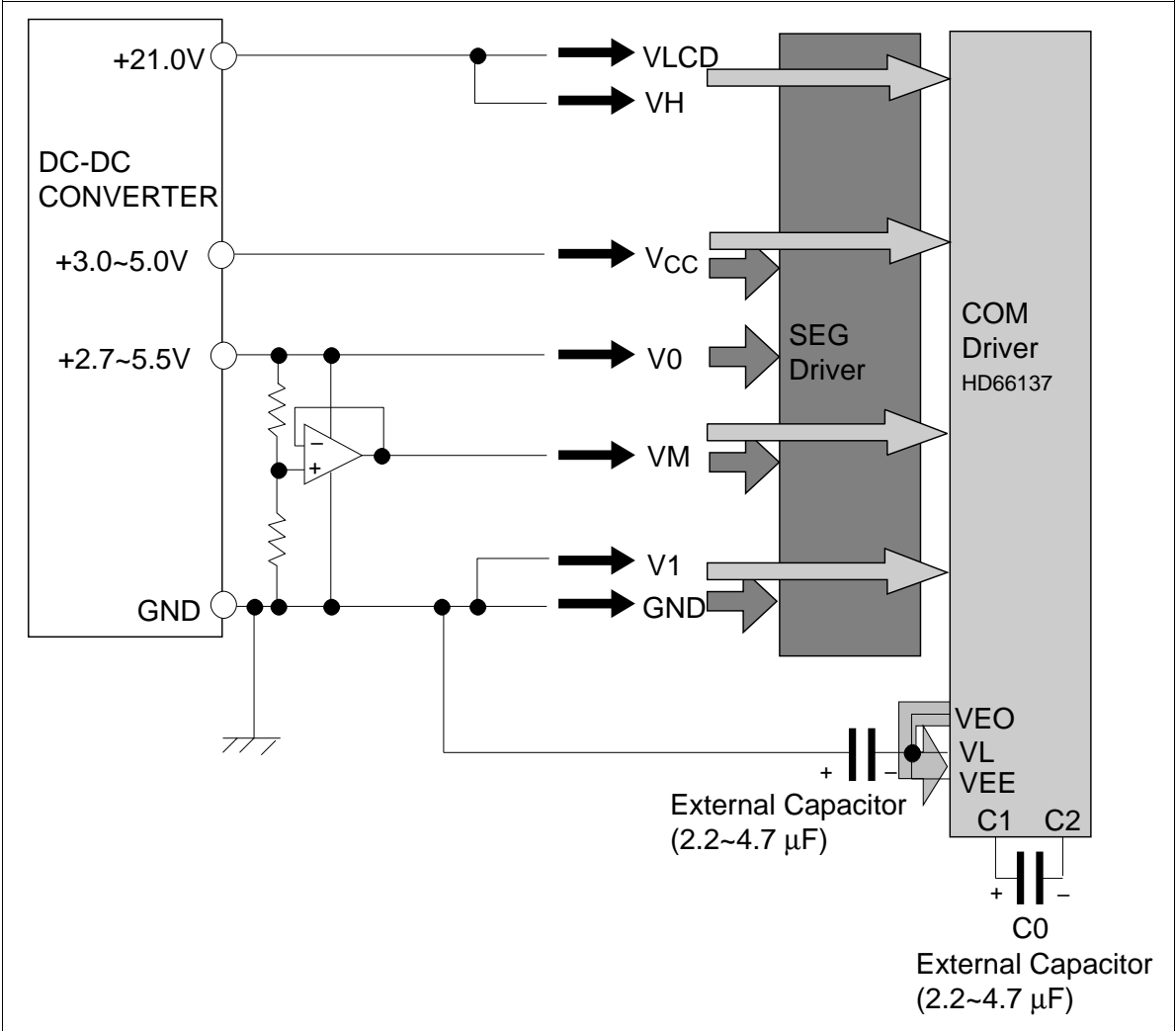


Figure 3 Power Supply Circuit Example

## Absolute Maximum Rating

| Item                  |                   | Symbol    | Ratings                | Unit | Notes   |
|-----------------------|-------------------|-----------|------------------------|------|---------|
| Power supply voltage  | Logic circuit     | $V_{CC}$  | -0.3 to +7.0           | V    | 1, 8    |
|                       | LCD drive circuit | $V_{LCD}$ | -0.3 to +25.0          | V    | 1, 3, 8 |
|                       |                   | $V_{EE}$  | -20.0 to +0.3          | V    | 1, 4, 8 |
| Input voltage (1)     |                   | VT1       | -0.3 to $V_{CC} + 0.3$ | V    | 1, 2    |
| Input voltage (2)     |                   | VH        | -0.3 to $V_{LCD}$      | V    | 1, 5, 8 |
| Input voltage (3)     |                   | VL        | +0.3 to $V_{EE}$       | V    | 1, 6, 8 |
| Input voltage (4)     |                   | VM        | -0.3 to + 5.0          | V    | 1, 7, 8 |
| Operating temperature |                   | Topr      | -30 to +75             | °C   |         |
| Storage temperature   |                   | Tstg      | -55 to +110            | °C   |         |

Notes: 1. Voltage from GND.

2. Applicable to DIO1,  $\overline{DISPOFF}$ , SHL, M, NWS0, NWS1, NWS2, NWS3, NWS4,  $\overline{RESET}$ , MODE0, MODE1, CL,  $\overline{M/S}$ , AMP, CCL, DIO2.

3. Applicable to  $V_{LCDL}$ , R pins.

4. Applicable to  $V_{EEL}$ , R pins.

5. Applicable to  $V_{HL}$ , R pins.

6. Applicable to  $V_{LL}$ , R pins.

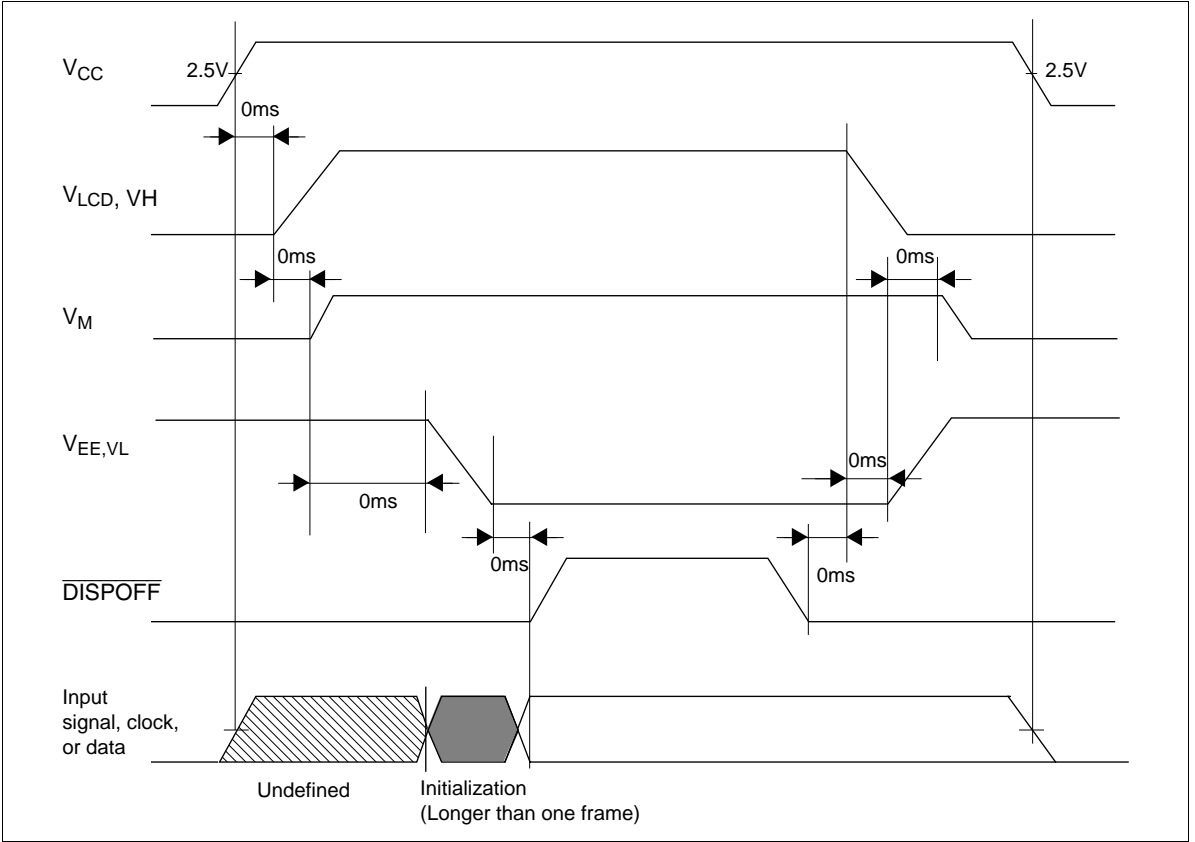
7. Applicable to  $V_{ML}$ , R pins.

(Caution)

Operating the LSI in excess of the absolute maximum rating will result in permanent damage. Use the LSI observing electrical characteristic conditions in normal operation. Exceeding the conditions will cause malfunctions or will affect LSI reliability.

8. Observe the sequence of activation and inactivation for the following power supplies and signals. And this sequence apply to use built - in switching circuit.

If the sequence is not observed, it may cause LSI malfunction, permanent damage, or adverse effects.



## 8.1 Power on

- Turn on the power supply in the order of GND-  $V_{CC}$ , GND-VLCD (VH), and VM. VM-VEE is generated automatically. In this case, input GND to the  $\overline{DISPOFF}$  pin.
- The LCD level forcibly outputs the VM level by the  $\overline{DISPOFF}$  function.
- The  $\overline{DISPOFF}$  function has a priority even if input signal distortion occurs immediately after  $V_{CC}$  input.
- Then input the predetermined signals to initialize the driver registers. In this case, assure a period for more than one frame.
- Preparation for normal display is thus completed. Cancel the  $\overline{DISPOFF}$  function by setting the  $\overline{DISPOFF}$  pin to  $V_{CC}$ . At this point, the levels of VEE (VL), VLCD (VH) and VM must have reached the predetermined respective voltage.

## 8.2 Shut down

As a rule, shut down in order opposite to that used for power on.

- Set the  $\overline{DISPOFF}$  pin to GND.
- At first shut off the LCD power supply GND-VLCD (VH), at same time GND-VEE (VL) get to VM. Next shut off the VM.
- Set  $V_{CC}$  and the input signal to GND.  
At this point, VEE (VL), VLCD (VH) and VM pin input must completely drop to 0 V.  
Since the  $\overline{DISPOFF}$  function is inactivated when the  $V_{CC}$  level drops to GND, the LCD output may output a level other than VM. Therefore, an incorrect display may appear at shut down or power on.

## Electrical Characteristics

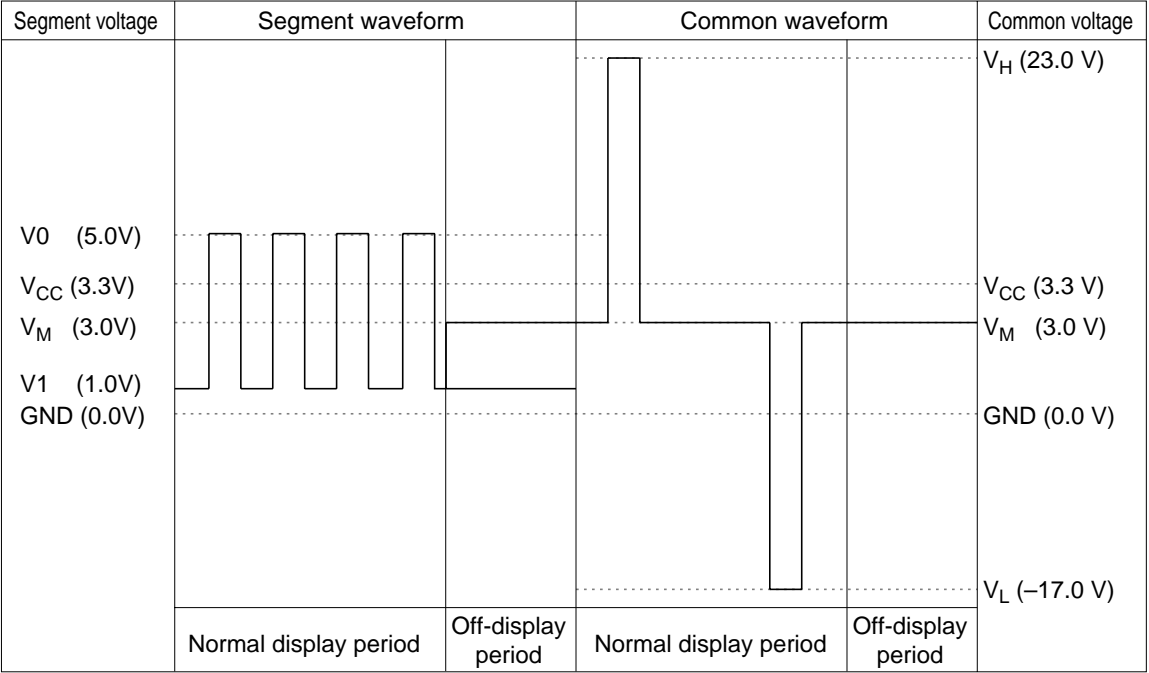
DC Characteristics ( $V_{CC} = 2.5$  to  $5.5$  V,  $GND = 0$  V,  $V_{LCD} - V_{EE} = 15$  to  $43$  V,  $T_a = -30$  to  $+75$  °C)

| Item                              | Symbol    | Applicable Pins   | Min.                | Typ. | Max.                | Unit       | Measurement Conditions   | Notes |
|-----------------------------------|-----------|---|---------------------|------|---------------------|------------|--|-------|
| Input high-level voltage          | $V_{IH}$  | DIO1, $\overline{DISPOFF}$ ,<br>SHL, M, $\overline{M/S}$ ,<br>MWS0-4, $\overline{RESET}$ ,  | $0.7 \times V_{CC}$ | —    | $V_{CC}$            | V          |  |       |
| Input low-level voltage           | $V_{IL}$  | CL, MODE0,<br>MODE1, $\overline{DOC}$ ,<br>AMP, CCL, DIO2   | 0                   | —    | $0.3 \times V_{CC}$ | V          |  |       |
| Output high-level voltage         | $V_{OH}$  | M, $\overline{DOC}$ , DIO1,<br>DIO2   | $V_{CC} - 0.4$      | —    | —                   | V          | $I_{OH} = -0.4$ mA   |       |
| Output low-level voltage          | $V_{OL}$  | M, $\overline{DOC}$ , DIO1,<br>DIO2   | —                   | —    | 0.4                 | V          | $I_{OL} = 0.4$ mA  |       |
| ON resistance between $V_i - Y_j$ | $R_{ON}$  | X1 to X240, V pin   | —                   | 0.7  | 2.0                 | k $\Omega$ | $I_{ON} = 150$ $\mu$ A   | 1     |
| Input leak current (1)            | $I_{IL1}$ | DIO1, $\overline{DISPOFF}$ ,<br>SHL, M, $\overline{M/S}$ ,<br>MWS0-4, $\overline{RESET}$ ,<br>CL, MODE0,<br>MODE1, $\overline{DOC}$ ,<br>AMP, CCL, DIO2 | -5                  | —    | 5                   | $\mu$ A    | $V_{IN} = V_{CC}$ to GND   |       |
| Input leak current (2)            | $I_{IL2}$ | VH, VL, VM, C1,<br>C2   | -25                 | —    | 25                  | $\mu$ A    |  |       |
| Current consumption (1)           | $I_{CC1}$ | $V_{CC}$  | —                   | 10   | 40                  | $\mu$ A    | $V_{CC} = 3.3$ V,<br>$V_{LCD} - V_{EE} = 40$ V,<br>$f_{CL} = 19.2$ kHz,<br>$f_M = 1.5$ kHz | 2     |
| Current consumption (2)           | $I_{CC2}$ | $V_{CC}$  | —                   | 20   | 50                  | $\mu$ A    | $V_{CC} = 5.0$ V,<br>$V_{LCD} - V_{EE} = 40$ V,<br>$f_{CL} = 19.2$ kHz,<br>$f_M = 1.5$ kHz |       |
| Current consumption (3)           | $I_{LCD}$ | $V_{LCD}$   | —                   | 25   | 50                  | $\mu$ A    | $V_{CC} = 3.3$ V,<br>$V_{LCD} - V_{EE} = 40$ V,<br>$f_{CL} = 19.2$ kHz,<br>$f_M = 1.5$ kHz |       |

Notes: 1. This is a resistance value between the X and V pins (either of VH, VL, or VM) when a load current is applied to one of x1 to x240 pins. These values are regulated under the conditions of  $V_{LCD} = V_H = 21.75$  V,  $V_{EE} = V_L = -18.5$  V,  $V_M = 1.75$  V,  $GND = 0$  V, Use VH, VL, and VM in the range of  $V_{LCD} - V_M \geq V_H - V_M = 21.5$  to  $7.5$  V,  $V_{EE} - V_M \leq V_L - V_M = -21.5$  to  $-7.5$  V, with the relation of  $V_H > V_M > V_L$ .

2. The current applied between the input and output is excluded. When an input to a CMOS gate is at an intermediate level, through current flows between the power supplies, and the power supply current increases. Therefore, use  $V_{IH} = V_{CC}$  and  $V_{IL} = GND$ .

3. The voltage relationship of each signal is as follows :



AC Characteristics (1) ( $V_{CC} = 2.5$  to  $5.5$  V,  $GND = 0$  V,  $V_{LCD}-V_{EE} = 15$  to  $43$  V,  $T_a = -30$  to  $+75$  °C)

| Item                   | Symbol            | Pin Name                                | min. | max. | Dimensions | Note |
|------------------------|-------------------|---|------|------|------------|------|
| Clock cycle time       | t <sub>CYC</sub>  | CL                                      | 400  | —    | ns         |      |
| CL high-level width    | t <sub>CWH</sub>  | CL                                      | 25   | —    | ns         |      |
| CL low-level width     | t <sub>CWL</sub>  | CL                                      | 370  | —    | ns         |      |
| CL rising time         | t <sub>r</sub>    | CL                                      | —    | 30   | ns         |      |
| CL falling time        | t <sub>f</sub>    | CL                                      | —    | 30   | ns         |      |
| Data set-up time       | t <sub>DS</sub>   | DIO1, DIO2, CL                          | 100  | —    | ns         |      |
| Data hold time         | t <sub>DH</sub>   | DIO1, DIO2, CL                          | 10   | —    | ns         |      |
| Data output delay time | t <sub>DD</sub>   | DIO1, DIO2, CL                          | —    | 200  | ns         | 1    |
| M output delay time    | t <sub>MD</sub>   | M, CL                                   | —    | 200  | ns         | 1    |
| M set-up time          | t <sub>MS</sub>   | M, CL                                   | 20   | —    | ns         |      |
| M Hold time            | t <sub>MH</sub>   | M, CL                                   | 20   | —    | ns         |      |
| DOC delay time 1       | t <sub>DOC1</sub> | $\overline{DISPOFF}$ , $\overline{DOC}$ | —    | 300  | ns         | 2    |
| DOC delay time 2       | t <sub>DOC2</sub> | DIO1, DIO2, $\overline{DOC}$            | —    | 300  | ns         | 2    |

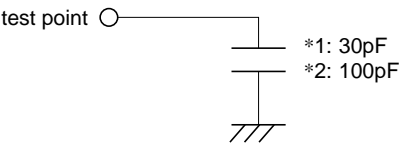
AC Characteristics (2) ( $V_{CC} = 2.5$  to  $4.5$  V,  $GND = 0$  V,  $V_{LCD}-V_{EE} = 43$  V,  $T_a = -30$  to  $+75$  °C)

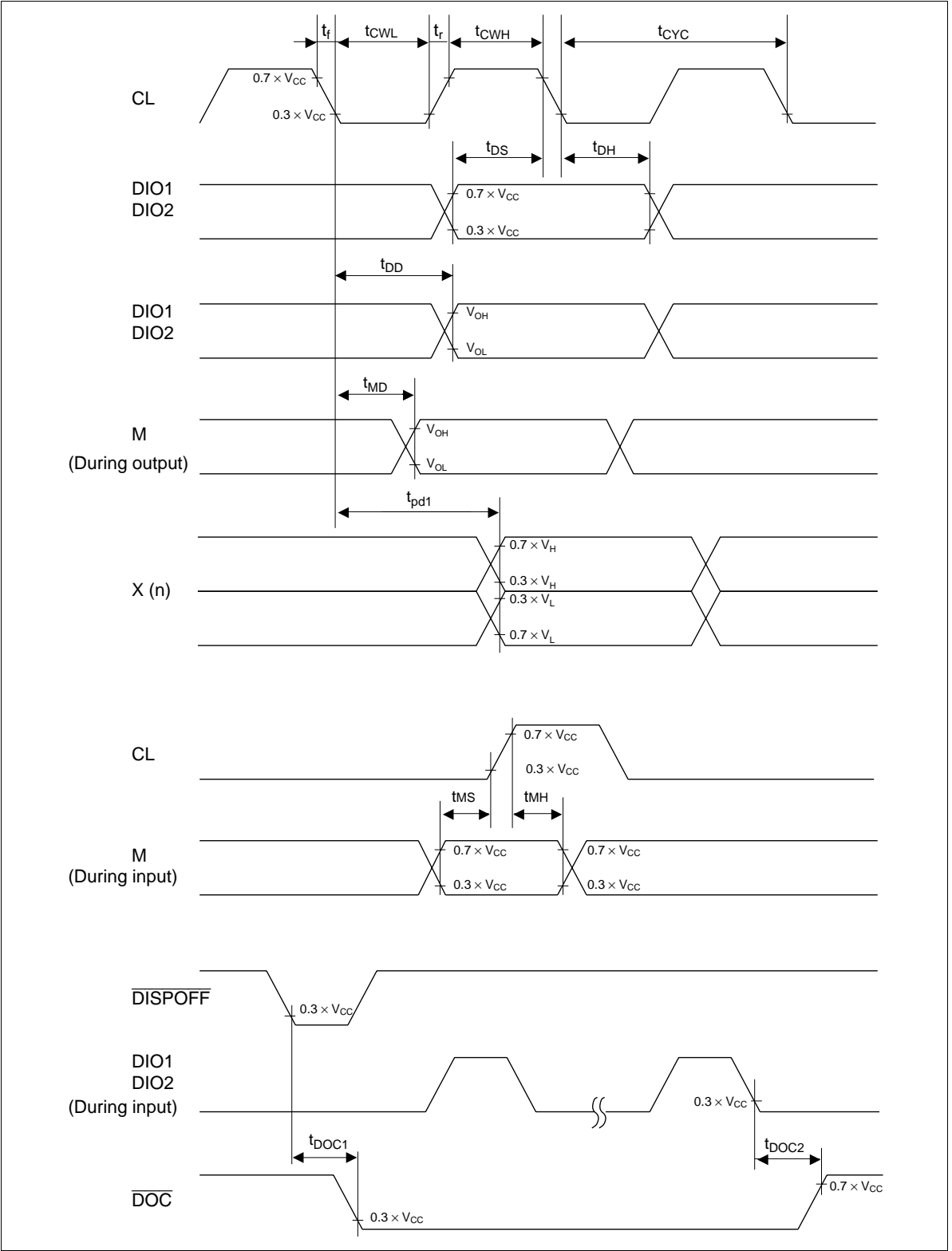
| Item               | Symbol    | Pin Name | min. | max. | Dimensions | Note |
|--------------------|-----------|----------|------|------|------------|------|
| Output delay time1 | $t_{pd1}$ | X(n), M  | —    | 1.2  | $\mu$ s    | 2    |

AC Characteristics (3) ( $V_{CC} = 4.5$  to  $5.5$  V,  $GND = 0$  V,  $V_{LCD}-V_{EE} = 43$  V,  $T_a = -30$  to  $+75$  °C)

| Item               | Symbol    | Pin Name | min. | max. | Dimensions | Note |
|--------------------|-----------|----------|------|------|------------|------|
| Output delay time1 | $t_{pd1}$ | X(n), M  | —    | 0.7  | $\mu$ s    | 2    |

\*1, \*2. The following timing is regulated with the circuit at the right connected.

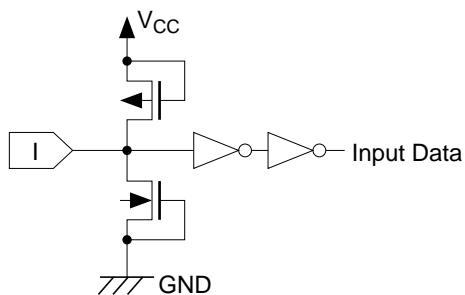






## Terminal Configuration

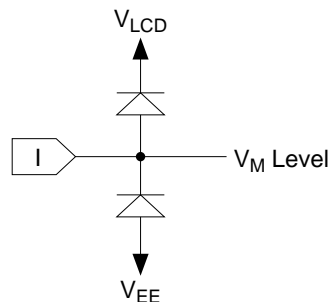
### Terminal Configuration (1)



Input Terminal 1

Applicable terminals :

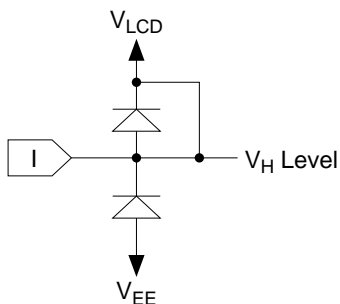
CL, CCL, SHL, MODE0,1, AMP  
DISPOFF, RESET, MWS0~4,  $\bar{M}/S$



Input Terminal 2

Applicable terminals :  $V_{MR, L}$

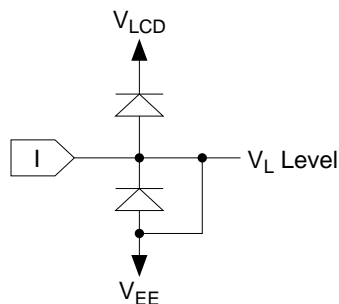
\*  $V_{MR}$  terminal connect with  $V_{ML}$  terminal in LSI.



Input Terminal 3

Applicable terminals :  $V_{HR, L}$

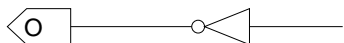
\*  $V_{HR}$  terminal connect with  $V_{HL}$  terminal in LSI.



Input Terminal 4

Applicable terminals :  $V_{LR, L}$

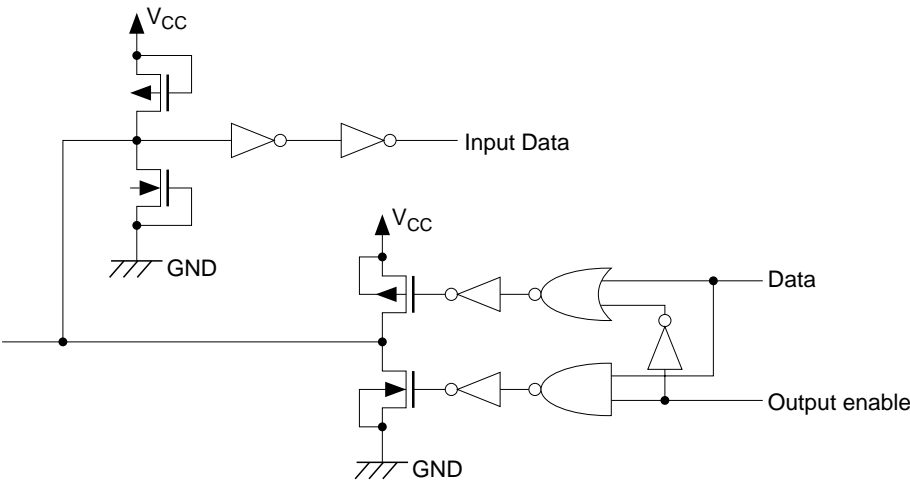
\*  $V_{LR}$  terminal connect with  $V_{LL}$  terminal in SLI.



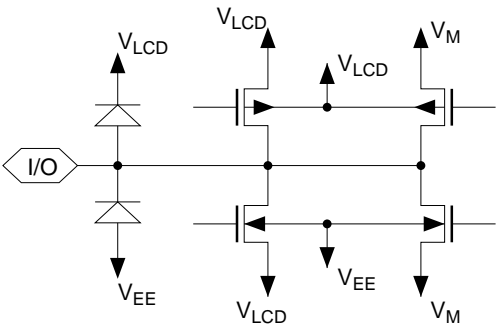
Output Terminal 1

Applicable terminals :  $\overline{DOC}$

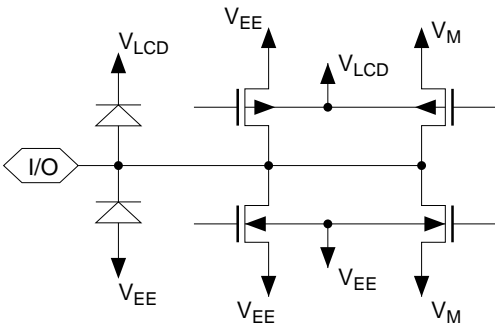
Terminal Configuration (2)



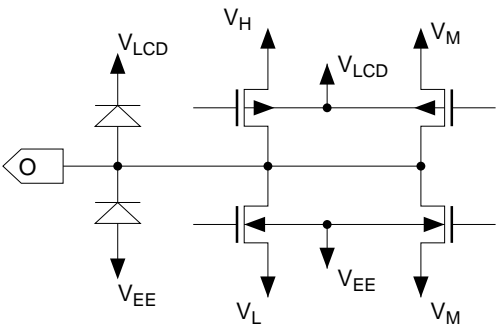
I/O Terminal 1  
Applicable terminals : DIO1, DIO2, M,



I/O Terminal 2  
Applicable terminals : C1



I/O Terminal 3  
Applicable terminals : C2



LCD drive Output Terminal  
Applicable terminals : X1 to X240

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