

TTL HD74/HD74S Series

■ PERFORMANCE(per gate)

| Performance | HD74 Series | HD74S Series |
|------------------------|-------------|--------------|
| Propagation Delay Time | 10 ns | 3 ns |
| Power Dissipation | 10 mW | 20 mW |
| Speed-Power Product | 100 pJ | 60 pJ |

■ MAIN CHARACTERISTICS($T_a = -20 \sim +75^\circ\text{C}$)

| Parameter | Series | | HD74S Series | |
|------------------------------------|--------|------------------|--------------|------------------|
| | min. | max. | min. | max. |
| $V_{OL}(I_{OL} \text{ max})$ | — | 0.4V | — | 0.5V |
| $V_{OH}(I_{OH} = -400\mu\text{A})$ | 2.4V | — | 2.7V | — |
| V_{IL} | — | 0.8V | — | 0.8V |
| V_{IH} | 2V | — | 2V | — |
| I_{IL} | — | -1.6mA | — | -2mA |
| $I_{IH}(V_{IH} \text{ min})$ | — | 40 μA | — | 50 μA |

■ SELECTION GUIDE

● NAND/NOR/AND/OR GATES

| Function | HD74Series | HD74S Series |
|--|------------|--------------|
| Quad. 2-input Positive NAND Gates | 00 ✓ | 00 ✓ |
| Quad. 2-input Positive NAND Gates (with Open Collector Output) | 01 ✓ | — |
| Quad. 2-input Positive NOR Gates | 02 ✓ | 02 ✓ |
| Quad. Positive NAND Gates (with Open Collector Output) | 03 ✓ | 03 ✓ |
| Hex Inverters | 04 ✓ | 04 ✓ |
| Hex Inverters (with Open Collector Output) | 05 ✓ | 05 ✓ |
| Hex Inverter Buffers/Drivers (with Open Collector High-voltage Output) | 06 ✓ | — |
| Hex Buffers/Drivers (with Open Collector High-voltage Output) | 07 ✓ | — |
| Quad. 2-input Positive AND Gates | 08 ✓ | — |
| Quad. 2-input Positive AND Gates (with Open Collector Output) | 09 ✓ | — |
| Triple 3-input Positive NAND Gates | 10 ✓ | 10 ✓ |
| Triple 3-input Positive AND Gates | — | 11 ✓ |
| Triple 3-input Positive NAND Gates (with Open Collector Output) | 12 ✓ | 12 ✓ |
| Dual 4-input Schmitt NAND Gates | 13 ✓ | — |
| Hex Schmitt-trigger Inverters | 14 ✓ | — |
| Triple 3-input Positive AND Gates (with Open Collector Output) | — | 15 ✓ |
| Hex Inverter Buffers/Drivers (with Open Collector High-voltage Output) | 16 ✓ | — |
| Hex Buffers/Drivers (with Open Collector High-voltage Output) | 17 ✓ | — |
| Dual 4-input Positive NAND Gates | 20 ✓ | 20 ✓ |
| Dual 4-input Positive NAND Gates (with Open Collector Output) | 22 ✓ | 22 ✓ |
| Expandable Dual 4-input Positive NOR Gates (with Strobe) | 23 ✓ | — |
| Dual 4-input Positive NOR Gates | 25 ✓ | — |
| Quad. 2-input High-voltage Interface NAND Gates | 26 ✓ | — |
| Triple 3-input Positive NOR Gates | 27 ✓ | — |
| 8-input Positive NAND Gate | 30 ✓ | — |
| Quad. 2-input Positive OR Gates | 32 ✓ | — |
| Quad. 2-input Positive NAND Buffers | 37 ✓ | — |
| Quad. 2-input Positive NAND Buffers (with Open Collector Output) | 38 ✓ | — |
| Dual 4-input Positive NAND Buffers | 40 ✓ | 40 ✓ |
| Quad. Bus Buffer Gates with 3-state Output (Inverting) | 125 ✓ | — |
| Quad. Bus Buffer Gates with 3-state Output (Noninverting) | 126 ✓ | — |
| Quad. 2-input Positive NAND Schmitt Triggers | 132 ✓ | — |
| 13-input Positive NAND Gate | — | 133 ✓ |
| 12-input Positive NAND Gate (with 3-state Out.) | — | 134 ✓ |
| Dual 4-input Positive NAND Line Drivers | — | 140 ✓ |

(to be continued)

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● AND-OR-INVERT GATES

| Function | HD74 Series | HD74S Series |
|---|-------------|--------------|
| Expandable Dual 2-wide 2-input AND-OR-INVERT Gates | 50 ✓ | — |
| Dual 2-wide 2-input AND-OR-INVERT Gates | 51 ✓ | — |
| Expandable 4-wide 2-input AND-OR-INVERT Gate | 53 ✓ | — |
| 4-wide 2-input AND-OR-INVERT Gate | 54 | — |
| 4-2-3-2-input AND-OR-INVERT Gate | — | 64 ✓ |
| 4-2-3-2-input AND-OR-INVERT Gate (with Open Collector Output) | — | 65 ✓ |

● EXPANDER

| Function | HD74 Series | HD74S Series |
|------------------------|-------------|--------------|
| Dual 4-input Expanders | 60 ✓ | — |

● FLIP FLOPS

| Function | HD74 Series | HD74S Series |
|--|-------------|--------------|
| J-K Master-Flip Flop (AND Inputs) | 72 | — |
| Dual J-K Flip Flops | 73 | — |
| Dual D-type Edge-triggered Flip Flops | 74 ✓ | 74 |
| Dual J-K Flip Flops (with PR and CLR) | 76 | — |
| Dual J-K Flip Flops | 107 ✓ | — |
| Dual J-K Negative-edge-triggered Flip Flops (with PR and CLR) | — | 112 ✓ |
| Dual J-K Negative-edge-triggered Flip Flops (with PR) | — | 113 ✓ |
| Dual J-K Negative-edge-triggered Flip Flops (with PR, Common CLR, and Common CK) | — | 114 |
| Monostable Multivibrator | 121 ✓ | — |
| Dual Retriggerable Monostable Multivibrators | 123 | — |
| Hex D-type Flip Flops (with CLR) | 174 | 174 ✓ |
| Quad. D-type Flip Flops (with CLR) | 175 | 175 ✓ |
| Dual Monostable Multivibrators (with Schmitt Trigger) | 221 | — |

● COUNTERS

| Function | HD74 Series | HD74S Series |
|--|-------------|--------------|
| Decade Counter | 90A ✓ | — |
| Divide-by-Twelve Counter | 92A | — |
| 4-bit Binary Counter | 93A | — |
| Presetable Decade Counter/Latch | 176 | — |
| 4-bit Binary Counter/Latch | 177 | — |
| Synchronous Decade Counter | 160 | — |
| Synchronous 4-bit Binary Counter | 161 | — |
| Fully Synchronous Decade Counter | 162 | — |
| Fully Synchronous 4-bit Binary Counter | 163 | — |
| Synchronous Decade Decimal Rate Multiplier | 167 ✓ | — |
| Synchronous Decade Up/Down Counter | 190 ✓ | — |
| Synchronous 4-bit Binary Up/Down Counter | 191 ✓ | — |
| Synchronous Decade Up/Down Counter | 192 ✓ | — |
| Synchronous 4-bit Binary Up/Down Counter | 193 ✓ | — |
| Decade Counter | 290 ✓ | — |
| 4-bit Binary Counter | 293 ✓ | — |

(to be continued)

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● 4-BIT, 5-BIT SHIFT/STORAGE REGISTERS

| Function | HD74 Series | HD74S Series |
|---|-------------|--------------|
| 4-bit Right-shift, Left-shift Register | 95A ✓ | — |
| 5-bit Shift Register (Dual Parallel-in, Parallel-out) | 96 ✓ | — |
| 4-bit D-type Register (with 3-state Output) | 173 ✓ | — |
| 4-bit Parallel-in, Parallel-out Bidirectional Shift Register | 194 ✓ | — |
| 4-bit Parallel-in, Parallel-out Shift Register (J-K Inputs for First Stage) | 195 ✓ | — |

● 8-BIT SHIFT REGISTERS

| Function | HD74 Series | HD74S Series |
|---|-------------|--------------|
| 8-bit Shift Register | 91A ✓ | — |
| 8-bit Parallel-out Shift Register | 164 ✓ | — |
| Parallel-load 8-bit Shift Register | 166 ✓ | — |
| 8-bit Parallel-in, Parallel-out Bidirectional Shift Register | 198 ✓ | — |
| 8-bit Parallel-in, Parallel-out Shift Register (J-K Inputs for First Stage) | 199 ✓ | — |

● ENCODERS

| Function | HD74 Series | HD74S Series |
|------------------------------------|-------------|--------------|
| 10-line-to-4-line Priority Encoder | 147 ✓ | — |
| 8-line-to-3-line Priority Encoder | 148 ✓ | — |

● DECODERS/DEMULPLEXERS

| Function | HD74 Series | HD74S Series |
|--|-------------|--------------|
| BCD-to-Decimal Decoder | 42A ✓ | — |
| Excess 3-to-Decimal Decoder | 43A ✓ | — |
| Excess 3-Gray-to-Decimal Decoder | 44A ✓ | — |
| 4-line-to-16-line Decoder/Demultiplexer | 154 ✓ | — |
| Dual 2-line-to-4-line Decoders/Demultiplexers | 155 ✓ | — |
| Dual 2-line-to-4-line Decoders/Demultiplexers (with Open Collector Output) | 156 ✓ | — |
| 4-line-to-16-line Decoder/Demultiplexer (with Open Collector Output) | 159 ✓ | — |

● DECODERS/LAMP DRIVERS/BUFFERS

| Function | HD74 Series | HD74S Series |
|---|-------------|--------------|
| BCD-to-Decimal Decoder/Driver (with 30V Out.) | 45 ✓ | — |
| BCD-to-Decimal Decoder/Driver (with 15V Out.) | 145 ✓ | — |
| BCD-to-Seven Segment Decoder/Driver (with 30V Output) | 46A ✓ | — |
| BCD-to-Seven Segment Decoder/Driver (with 15V Output) | 47A ✓ | — |
| BCD-to-Decimal Decoder/Driver (with 60V Out.) | 141 ✓ | — |

● LATCHES

| Function | HD74 Series | HD74S Series |
|-------------------------------------|-------------|--------------|
| Quad. Bistable Latches | 75 ✓ | — |
| Quad. \bar{S} - \bar{R} Latches | 279 ✓ | — |

● RANDOM ACCESS MEMORIES (less than 256-bit)

| Function | HD74 Series | HD74S Series |
|---|-------------|--------------|
| 64-bit Random Access Memory (16w by 4b) | 89 ✓ | — |

(to be continued)

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● ARITHMETIC ELEMENTS

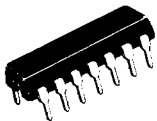
| Function | HD74 Series | HD74S Series |
|---|-------------|--------------|
| 4-bit Binary Full Adder | 83A ✓ | — |
| 4-bit Magnitude Comparator | 85 ✓ | — |
| Quad. 2-input Exclusive-OR Gates | 86 ✓ | 86 ✓ |
| Quad. Exclusive-OR/NOR Gates | — | 135 ✓ |
| Quad. 2-input Exclusive-OR Gates (with Open Collector Output) | 136 ✓ | — |
| 8-bit Odd/Even Parity Generator/Checker | 180 ✓ | — |
| 4-bit Arithmetic Logic Unit/Function Generator | — | 181 ✓ |
| Look-Ahead Carry Generator (for ALU) | 182 ✓ | 182 ✓ |
| Dual Carry Save Full Adders | H183 ✓ | — |
| 9-bit Odd/Even Parity Generator/Checker | — | 280 ✓ |
| 4-bit Binary Full Adder (with Fast Carry) | 283 ✓ | — |

● DATA SELECTORS/MULTIPLEXERS

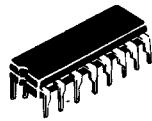
| Function | HD74 Series | HD74S Series |
|--|-------------|--------------|
| 16-bit Data Selector/Multiplexer | 150 ✓ | — |
| 8-bit Data Selector/Multiplexer (with Strobe) | 151A ✓ | 151 ✓ |
| 8-bit Data Selector/Multiplexer | — | — |
| Dual 4-line-to-1-line Data Selectors/Multiplexers | 153 ✓ | — |
| Quad. 2-line-to-1-line Data Selectors/Multiplexers | 157 ✓ | 157 ✓ |
| Quad. 2-line-to-1-line Data Selectors/Multiplexers | — | 158 ✓ |
| 8-bit Data Selector/Multiplexer (with Strobe and 3-state Output) | 251 ✓ | 251 ✓ |
| Quad. 2-line-to-1-line Data Selectors/Multiplexers (with 3-state Output) | — | 257 ✓ |
| Quad. 2-line-to-1-line Data Selectors/Multiplexers (with 3-state Output) | — | 258 ✓ |

■ OUTLINE

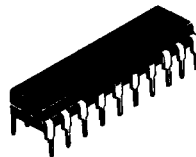
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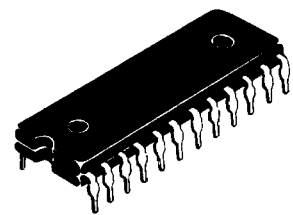
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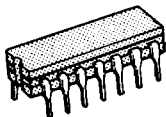
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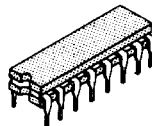
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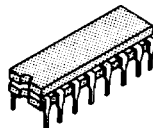
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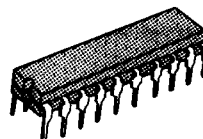
DG-16



DG-16A



DG-20



DG-24

