
HD74ALVCH162543

16-bit Registered Transceivers with 3-state Outputs

HITACHI

ADE-205-183 (Z)
Preliminary
1st. Edition
December 1996

Description

The HD74ALVCH162543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch enable ($\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$) and output enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control in either direction of data flow. The A to B enable ($\overline{\text{CEAB}}$) input must be low in order to enter data from A or to output data from B. If $\overline{\text{CEAB}}$ is low and $\overline{\text{LEAB}}$ is low, the A to B latches are transparent; a subsequent low to high transition of $\overline{\text{LEAB}}$ puts the A latches in the storage mode. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$. Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level. All outputs, which are designed to sink up to 12 mA, include 26 Ω resistors to reduce overshoot and undershoot.

Features

- $V_{\text{CC}} = 2.3 \text{ V}$ to 3.6 V
- Typical V_{OL} ground bounce $< 0.8 \text{ V}$ ($@V_{\text{CC}} = 3.3 \text{ V}$, $T_a = 25^\circ\text{C}$)
- Typical V_{OH} undershoot $> 2.0 \text{ V}$ ($@V_{\text{CC}} = 3.3 \text{ V}$, $T_a = 25^\circ\text{C}$)
- High output current $\pm 12 \text{ mA}$ ($@V_{\text{CC}} = 3.0 \text{ V}$)
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors
- All outputs have equivalent 26 Ω series resistors, so no external resistors are required.

Function Table ^{*2}

| Inputs | | | | Output B |
|--------|------|------|---|------------------------------|
| CEAB | LEAB | OEAB | A | |
| H | X | X | X | Z |
| X | X | H | X | Z |
| L | H | L | X | B ₀ ^{*1} |
| L | L | L | L | L |
| L | L | L | H | H |

H : High level

L : Low level

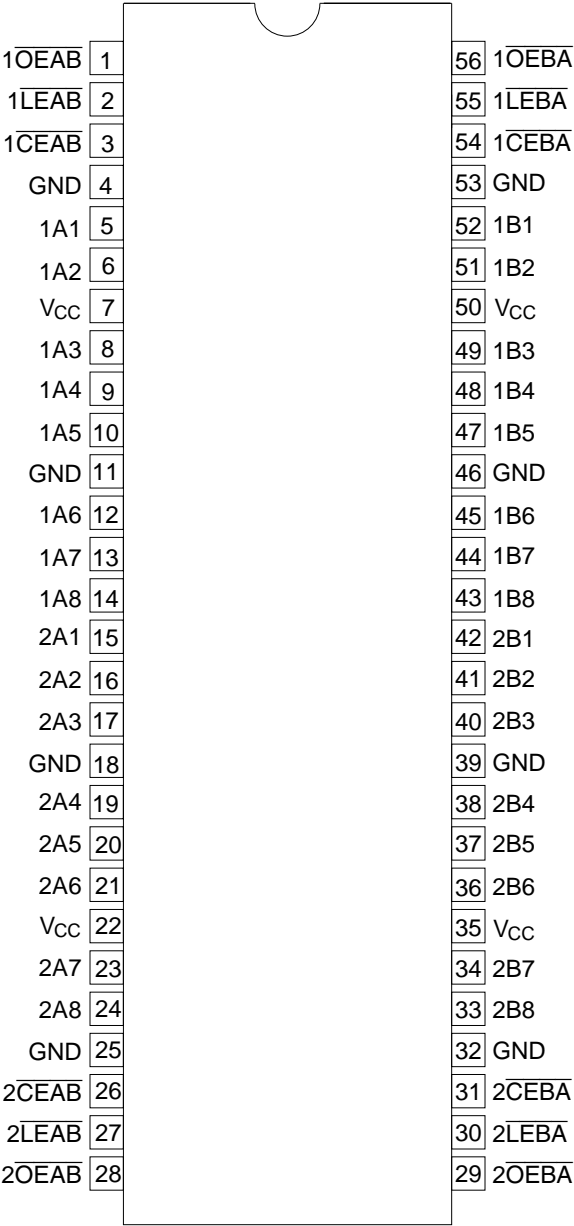
X : Immaterial

Z : High impedance

Notes: 1. Output level before the indicated steady state input conditions were established.

2. A to B data flow is shown; B to A flow control is the same except that it uses $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit | Conditions |
|--|-----------|---------------------------------------|------------------|-------------------------------|
| Supply voltage | V_{CC} | −0.5 to 4.6 | V | |
| Input voltage ^{*1, 2} | V_I | −0.5 to 4.6 −0.5 to $V_{CC} + 0.5$ | V | Except I/O ports I/O ports |
| Output voltage ^{*1, 2} | V_O | −0.5 to $V_{CC} + 0.5$ | V | |
| Input clamp current | I_{IK} | −50 | mA | |
| Output clamp current | I_{OK} | ±50 | mA | $V_O < 0$ or $V_O > V_{CC}$ |
| Continuous output current | I_O | ±50 ±100 | mA | $V_O = 0$ to V_{CC} |
| Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air) ^{*3} | P_T | 1 | W | TSSOP |
| Storage temperature | T_{stg} | −65 to 150 | $^\circ\text{C}$ | |

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

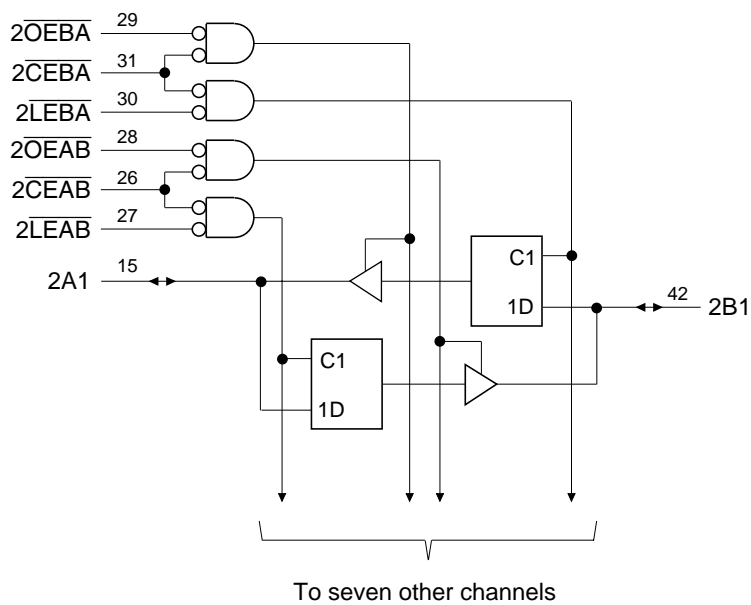
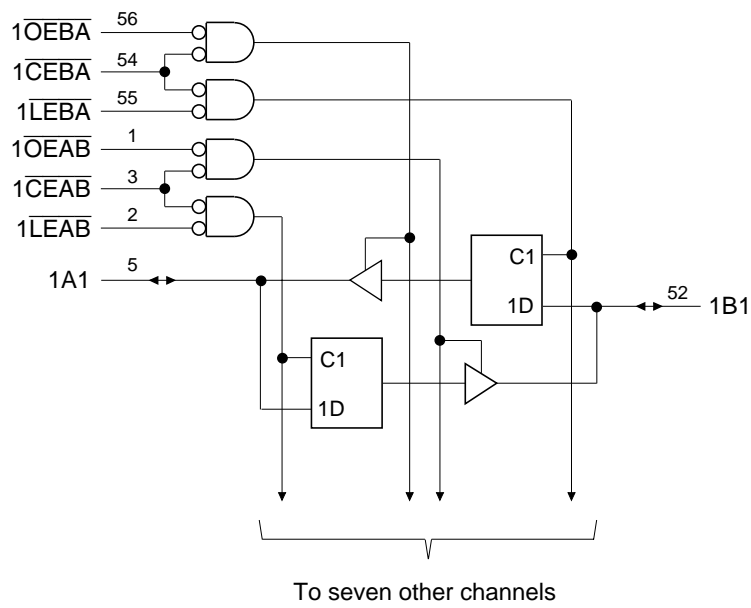
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Recommended Operating Conditions

| Item | Symbol | Min | Max | Unit | Conditions |
|------------------------------------|-----------------------|-----|-----------------|------------------|---|
| Supply voltage | V_{CC} | 2.3 | 3.6 | V | |
| Input voltage | V_I | 0 | V_{CC} | V | |
| Output voltage | V_O | 0 | V_{CC} | V | |
| High level output current | I_{OH} | — | −6 −8 −12 | mA | $V_{CC} = 2.3\text{ V}$ $V_{CC} = 2.7\text{ V}$ $V_{CC} = 3.0\text{ V}$ |
| Low level output current | I_{OL} | — | 6 8 12 | mA | $V_{CC} = 2.3\text{ V}$ $V_{CC} = 2.7\text{ V}$ $V_{CC} = 3.0\text{ V}$ |
| Input transition rise or fall rate | $\Delta t / \Delta v$ | 0 | 10 | ns / V | |
| Operating temperature | T_a | −40 | 85 | $^\circ\text{C}$ | |

Note: Unused control inputs must be held high or low to prevent them from floating.

Logic Diagram



Electrical Characteristics (Ta = -40 to 85°C)

| Item | Symbol | V _{CC} (V) ^{*1} | Min | Max | Unit | Test Conditions |
|--|------------------------|-----------------------------------|----------------------|------|------|--|
| Input voltage | V _{IH} | 2.3 to 2.7 | 1.7 | — | V | |
| | | 2.7 to 3.6 | 2.0 | — | | |
| | V _{IL} | 2.3 to 2.7 | — | 0.7 | | |
| | | 2.7 to 3.6 | — | 0.8 | | |
| Output voltage | V _{OH} | Min to Max | V _{CC} -0.2 | — | V | I _{OH} = -100 μA |
| | | 2.3 | 1.9 | — | | I _{OH} = -4 mA, V _{IH} = 1.7 V |
| | | 2.3 | 1.7 | — | | I _{OH} = -6 mA, V _{IH} = 1.7 V |
| | | 3.0 | 2.4 | — | | I _{OH} = -6 mA, V _{IH} = 2.0 V |
| | | 2.7 | 2.0 | — | | I _{OH} = -8 mA, V _{IH} = 2.0 V |
| | | 3.0 | 2.0 | — | | I _{OH} = -12 mA, V _{IH} = 2.0 V |
| | V _{OL} | Min to Max | — | 0.2 | | I _{OL} = 100 μA |
| | | 2.3 | — | 0.4 | | I _{OL} = 4 mA, V _{IL} = 0.7 V |
| | | 2.3 | — | 0.55 | | I _{OL} = 6 mA, V _{IL} = 0.7 V |
| | | 3.0 | — | 0.55 | | I _{OL} = 6 mA, V _{IL} = 0.8 V |
| | | 2.7 | — | 0.6 | | I _{OL} = 8 mA, V _{IL} = 0.8 V |
| | | 3.0 | — | 0.8 | | I _{OL} = 12 mA, V _{IL} = 0.8 V |
| Input current | I _{IN} | 3.6 | — | ±5 | μA | V _{IN} = V _{CC} or GND |
| | I _{IN (hold)} | 2.3 | 45 | — | | V _{IN} = 0.7 V |
| | | 2.3 | -45 | — | | V _{IN} = 1.7 V |
| | | 3.0 | 75 | — | | V _{IN} = 0.8 V |
| | | 3.0 | -75 | — | | V _{IN} = 2.0 V |
| | | 3.6 | — | ±500 | | V _{IN} = 0 to 3.6 V |
| Off state output current ^{*2} | I _{OZ} | 3.6 | — | ±10 | μA | V _{OUT} = V _{CC} or GND |
| Quiescent supply current | I _{CC} | 3.6 | — | 40 | μA | V _{IN} = V _{CC} or GND |
| | ΔI _{CC} | 3.0 to 3.6 | — | 750 | μA | V _{IN} = one input at (V _{CC} -0.6) V, other inputs at V _{CC} or GND |

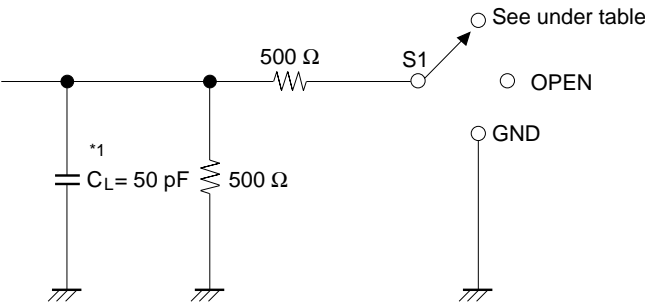
Notes: 1. For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

2. For I/O ports, the parameter I_{OZ} includes the input leakage current.

Switching Characteristics (Ta = -40 to 85°C)

| Item | Symbol | V _{CC} (V) | Min | Typ | Max | Unit | FROM (Input) | TO (Output) |
|------------------------|-------------------|---------------------|-----|-----|-----|------|--|----------------|
| Propagation delay time | t _{PLH} | 2.5±0.2 | 1.0 | — | 6.2 | ns | A or B | B or A |
| | t _{PHL} | 2.7 | — | — | 5.5 | | | |
| | | 3.3±0.3 | 1.0 | — | 4.9 | | | |
| | | 2.5±0.2 | 1.1 | — | 7.6 | | $\overline{\text{LE}}$ | A or B |
| | | 2.7 | — | — | 6.9 | | | |
| | | 3.3±0.3 | 1.1 | — | 5.6 | | | |
| Output enable time | t _{ZH} | 2.5±0.2 | 1.0 | — | 8.2 | ns | $\overline{\text{CE}}$ | A or B |
| | t _{ZL} | 2.7 | — | — | 7.6 | | | |
| | | 3.3±0.3 | 1.0 | — | 6.2 | | | |
| | | 2.5±0.2 | 1.0 | — | 7.8 | | $\overline{\text{OE}}$ | A or B |
| | | 2.7 | — | — | 7.0 | | | |
| | | 3.3±0.3 | 1.0 | — | 5.9 | | | |
| Output disable time | t _{HZ} | 2.5±0.2 | 2.0 | — | 6.8 | ns | $\overline{\text{CE}}$ | A or B |
| | t _{LZ} | 2.7 | — | — | 6.7 | | | |
| | | 3.3±0.3 | 1.5 | — | 5.6 | | | |
| | | 2.5±0.2 | 1.6 | — | 6.4 | | $\overline{\text{OE}}$ | A or B |
| | | 2.7 | — | — | 5.3 | | | |
| | | 3.3±0.3 | 1.1 | — | 5.1 | | | |
| Setup time | t _{su} | 2.5±0.2 | 1.2 | — | — | ns | Data before $\overline{\text{CE}}\uparrow$ | |
| | | 2.7 | 1.5 | — | — | | | |
| | | 3.3±0.3 | 1.2 | — | — | | | |
| | | 2.5±0.2 | 1.2 | — | — | | Data before $\overline{\text{LE}}\uparrow$ | |
| | | 2.7 | 1.5 | — | — | | $\overline{\text{CE}}$ "L" | |
| | | 3.3±0.3 | 1.2 | — | — | | | |
| Hold time | t _h | 2.5±0.2 | 1.2 | — | — | ns | Data after $\overline{\text{CE}}\uparrow$ | |
| | | 2.7 | 0.8 | — | — | | | |
| | | 3.3±0.3 | 1.3 | — | — | | | |
| | | 2.5±0.2 | 1.2 | — | — | | Data after $\overline{\text{LE}}\uparrow$ | |
| | | 2.7 | 0.8 | — | — | | $\overline{\text{CE}}$ "L" | |
| | | 3.3±0.3 | 1.3 | — | — | | | |
| Pulse width | t _w | 2.5±0.2 | 3.3 | — | — | ns | $\overline{\text{CE}}$ or $\overline{\text{LE}}$ "L" | |
| | | 2.7 | 3.3 | — | — | | | |
| | | 3.3±0.3 | 3.3 | — | — | | | |
| Input capacitance | C _{IN} | 3.3 | — | 3.5 | — | pF | Control inputs | |
| Output capacitance | C _{IN/O} | 3.3 | — | 7.0 | — | pF | A or B ports | |

• Test Circuit

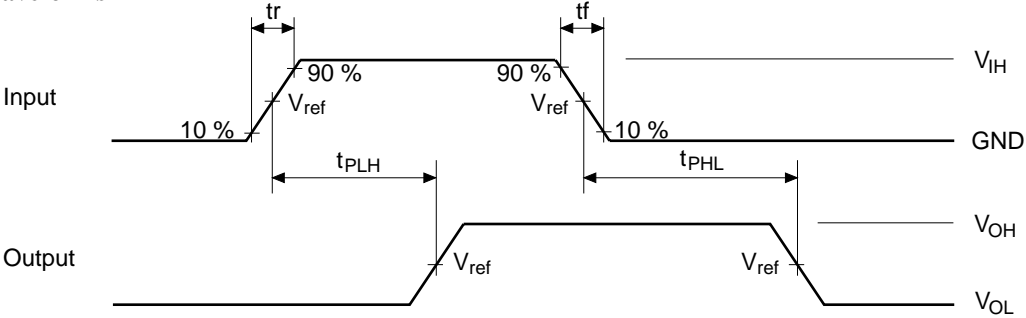


Load Circuit for Outputs

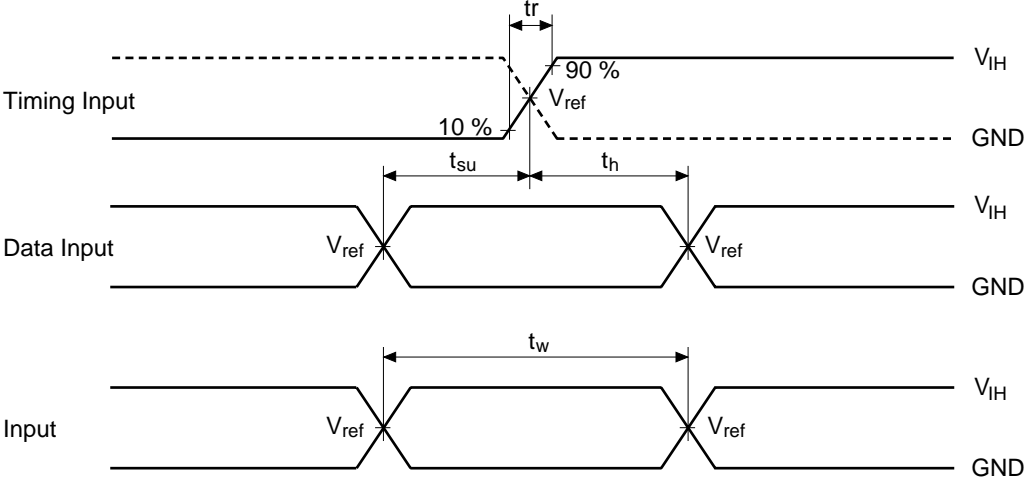
| Symbol | Vcc=2.5±0.2V | Vcc=2.7V, 3.3±0.3V |
|---|--------------|-----------------------|
| t _{PLH} /t _{PHL} | OPEN | OPEN |
| t _{su} /t _h /t _w | OPEN | OPEN |
| t _{ZH} /t _{HZ} | GND | GND |
| t _{ZL} /t _{LZ} | 4.6 V | 6.0 V |

Note: 1. C_L includes probe and jig capacitance.

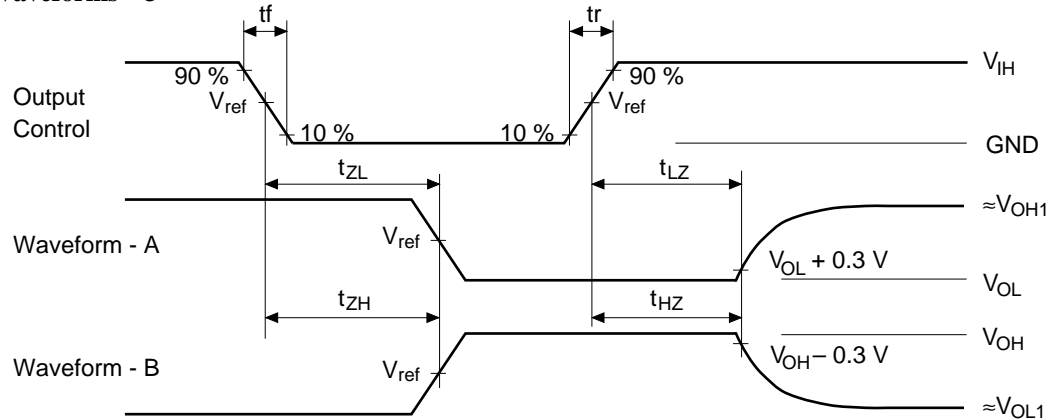
• Waveforms – 1



• Waveforms – 2



• Waveforms – 3

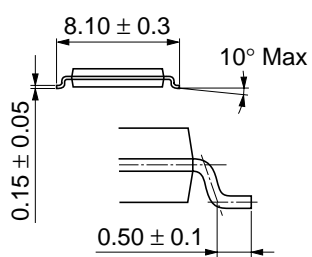
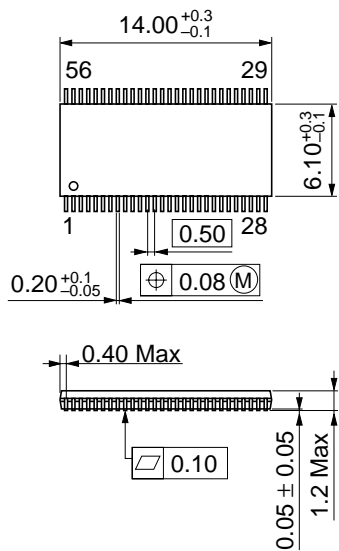


| TEST | V _{CC} =2.5±0.2V | V _{CC} =2.7V, 3.3±0.3V |
|------------------|---------------------------|------------------------------------|
| V _{IH} | 2.3 V | 2.7 V |
| V _{ref} | 1.2 V | 1.5 V |
| V _{OH1} | 2.3 V | 3.0 V |
| V _{OL1} | GND | GND |

- Notes:
1. All input pulses are supplied by generators having the following characteristics:
PRR ≤ 10 MHz, Z_o = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
 3. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.
 4. The output are measured one at a time with one transition per measurement.

Package Dimensions

Unit : mm



| | |
|--------------|---------|
| Hitachi code | TTP-56D |
| EIAJ code | — |
| JEDEC code | — |

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

| | | |
|-----|------------------|---|
| URL | NorthAmerica | : http://semiconductor.hitachi.com/ |
| | Europe | : http://www.hitachi-eu.com/hel/ecg |
| | Asia (Singapore) | : http://www.has.hitachi.com.sg/grp3/sicd/index.htm |
| | Asia (Taiwan) | : http://www.hitachi.com.tw/E/Product/SICD_Frame.htm |
| | Asia (HongKong) | : http://www.hitachi.com.hk/eng/bo/grp3/index.htm |
| | Japan | : http://www.hitachi.co.jp/Sicd/indx.htm |

For further information write to:

| | |
|--|---|
| Hitachi Semiconductor (America) Inc. 179 East Tasman Drive, San Jose, CA 95134 Tel: <1> (408) 433-1990 Fax: <1> (408) 433-0223 | Hitachi Europe GmbH Electronic components Group Dornacher Straße 3 D-85622 Feldkirchen, Munich Germany Tel: <49> (89) 9 9180-0 Fax: <49> (89) 9 29 30 00 Hitachi Europe Ltd. Electronic Components Group. Whitebrook Park Lower Cookham Road Maidenhead Berkshire SL6 8YA, United Kingdom Tel: <44> (1628) 585000 Fax: <44> (1628) 778322 |
|--|---|

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building, No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

Copyright ' Hitachi, Ltd., 1999. All rights reserved. Printed in Japan.